Product Brochure
ECK33-B Core Board



Chengdu Ebyte Electronic Technology Co.,Ltd.

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1. Product Overview

1.1.Product Introduction

Ebyte ECK33-B series core board is carefully designed based on Allwinner's T536 series processor, and adopts a new LGA interface form of high performance, low power consumption, high reliability, and domestically produced industrial-grade embedded core board. It can be widely used in content sharing and self-service terminals, intelligent manufacturing, and other electronic business and industrial equipment.

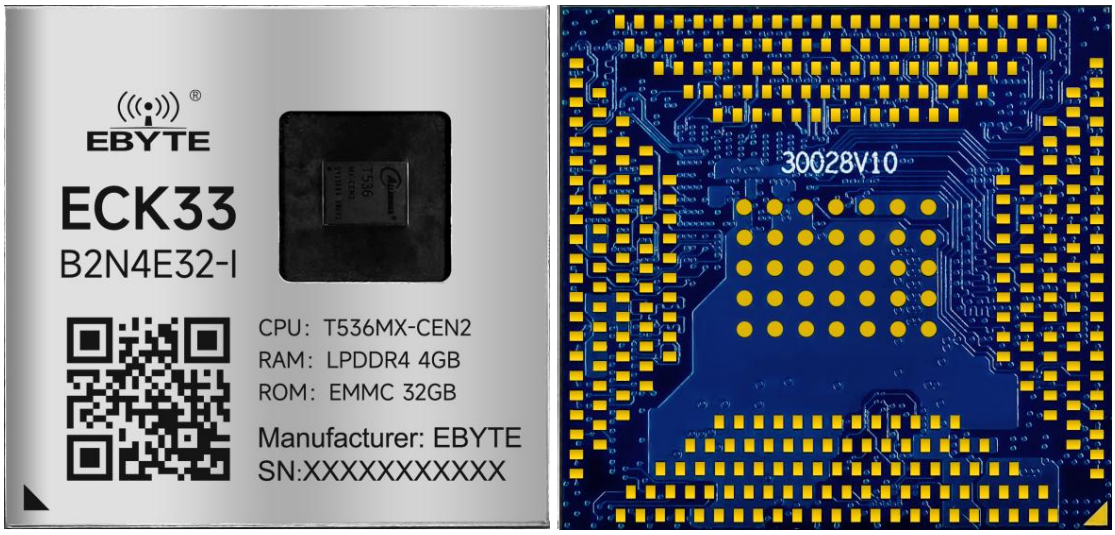
Allwinner T536 series is a SoC product with a high-performance quad- core Cortex-A55 AI platform , suitable for commercial, industrial and automotive fields. The chip family integrates a quad- core Cortex-A55 CPU, E907 RISC-V MCU, 2 TOPS NPU, 32-bit DDR3/DDR3L/DD4/LPDDR3/LPDDR4/LPDDR4X DRAM, high-speed interfaces (PCIe2.1 and USB3.1), automotive interfaces (CAN FD), multiple video output interfaces (RGB , Dual-link LVDS , MIPI-DSI) and video input interfaces (MIPI - CSI). The chip family supports 4K@ 25 fps H.26 4 encoder , 4K@ 15 fps MJPEG encoder , and supports geometric distortion correction (GDC), including lens distortion correction (LDC) and fisheye correction (FEC), providing users with efficient video acquisition and processing .

The ECK33-B series core board includes 2 specific product models, both of which are designed with domestically produced industrial-grade devices. They mainly differ in NPU support, DRAM memory capacity, eMMC storage capacity, etc. Customers can choose the appropriate model according to their needs. For product selection, please refer to the product selection section.

The physical picture of the ECK33-B series core board (no components on the bottom of the product) is as follows:

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Physical picture

1.2.Features

1. Processor: Allwinner T536MX series processor;
   - Quad-core ARM CortexTM-A55@1.6GHz;
   - E907 RISC-V MCU@600MHz;
   - NPU 2 TOPS (supported only by T536MX-CEN2);
   - ECC data protection;
2. Display Engine:
   - MJPEG Decoder , supports up to 3840 x 2160@15fps ;
   - JPEG Decoder , supports up to 1920 x 1080@60fps ;
   - H.264 Encoder , supports up to 3840 x 2160@25fps ;
   - JPEG Encoder , supports up to 3840 x 2160@15fps ;
   - MJPEG Encoder , supports up to 3840 x 2160@15fps ;
3. Memory: Onboard LPDDR4 2GB/4GB, 32bits;
4. Storage: 16GB/32GB eMMC optional;
5. Video Output:
   - 1 Dual -link LVDS , maximum support 1920 x 1080@60fps ;
   - 1 -way 4-lane MIPI DSI , supporting up to 1920 x 1200@60fps ;
   - 1 channel RGB , maximum support 1920 x 1200@60fps ;
6. Video Input:
   - MIPI CSI, configurable 4+4-lane or 4+2+2-lane or 2+2+2+2-lane;

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- Parallel CSI , supports 8/10/12/16-bit width;

7. Audio:

- 1 channel audio differential lineout output (LINEOUTP/N);
- 4-way I2S/PCM interface (I2S0, I2S1, I2S2, and I2S3);
- Supports up to 8 digital PDM microphones;
- 1-channel OWA TX and 1-channel OWA RX, compliant with S/PDIF interface specifications;

8. Network: 2-way Gigabit Ethernet controller, supporting RGMII/RMII interface;

9. PCIE : 1-channel PCIe2.1, RC mode (multiplexed with USB3.1);

10. USB: 1-channel USB2.0 DRD, 1-channel USB2.0 HOST;

- 1-channel USB2.0 DRD ;
- 1-way USB2.0 Host ;
- 1 USB3.1 DRD (multiplexed with PCIe2.1) ;

11. SDIO: 2- way SD/MMC Host controller;

- SMHC0 , compliant with SD3.0 specification;
- SMHC1 , compliant with SDIO3.0 specification;

12. 17-channel UART;

13. 4-way CAN FD ;

14. 9-way I2C;

15. 34 -channel PWM;

16. 6-way SPI;

17. ADC:

- 1 LRADC, 6 bits, maximum 2KHz sampling rate;
- 28-channel GPADC, 12 bits, maximum 1MHz sampling rate;

18. 4-way IR RX, 1-way IR TX;

19. Supports up to 1024 LED serial connections;

20. Supports up to 199 GPIOs and GPIO interrupts;

21. power supply:

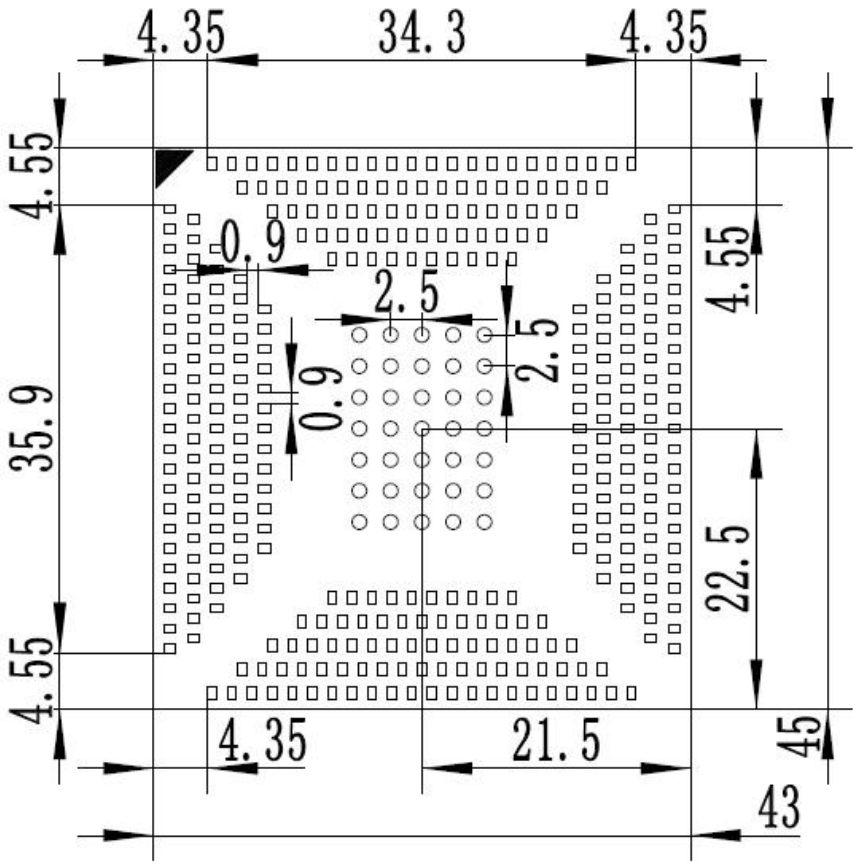
- Single DC +5V±10%@2A power input;
- 1 3.3V@500mA power output;

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22.Interface type: LGA 381 PIN;

23.PCB size: 45×43×1.6mm, as shown in the figure below:



Dimensions

24.Operating Temperature:

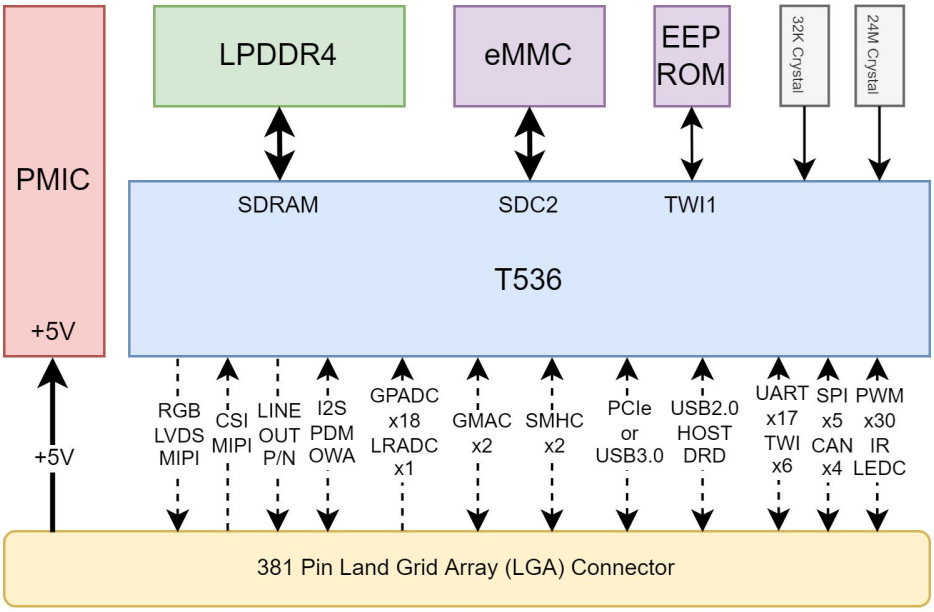
- Industrial grade: -40℃-85℃;

25.PCB technology: 12-layer board design, immersion gold, lead-free technology;

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1.3.Core board functional block diagram



Functional Block Diagram

1.4.Typical Applications

- Smart home;
- Smart toys;
- Smart cities;
- Tablet computer ;
- IoT Gateway ;
- Advertising all-in-one machine ;
- Industrial all-in-one machine ;
- Industrial control motherboard;
- Robots and drones.

2. Product Selection

2.1.Model configuration

The ECK33-B series core board selection and configuration table is as follows:

Product Selection and Configuration Table

Serial number	Product Model	Processor model	Memory	storage	Operating temperature
1	ECK33-B2N4E32-I	T536MX-CEN2	4GB	32GB	Domestic industrial grade

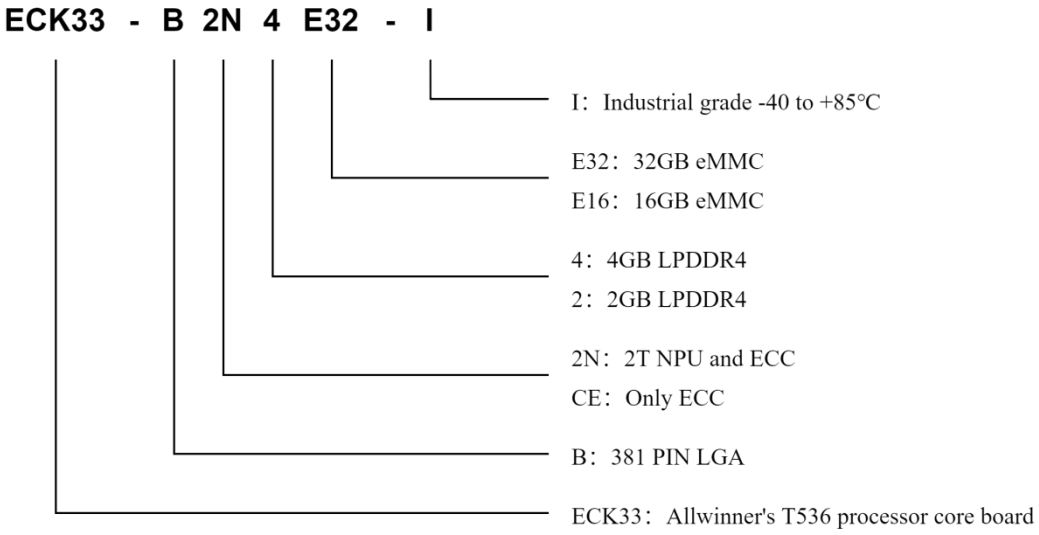
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			LPDDR4	eMMC	-40℃ ~85℃
2	ECK33-BCE2E16-I	T536MX-CEX	2GB LPDDR4	16 GB eMMC	Domestic industrial grade -40℃ ~85℃

2.2.Model code

The product model coding is shown in the figure below:



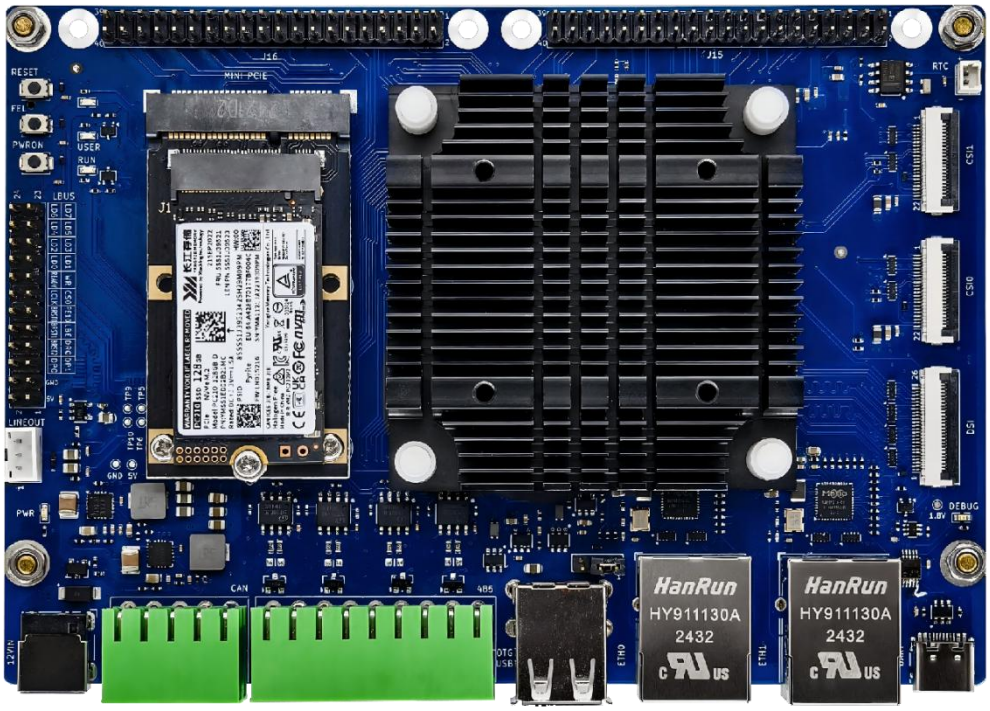
Model code description

3. Quick Experience

Choosing Ebyte ECB33-PGB series single board computer products, you can quickly experience the typical application functions of ECK33-B core board products, and understa nd the development methods such as baseboard hardware design and software developmen t.

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ECB33-PGB Series Single Board Computer Product Photos

4. Features and parameters

4.1.Product Features

The ECK33-B series core board mainly integrates the processor, DRAM memory, eMMC storage and PMIC power system, and leads out all the I/O pins on the processor. Users can design the baseboard to apply the I/O resources on the core board according to their needs and reuse the I/O into the functional interface they need.

The following table lists the main function parameters of the ECK33-B series core board integrated on the board, and the function parameters of the reusable I/O resources. The description of each I/O function is the maximum indicator that the core board can use the I/O function without using other I/O functions (for example, after using the 24-bit color RGB interface function and the network interface function, all UART functions cannot be realized).

Product Features

Function	Functional Description
CPU	T536MX-CEN2 / T536MX-CEX; Quad-core ARM Cortex-A55, up to 1.6GHz; E907 RISC-V MCU, up to 600MHz;

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	NPU up to 2 TOPS (CEX not support); ECC Protection;
ISP	Supports multiple sensor (up to 4) inputs; Supports raw8/10/12/14/16; Performance of one sensor: Online: 5M@30fps (linear), 5M@30fps(2f-wdr); Offline: 8M@30fps (linear), 8M@30fps (2f-wdr);
MEM	On board 2GB LPDDR4 / 4GB LPDDR4;
FLASH	On board 16GB/32GB eMMC;
Video Engine	MJPEG Decoder, up to 3840 x 2160@15fps; JPEG Decoder, up to 1920 x 1080@60fps; H.264 Encoder, up to 3840 x 2160@25fps; JPEG Encoder, up to 3840 x 2160@15fps; MJPEG Encoder, up to 3840 x 2160@15fps;
Video Output	1x Dual-link LVDS, up to 1920 x 1080@60fps; 1x 4-lane MIPI DSI, up to 1920 x 1200@60fps; 1x RGB, up to 1920 x 1200@60fps;
Video Input	4+4-lane or 4+2+2-lane or 2+2+2+2-lane MIPI CSI; 8/10/12/16-bit Parallel CSI;
Audio	1x audio differential lineout output: LINEOUTP/N; 4x I2S/PCM interfaces (I2S0, I2S1, I2S2, and I2S3); Supports maximum 8 digital PDM microphones; 1x OWA TX and 1x OWA RX, compliant with S/PDIF interface;
GMAC	2x 10/100/1000Mbit/s Ethernet with RGMII and RMII interfaces;
SMHC	2x SD/MMC Host Controller (SMHC) interfaces; SMHC0, compliant Secure Digital Memory (up to SD3.0); SMHC1, compliant Secure Digital I/O (up to SDIO3.0);
PCIe	1x PCIe2.1&USB3.1 combo PHY; Compliance to PCI Express Base Specification, Revision 2.1; Supports 1 lane link width, Root Complex (RC) mode;
USB	1 x USB2.0 Host; 1 x USB2.0 DRD; 1 x USB3.1 DRD&PCIe2.1 Combo;
Local Bus	1x 8/16-bit wide Local Bus;
UART	17x UART, compatible with industry-standard 16450/16550;
TWI	9x TWI, compliant with I2C bus standard;
SPI	6x SPI, support SPI mode and display bus interface (DBI) mode;
CAN	4x CAN-FD ports (up to 64 data bytes);
PWM	30x PWM channels and 4x S-PWM channels;
ADC	1x LRADC, 6-bit resolution up to 2KHz sampling rate; 2 8x GPADC, 12-bit resolution up to 1MHz sampling rate;
led	Maximum 1024 LEDs serial connect;
IR	1x IR_TX interface, 4x IR_RX interface;
GPIO	199x GPIOs and GPIO interrupt input;

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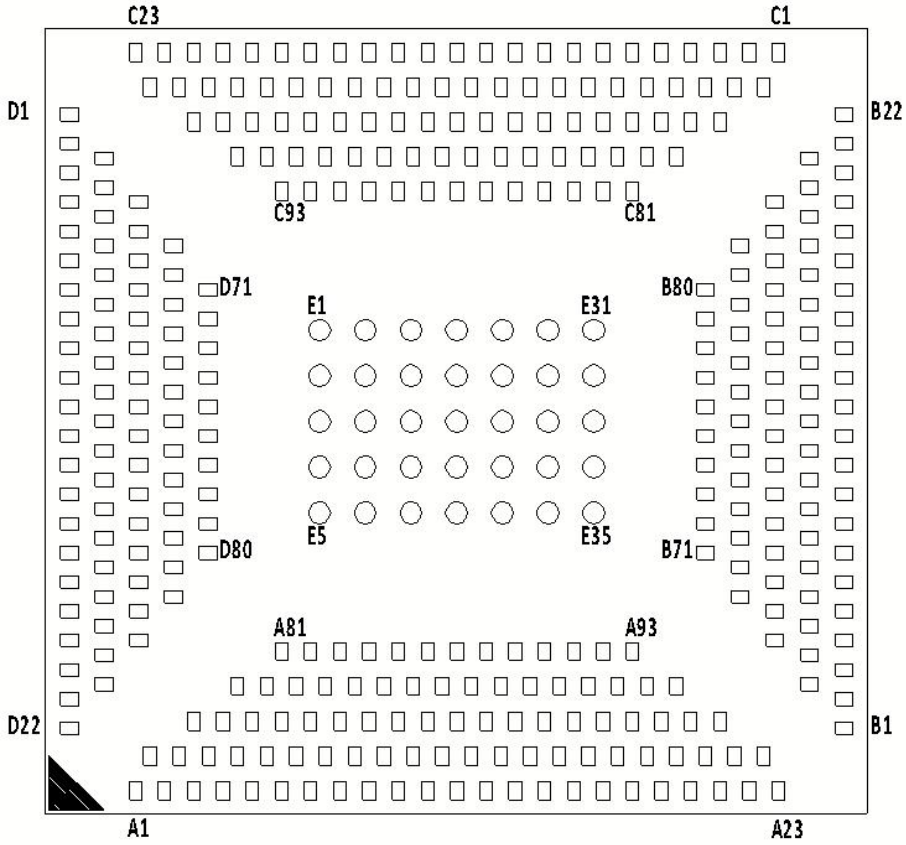
4.2.Environmental characteristics

Environmental characteristics table

Operating temperature	Industrial Grade	-40℃ ~85℃;
Storage temperature	-40℃ ~85℃;	
Operating humidity	5% to 95% humidity, non-condensing;	
Storage humidity	60℃@95% humidity, non-condensing;	

4.3.I/O features

4.3.1. Pin numbering diagram



Pin Numbering Diagram (Top View)

Note: The above picture is a top view, which is a mirror image of the pins observed from the bottom of the actual object.

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4.3.2. Pin Definition Table

The ECK33-B core board interface pin definitions are shown in the following table. If you need to change the pin function, please modify the relevant driver configuration code.

Pin Definition Table

LGA	Pin Name	MPU	Power Rail	Type	Comment
A01	VDD_IN_5V	/	VDD_IN_5/5.0V	PWR	External input 5V
A02	VDD_IN_5V	/	VDD_IN_5/5.0V	PWR	External input 5V
A03	VDD_IN_5V	/	VDD_IN_5/5.0V	PWR	External input 5V
A04	VDD_IN_5V	/	VDD_IN_5/5.0V	PWR	External input 5V
A05	DGND	/	DGND/0.0V	GND	
A06	DGND	/	DGND/0.0V	GND	
A07	PC3	Y3	CLDO1/1.8V	I/O	
A08	PC2	V5	CLDO1/1.8V	I/O	
A09	PC4	Y4	CLDO1/1.8V	I/O	
A10	DGND	/	DGND/0.0V	GND	
A11	GPADC3-0	H27	ALDO4/1.8V	AI	
A12	DGND	/	DGND/0.0V	GND	
A13	DGND	/	DGND/0.0V	GND	
A14	AP-CK24M-OUT	AH28	ALDO4/1.8V	AO	
A15	AP-CK32K-OUT	AF28	RTC/1.8V	AO	1nF pull down, 10KΩ pull up
A16	DGND	/	DGND/0.0V	GND	
A17	DGND	/	DGND/0.0V	GND	
A18	DGND	/	DGND/0.0V	GND	
A19	DGND	/	DGND/0.0V	GND	
A20	PA_GPADC06	G29	CLDO4/3.3V	I/O	1.8V for ADC and 3.3V for GPIO
A21	PA_GPADC02	F27	CLDO4/3.3V	I/O	1.8V for ADC and 3.3V for GPIO
A22	PA_GPADC09	H26	CLDO4/3.3V	I/O	1.8V for ADC and 3.3V for GPIO
A23	PI12	F21	DCDC4/3.3V	I/O	
A24	VDD_IN_5V	/	VDD_IN_5/5.0V	PWR	External input 5V
A25	VDD_IN_5V	/	VDD_IN_5/5.0V	PWR	External input 5V
A26	VDD_IN_5V	/	VDD_IN_5/5.0V	PWR	External input 5V
A27	VDD_IN_5V	/	VDD_IN_5/5.0V	PWR	External input 5V
A28	DGND	/	DGND/0.0V	GND	
A29	PC12	Y5	CLDO1/1.8V	I/O	
A30	PC7	Y7	CLDO1/1.8V	I/O	
A31	DGND	/	DGND/0.0V	GND	
A32	GPADC1-0	J29	ALDO4/1.8V	AI	1nF pull down
A33	GPADC1-1	H28	ALDO4/1.8V	AI	1nF pull down

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A34	GPADC1-2	J27	ALDO4/1.8V	AI	1nF pull down
A35	GPADC1-3	J28	ALDO4/1.8V	AI	1nF pull down
A36	DGND	/	DGND/0.0V	GND	
A37	DGND	/	DGND/0.0V	GND	
A38	DGND	/	DGND/0.0V	GND	
A39	DGND	/	DGND/0.0V	GND	
A40	DGND	/	DGND/0.0V	GND	
A41	PA_GPADC05	F28	CLDO4/3.3V	I/O	1.8V for ADC and 3.3V for GPIO
A42	PA_GPADC03	E28	CLDO4/3.3V	I/O	1.8V for ADC and 3.3V for GPIO
A43	PA_GPADC04	E29	CLDO4/3.3V	I/O	1.8V for ADC and 3.3V for GPIO
A44	PA_GPADC07	G28	CLDO4/3.3V	I/O	1.8V for ADC and 3.3V for GPIO
A45	PA_GPADC08	G27	CLDO4/3.3V	I/O	1.8V for ADC and 3.3V for GPIO
A46	VDD_IN_5V	/	VDD_IN_5/5.0V	PWR	External input 5V
A47	VDD_IN_5V	/	VDD_IN_5/5.0V	PWR	External input 5V
A48	DGND	/	DGND/0.0V	GND	
A49	DGND	/	DGND/0.0V	GND	
A50	GPADC2-5	N27	ALDO4/1.8V	AI	
A51	GPADC2-6	N28	ALDO4/1.8V	AI	
A52	GPADC2-8	P26	ALDO4/1.8V	AI	
A53	GPADC2-9	P27	ALDO4/1.8V	AI	
A54	GPADC2-4	M28	ALDO4/1.8V	AI	
A55	GPADC2-7	N29	ALDO4/1.8V	AI	
A56	DGND	/	DGND/0.0V	GND	
A57	DGND	/	DGND/0.0V	GND	
A58	DGND	/	DGND/0.0V	GND	
A59	DGND	/	DGND/0.0V	GND	
A60	DGND	/	DGND/0.0V	GND	
A61	DGND	/	DGND/0.0V	GND	
A62	DGND	/	DGND/0.0V	GND	
A63	DGND	/	DGND/0.0V	GND	
A64	DGND	/	DGND/0.0V	GND	
A65	VCC33-IO	/	CLDO3/3.3V	PWR	Core board outputs 3V3
A66	VCC33-IO	/	CLDO3/3.3V	PWR	Core board outputs 3V3
A67	DGND	/	DGND/0.0V	GND	
A68	DGND	/	DGND/0.0V	GND	
A69	LRADC	P28	ALDO4/1.8V	AI	
A70	GPADC1-7	K26	ALDO4/1.8V	AI	
A71	GPADC1-8	L28	ALDO4/1.8V	AI	
A72	GPADC1-9	M24	ALDO4/1.8V	AI	
A73	DGND	/	DGND/0.0V	GND	
A74	DGND	/	DGND/0.0V	GND	

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A75	DGND	/	DGND/0.0V	GND	
A76	DGND	/	DGND/0.0V	GND	
A77	DGND	/	DGND/0.0V	GND	
A78	DGND	/	DGND/0.0V	GND	
A79	DGND	/	DGND/0.0V	GND	
A80	DGND	/	DGND/0.0V	GND	
A81	DGND	/	DGND/0.0V	GND	
A82	DGND	/	DGND/0.0V	GND	
A83	GPADC2-0	L27	ALDO4/1.8V	AI	
A84	GPADC2-1	M25	ALDO4/1.8V	AI	
A85	GPADC2-2	M26	ALDO4/1.8V	AI	
A86	GPADC2-3	M27	ALDO4/1.8V	AI	
A87	DGND	/	DGND/0.0V	GND	
A88	DGND	/	DGND/0.0V	GND	
A89	DGND	/	DGND/0.0V	GND	
A90	DGND	/	DGND/0.0V	GND	
A91	DGND	/	DGND/0.0V	GND	
A92	DGND	/	DGND/0.0V	GND	
A93	DGND	/	DGND/0.0V	GND	
B01	PH4	B6	DCDC4/3.3V	I/O	
B02	PH5	A6	DCDC4/3.3V	I/O	
B03	PH7	B7	DCDC4/3.3V	I/O	
B04	PH6	C6	DCDC4/3.3V	I/O	
B05	DGND	/	DGND/0.0V	GND	
B06	PL2	W28	ALDO3/3V3	I/O	
B07	PL3	W29	ALDO3/3V3	I/O	
B08	PB9	AH26	CLDO3/3.3V	I/O	
B09	PB10	AG26	CLDO3/3.3V	I/O	
B10	PL10	AA27	ALDO3/3V3	I/O	
B11	PL11	AA28	ALDO3/3V3	I/O	
B12	PB12	AC23	CLDO3/3.3V	I/O	
B13	PB11	AF25	CLDO3/3.3V	I/O	
B14	PI9	E25	DCDC4/3.3V	I/O	
B15	PI8	D25	DCDC4/3.3V	I/O	
B16	PI11	E21	DCDC4/3.3V	I/O	
B17	DGND	/	DGND/0.0V	GND	
B18	U3-PCIE21-RXP	B23	CLDO1/1.8V	AI	
B19	U3-PCIE21-RXN	A23	CLDO1/1.8V	AI	
B20	DGND	/	DGND/0.0V	GND	
B21	PCIE21-REFCLKP	B24	CLDO1/1.8V	AI/O	
B22	PCIE21-REFCLKN	A24	CLDO1/1.8V	AI/O	

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B23	PB13	AJ25	CLDO3/3.3V	I/O	
B24	PB14	AH25	CLDO3/3.3V	I/O	
B25	PB4	AE23	CLDO3/3.3V	I/O	
B26	PB5	AD23	CLDO3/3.3V	I/O	
B27	DGND	/	DGND/0.0V	GND	
B28	DGND	/	DGND/0.0V	GND	
B29	DGND	/	DGND/0.0V	GND	
B30	DGND	/	DGND/0.0V	GND	
B31	PL12	AB26	ALDO3/3V3	I/O	
B32	PL13	AB25	ALDO3/3V3	I/O	
B33	DGND	/	DGND/0.0V	GND	
B34	DGND	/	DGND/0.0V	GND	
B35	PI10	D21	DCDC4/3.3V	I/O	
B36	PI7	B26	DCDC4/3.3V	I/O	
B37	PI6	A27	DCDC4/3.3V	I/O	
B38	PI16	B25	DCDC4/3.3V	I/O	
B39	PI15	A26	DCDC4/3.3V	I/O	
B40	U3-PCIE21-TXP	B22	CLDO1/1.8V	AO	
B41	U3-PCIE21-TXN	A22	CLDO1/1.8V	AO	
B42	PL4	AA29	ALDO3/3V3	I/O	
B43	PL5	Y27	ALDO3/3V3	I/O	
B44	PL7	Y25	ALDO3/3V3	I/O	
B45	PL6	Y26	ALDO3/3V3	I/O	
B46	DGND	/	DGND/0.0V	GND	
B47	DGND	/	DGND/0.0V	GND	
B48	DGND	/	DGND/0.0V	GND	
B49	DGND	/	DGND/0.0V	GND	
B50	PM4	AC29	BLDO2/1.8V	I/O	
B51	PM2	AD28	BLDO2/1.8V	I/O	
B52	/	/	/	N/A	
B53	PM3	AC27	BLDO2/1.8V	I/O	
B54	DGND	/	DGND/0.0V	GND	
B55	DGND	/	DGND/0.0V	GND	
B56	PI13	D23	DCDC4/3.3V	I/O	
B57	PI14	E23	DCDC4/3.3V	I/O	
B58	DGND	/	DGND/0.0V	GND	
B59	DGND	/	DGND/0.0V	GND	
B60	PF3_SDC0-CMD	AG22	CLDO3/3.3V	I/O	1.8V for SDIO and 3.3V for GPIO
B61	PF6	AF21	CLDO3/3.3V	I/O	1.8V for SDIO and 3.3V for GPIO
B62	PF2_SDC0-CLK	AH22	CLDO3/3.3V	I/O	33Ω in series, 1.8V for SDIO and 3.3V for GPIO

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B63	DGND	/	DGND/0.0V	GND	
B64	PL8	AB28	ALDO3/3V3	I/O	
B65	PL9	AB27	ALDO3/3V3	I/O	
B66	PM0	AD27	BLDO2/1.8V	I/O	
B67	PM1	AE29	BLDO2/1.8V	I/O	
B68	PM5	AC28	BLDO2/1.8V	I/O	
B69	PG9	V28	BLDO1/3.3V	I/O	
B70	PG8	V27	BLDO1/3.3V	I/O	
B71	PF4_SDC0-D3	AJ23	CLDO3/3.3V	I/O	1.8V for SDIO and 3.3V for GPIO
B72	PF4_SDC0-D2	AH23	CLDO3/3.3V	I/O	1.8V for SDIO and 3.3V for GPIO
B73	PF4_SDC0-D1	AH21	CLDO3/3.3V	I/O	1.8V for SDIO and 3.3V for GPIO
B74	PF4_SDC0-D0	AG21	CLDO3/3.3V	I/O	1.8V for SDIO and 3.3V for GPIO
B75	PB3	AF23	CLDO3/3.3V	I/O	
B76	PB0	AC21	CLDO3/3.3V	I/O	
B77	PB1	AB21	CLDO3/3.3V	I/O	
B78	PB2	AG24	CLDO3/3.3V	I/O	
B79	PG6	T24	BLDO1/3.3V	I/O	
B80	PG7	T25	BLDO1/3.3V	I/O	
C01	LINEOUTP	D28	ALDO4/1.8V	AO	
C02	LINEOUTN	D29	ALDO4/1.8V	AO	
C03	DGND	/	DGND/0.0V	GND	
C04	AP-RESET	AF27	RTC/1.8V	I/O	1nF pull down, 100Ω in series, 10KΩ pull up
C05	AP-PWRON	/	RTC/1.8V	DI	100nF pull down, 100Ω in series
C06	/	/	/	N/A	
C07	PG5_SDC1-D3	U28	BLDO1/3.3V	I/O	
C08	PG4_SDC1-D2	U29	BLDO1/3.3V	I/O	
C09	PG3_SDC1-D1	R27	BLDO1/3.3V	I/O	
C10	PG2_SDC1-D0	R28	BLDO1/3.3V	I/O	
C11	DGND	/	DGND/0.0V	GND	
C12	PE7_LB	E13	DCDC4/3.3V	I/O	
C13	PE6_LB	D13	DCDC4/3.3V	I/O	
C14	PE5_LB	E11	DCDC4/3.3V	I/O	
C15	PE4_LB	F11	DCDC4/3.3V	I/O	
C16	PE3_LB	G11	DCDC4/3.3V	I/O	
C17	PE2_LB	F9	DCDC4/3.3V	I/O	
C18	PE1_LB	G9	DCDC4/3.3V	I/O	
C19	PE0_LB	B9	DCDC4/3.3V	I/O	
C20	DGND	/	DGND/0.0V	GND	
C21	PD12_LCD_LV1-D1P	F1	DCDC4/3.3V	I/O	1.8V for LVDS and 3.3V for GPIO
C22	PD14_LCD_LV1-D2P	G1	DCDC4/3.3V	I/O	1.8V for LVDS and 3.3V for GPIO

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C23	PD13_LCD_LV1-D1N	F2	DCDC4/3.3V	I/O	1.8V for LVDS and 3.3V for GPIO
C24	USB0-DM	B20	CLDO3/3.3V	AI/O	
C25	USB0-DP	A20	CLDO3/3.3V	AI/O	
C26	DGND	/	DGND/0.0V	GND	
C27	FEL	AD21	CLDO3/3.3V	DI	1nF pull down, 100Ω in series
C28	AP-NMI	AE28	RTC/1.8V	I/O	1nF pull down, 10KΩ pull up
C29	PG13	U27	BLDO1/3.3V	I/O	
C30	PG14	P24	BLDO1/3.3V	I/O	
C31	PG1_SDC1-CMD	T27	BLDO1/3.3V	I/O	
C32	PG0_SDC1-CLK	R29	BLDO1/3.3V	I/O	33Ω in series
C33	DGND	/	DGND/0.0V	GND	
C34	DGND	/	DGND/0.0V	GND	
C35	PE13_LB	C9	DCDC4/3.3V	I/O	
C36	PE17_LB	F13	DCDC4/3.3V	I/O	
C37	PE8_LB	E9	DCDC4/3.3V	I/O	
C38	PE9_LB	D11	DCDC4/3.3V	I/O	
C39	PK9_LB_MIB-D1P	A14	DCDC4/3.3V	I/O	1.8V for CSI and 3.3V for GPIO
C40	PK5_LB_MIA-CKP	A12	DCDC4/3.3V	I/O	1.8V for CSI and 3.3V for GPIO
C41	PK2_LB_MIA-D1N	B11	DCDC4/3.3V	I/O	1.8V for CSI and 3.3V for GPIO
C42	PK0_LB_MIA-D0N	B13	DCDC4/3.3V	I/O	1.8V for CSI and 3.3V for GPIO
C43	DGND	/	DGND/0.0V	GND	
C44	PD11_LCD_LV1-D0N	E2	DCDC4/3.3V	I/O	1.8V for LVDS and 3.3V for GPIO
C45	PD15_LCD_LV1-D2N	G2	DCDC4/3.3V	I/O	1.8V for LVDS and 3.3V for GPIO
C46	USB1-DM	B21	CLDO3/3.3V	AI/O	
C47	USB1-DP	A21	CLDO3/3.3V	AI/O	
C48	DGND	/	DGND/0.0V	GND	
C49	PG10	V26	BLDO1/3.3V	I/O	
C50	PG12	T26	BLDO1/3.3V	I/O	
C51	PG11	V25	BLDO1/3.3V	I/O	
C52	PD18_LCD_LV1-D3P	J1	DCDC4/3.3V	I/O	1.8V for LVDS and 3.3V for GPIO
C53	PD19_LCD_LV1-D3N	J2	DCDC4/3.3V	I/O	1.8V for LVDS and 3.3V for GPIO
C54	PH12	C7	DCDC4/3.3V	I/O	
C55	PH13	B8	DCDC4/3.3V	I/O	
C56	PE12_LB	A10	DCDC4/3.3V	I/O	
C57	PE11_LB	C10	DCDC4/3.3V	I/O	
C58	PE10_LB	D9	DCDC4/3.3V	I/O	
C59	PK11_LB_MIB-CKP	A15	DCDC4/3.3V	I/O	1.8V for CSI and 3.3V for GPIO
C60	PK7_LB_MIB-D0P	A16	DCDC4/3.3V	I/O	1.8V for CSI and 3.3V for GPIO
C61	PK4_LB_MIA-CKN	B12	DCDC4/3.3V	I/O	1.8V for CSI and 3.3V for GPIO
C62	PK1_LB_MIA-D0P	A13	DCDC4/3.3V	I/O	1.8V for CSI and 3.3V for GPIO
C63	DGND	/	DGND/0.0V	GND	

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C64	PD10_LCD_LV1-D0P	E1	DCDC4/3.3V	I/O	1.8V for LVDS and 3.3V for GPIO
C65	PI2	C28	DCDC4/3.3V	I/O	
C66	PI3	C27	DCDC4/3.3V	I/O	
C67	PI5	D27	DCDC4/3.3V	I/O	
C68	PI4	C29	DCDC4/3.3V	I/O	
C69	PK16_LB_MIC-CKN	B18	DCDC4/3.3V	I/O	1.8V for CSI and 3.3V for GPIO
C70	PK17_LB_MIC-CKP	A18	DCDC4/3.3V	I/O	1.8V for CSI and 3.3V for GPIO
C71	PH9	F7	DCDC4/3.3V	I/O	
C72	PH8	G7	DCDC4/3.3V	I/O	
C73	PE15_LB	H13	DCDC4/3.3V	I/O	
C74	PE16_LB	G13	DCDC4/3.3V	I/O	
C75	PK15_LB_MIC-D1P	A17	DCDC4/3.3V	I/O	1.8V for CSI and 3.3V for GPIO
C76	PK13_LB_MIC-D0P	A19	DCDC4/3.3V	I/O	1.8V for CSI and 3.3V for GPIO
C77	PK10_LB_MIB-CKN	B15	DCDC4/3.3V	I/O	1.8V for CSI and 3.3V for GPIO
C78	PK6_LB_MIB-D0N	B16	DCDC4/3.3V	I/O	1.8V for CSI and 3.3V for GPIO
C79	PK3_LB_MIA-D1P	A11	DCDC4/3.3V	I/O	1.8V for CSI and 3.3V for GPIO
C80	DGND	/	DGND/0.0V	GND	
C81	PK18_LB_MID-D0N	D19	DCDC4/3.3V	I/O	1.8V for CSI and 3.3V for GPIO
C82	PK19_LB_MID-D0P	E19	DCDC4/3.3V	I/O	1.8V for CSI and 3.3V for GPIO
C83	PK21_LB_MID-D1P	D15	DCDC4/3.3V	I/O	1.8V for CSI and 3.3V for GPIO
C84	PK20_LB_MID-D1N	E15	DCDC4/3.3V	I/O	1.8V for CSI and 3.3V for GPIO
C85	PH1	F5	DCDC4/3.3V	I/O	
C86	PH0	G5	DCDC4/3.3V	I/O	
C87	PK22_LB_MID-CKN	E17	DCDC4/3.3V	I/O	1.8V for CSI and 3.3V for GPIO
C88	PK23_LB_MID-CKP	D17	DCDC4/3.3V	I/O	1.8V for CSI and 3.3V for GPIO
C89	DGND	/	DGND/0.0V	GND	
C90	PK14_LB_MIC-D1N	B17	DCDC4/3.3V	I/O	1.8V for CSI and 3.3V for GPIO
C91	PK12_LB_MIC-D0N	B19	DCDC4/3.3V	I/O	1.8V for CSI and 3.3V for GPIO
C92	PK8_LB_MIB-D1N	B14	DCDC4/3.3V	I/O	1.8V for CSI and 3.3V for GPIO
C93	PE14_LB	B10	DCDC4/3.3V	I/O	
D01	PD0_LCD_DSI-D0P	B5	DCDC4/3.3V	I/O	1.8V for LVDS and 3.3V for GPIO
D02	PD1_LCD_DSI-D0N	A5	DCDC4/3.3V	I/O	1.8V for LVDS and 3.3V for GPIO
D03	DGND	/	DGND/0.0V	GND	
D04	PD4_LCD_DSI-CKP	B3	DCDC4/3.3V	I/O	1.8V for LVDS and 3.3V for GPIO
D05	PD5_LCD_DSI-CKN	A3	DCDC4/3.3V	I/O	1.8V for LVDS and 3.3V for GPIO
D06	DGND	/	DGND/0.0V	GND	
D07	DGND	/	DGND/0.0V	GND	
D08	PJ22_MII1-TXCK	P7	DCDC4/3.3V	I/O	
D09	PJ23_MII1-TXCTL	P6	DCDC4/3.3V	I/O	
D10	PJ30_MII1-TXD3	M7	DCDC4/3.3V	I/O	
D11	PJ31_MII1-TXD2	M6	DCDC4/3.3V	I/O	

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D12	PJ20_MII1-TXD1	R3	DCDC4/3.3V	I/O	
D13	PJ21_MII1-TXD0	R2	DCDC4/3.3V	I/O	
D14	DGND	/	DGND/0.0V	GND	
D15	PH14	C8	DCDC4/3.3V	I/O	
D16	PH15	A8	DCDC4/3.3V	I/O	
D17	PB6	AD24	CLDO3/3.3V	I/O	
D18	PI1	B28	DCDC4/3.3V	I/O	
D19	PI0	B27	DCDC4/3.3V	I/O	
D20	DGND	/	DGND/0.0V	GND	
D21	PH11	D7	DCDC4/3.3V	I/O	
D22	PH10	E7	DCDC4/3.3V	I/O	
D23	PD2_LCD_DSI-D1P	B4	DCDC4/3.3V	I/O	1.8V for LVDS and 3.3V for GPIO
D24	PD3_LCD_DSI-D1N	A4	DCDC4/3.3V	I/O	1.8V for LVDS and 3.3V for GPIO
D25	DGND	/	DGND/0.0V	GND	
D26	PD8_LCD_DSI-D3P	D1	DCDC4/3.3V	I/O	1.8V for LVDS and 3.3V for GPIO
D27	PD9_LCD_DSI-D3N	D2	DCDC4/3.3V	I/O	1.8V for LVDS and 3.3V for GPIO
D28	DGND	/	DGND/0.0V	GND	
D29	PJ27_MII1-RXD3	M4	DCDC4/3.3V	I/O	
D30	PJ28_MII1-RXD2	K1	DCDC4/3.3V	I/O	
D31	PJ16_MII1-RXD1	M1	DCDC4/3.3V	I/O	
D32	PJ17_MII1-RXD0	M3	DCDC4/3.3V	I/O	
D33	DGND	/	DGND/0.0V	GND	
D34	PJ3_MII0-CLKIN	U3	DCDC4/3.3V	I/O	
D35	PJ10_MII0-2550M	U2	DCDC4/3.3V	I/O	
D36	DGND	/	DGND/0.0V	GND	
D37	PB8	AG25	CLDO3/3.3V	I/O	
D38	PB7	AH24	CLDO3/3.3V	I/O	
D39	DGND	/	DGND/0.0V	GND	
D40	PD17_LCD_LV1-CKN	H2	DCDC4/3.3V	I/O	1.8V for LVDS and 3.3V for GPIO
D41	PD16_LCD_LV1-CKP	H1	DCDC4/3.3V	I/O	1.8V for LVDS and 3.3V for GPIO
D42	DGND	/	DGND/0.0V	GND	
D43	PD6_LCD_DSI-D2P	C1	DCDC4/3.3V	I/O	1.8V for LVDS and 3.3V for GPIO
D44	PD7_LCD_DSI-D2N	C2	DCDC4/3.3V	I/O	1.8V for LVDS and 3.3V for GPIO
D45	DGND	/	DGND/0.0V	GND	
D46	PJ29_MII1-RXCK	K2	DCDC4/3.3V	I/O	
D47	PJ18_MII1-RXCTL	M2	DCDC4/3.3V	I/O	
D48	PJ19_MII1-CLKIN	L1	DCDC4/3.3V	I/O	
D49	PJ26_MII1-2550M	M5	DCDC4/3.3V	I/O	
D50	DGND	/	DGND/0.0V	GND	
D51	PJ6_MII0-TXCK	T7	DCDC4/3.3V	I/O	
D52	PJ7_MII0-TXCTL	T6	DCDC4/3.3V	I/O	

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D53	PJ9_MII0-MDIO	K5	DCDC4/3.3V	I/O	
D54	PJ8_MII0-MDC	P5	DCDC4/3.3V	I/O	
D55	DGND	/	DGND/0.0V	GND	
D56	/	/	/	N/A	
D57	/	/	/	N/A	
D58	PD20_LCD_HSYNC	K6	DCDC4/3.3V	I/O	1.8V for LVDS and 3.3V for GPIO
D59	PD21_LCD_VSYNC	H6	DCDC4/3.3V	I/O	1.8V for LVDS and 3.3V for GPIO
D60	PD22	H5	DCDC4/3.3V	I/O	
D61	DGND	/	DGND/0.0V	GND	
D62	PJ25_MII1-MDIO	K3	DCDC4/3.3V	I/O	
D63	PJ24_MII1-MDC	K4	DCDC4/3.3V	I/O	
D64	DGND	/	DGND/0.0V	GND	
D65	PJ14_MII0-TXD3	T4	DCDC4/3.3V	I/O	
D66	PJ15_MII0-TXD2	T5	DCDC4/3.3V	I/O	
D67	PJ4_MII0-TXD1	P4	DCDC4/3.3V	I/O	
D68	PJ5_MII0-TXD0	T3	DCDC4/3.3V	I/O	
D69	PJ2_MII0-RXCTL	P3	DCDC4/3.3V	I/O	
D70	DGND	/	DGND/0.0V	GND	
D71	PD23	H4	DCDC4/3.3V	I/O	
D72	DGND	/	DGND/0.0V	GND	
D73	PA_GPADC00	H24	CLDO4/3.3V	I/O	1.8V for ADC and 3.3V for GPIO
D74	PA_GPADC01	H25	CLDO4/3.3V	I/O	1.8V for ADC and 3.3V for GPIO
D75	DGND	/	DGND/0.0V	GND	
D76	PJ11_MII0-RXD3	N2	DCDC4/3.3V	I/O	
D77	PJ12_MII0-RXD2	P2	DCDC4/3.3V	I/O	
D78	PJ0_MII0-RXD1	P1	DCDC4/3.3V	I/O	
D79	PJ1_MII0-RXD0	N3	DCDC4/3.3V	I/O	
D80	PJ13_MII0-RXCK	T2	DCDC4/3.3V	I/O	
E01	DGND	/	DGND/0.0V	GND	
E02	DGND	/	DGND/0.0V	GND	
E03	DGND	/	DGND/0.0V	GND	
E04	DGND	/	DGND/0.0V	GND	
E05	DGND	/	DGND/0.0V	GND	
E06	DGND	/	DGND/0.0V	GND	
E07	DGND	/	DGND/0.0V	GND	
E08	DGND	/	DGND/0.0V	GND	
E09	DGND	/	DGND/0.0V	GND	
E10	DGND	/	DGND/0.0V	GND	
E11	DGND	/	DGND/0.0V	GND	
E12	DGND	/	DGND/0.0V	GND	
E13	DGND	/	DGND/0.0V	GND	

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E14	DGND	/	DGND/0.0V	GND	
E15	DGND	/	DGND/0.0V	GND	
E16	DGND	/	DGND/0.0V	GND	
E17	DGND	/	DGND/0.0V	GND	
E18	DGND	/	DGND/0.0V	GND	
E19	DGND	/	DGND/0.0V	GND	
E20	DGND	/	DGND/0.0V	GND	
E21	DGND	/	DGND/0.0V	GND	
E22	DGND	/	DGND/0.0V	GND	
E23	DGND	/	DGND/0.0V	GND	
E24	DGND	/	DGND/0.0V	GND	
E25	DGND	/	DGND/0.0V	GND	
E26	DGND	/	DGND/0.0V	GND	
E27	DGND	/	DGND/0.0V	GND	
E28	DGND	/	DGND/0.0V	GND	
E29	DGND	/	DGND/0.0V	GND	
E30	DGND	/	DGND/0.0V	GND	
E31	DGND	/	DGND/0.0V	GND	
E32	DGND	/	DGND/0.0V	GND	
E33	DGND	/	DGND/0.0V	GND	
E34	DGND	/	DGND/0.0V	GND	
E35	DGND	/	DGND/0.0V	GND	

Note:

- AI: analog input;
- AO: analog output;
- DI: digital input;
- DO: digital output;
- I/O: digital input and output;
- PWR: power supply;
- The unit of trace length is mil;
- For detailed LGA pin multiplexing functions, please refer to the "ECK32B_Pin_List" file.

4.3.3. I/O length control

The length of the internal wiring of the core board is shown in the table below, and

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the length unit is mil.

Main length control signal table

LGA	Pin Name	MPU	Function1	Function2	Length
B22	PCIE21-REFCLKN	A24	PCIE21-REFCLKN		1000.38
B21	PCIE21-REFCLKP	B24	PCIE21-REFCLKP		1000.01
B19	U3-PCIE21-RXN	A23	PCIE21-RXN		1021.3
B18	U3-PCIE21-RXP	B23	PCIE21-RXP		1021.47
B41	U3-PCIE21-TXN	A22	PCIE21-TXN		1009.71
B40	U3-PCIE21-TXP	B22	PCIE21-TXP		1011.23
C24	USB0-DM	B20	USB0-DM		525.85
C25	USB0-DP	A20	USB0-DP		525.91
C46	USB1-DM	B21	USB1-DM		365.21
C47	USB1-DP	A21	USB1-DP		366.87
D05	PD5_LCD_DSI-CKN	A3	DSI-CKN	LCD-D7	1211.52
D04	PD4_LCD_DSI-CKP	B3	DSI-CKP	LCD-D6	1213.4
D02	PD1_LCD_DSI-D0N	A5	DSI-D0N	LCD-D3	1225.8
D01	PD0_LCD_DSI-D0P	B5	DSI-D0P	LCD-D2	1223.97
D24	PD3_LCD_DSI-D1N	A4	DSI-D1N	LCD-D5	1228.63
D23	PD2_LCD_DSI-D1P	B4	DSI-D1P	LCD-D4	1230.41
D44	PD7_LCD_DSI-D2N	C2	DSI-D2N	LCD-D11	1251.41
D43	PD6_LCD_DSI-D2P	C1	DSI-D2P	LCD-D10	1253.28
D27	PD9_LCD_DSI-D3N	D2	DSI-D3N	LCD-D13	1235.29
D26	PD8_LCD_DSI-D3P	D1	DSI-D3P	LCD-D12	1235.41
D40	PD17_LCD_LV1-CKN	H2	LVDS1-CKN	LCD-D23	1429.06
D41	PD16_LCD_LV1-CKP	H1	LVDS1-CKP	LCD-D22	1428.69
C44	PD11_LCD_LV1-D0N	E2	LVDS1-D0N	LCD-D15	1344.23
C64	PD10_LCD_LV1-D0P	E1	LVDS1-D0P	LCD-D14	1344.47
C23	PD13_LCD_LV1-D1N	F2	LVDS1-D1N	LCD-D19	1434.99
C21	PD12_LCD_LV1-D1P	F1	LVDS1-D1P	LCD-D18	1436.86
C45	PD15_LCD_LV1-D2N	G2	LVDS1-D2N	LCD-D21	1408.48
C22	PD14_LCD_LV1-D2P	G1	LVDS1-D2P	LCD-D20	1407.99
C53	PD19_LCD_LV1-D3N	J2	LVDS1-D3N	LCD-DE	1417.94
C52	PD18_LCD_LV1-D3P	J1	LVDS1-D3P	LCD-CLK	1419.35
D58	PD20_LCD_HSYNC	K6		LCD-HSYNC	819.99
D59	PD21_LCD_VSYNC	H6		LCD-VSYNC	816.11
C61	PK4_LB_MIA-CKN	B12	MCSIA-CKN	LBUS-LD4	1068.11
C40	PK5_LB_MIA-CKP	A12	MCSIA-CKP	LBUS-LD5	1068.25
C42	PK0_LB_MIA-D0N	B13	MCSIA-D0N	LBUS-LD0	1116.38
C62	PK1_LB_MIA-D0P	A13	MCSIA-D0P	LBUS-LD1	1115.17
C41	PK2_LB_MIA-D1N	B11	MCSIA-D1N	LBUS-LD2	1074.07

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C79	PK3_LB_MIA-D1P	A11	MCSIA-D1P	LBUS-LD3	1074.92
C77	PK10_LB_MIB-CKN	B15	MCSIB-CKN	LBUS-LD10	1220.21
C59	PK11_LB_MIB-CKP	A15	MCSIB-CKP	LBUS-LD11	1220.22
C78	PK6_LB_MIB-D0N	B16	MCSIB-D0N	LBUS-LD6	1318.93
C60	PK7_LB_MIB-D0P	A16	MCSIB-D0P	LBUS-LD7	1320.11
C92	PK8_LB_MIB-D1N	B14	MCSIB-D1N	LBUS-LD8	1232.84
C39	PK9_LB_MIB-D1P	A14	MCSIB-D1P	LBUS-LD9	1234.82
C69	PK16_LB_MIC-CKN	B18	MCSIC-CKN	LBUS-LD16	1070
C70	PK17_LB_MIC-CKP	A18	MCSIC-CKP	LBUS-LD17	1071.65
C91	PK12_LB_MIC-D0N	B19	MCSIC-D0N	LBUS-LD12	1163.49
C76	PK13_LB_MIC-D0P	A19	MCSIC-D0P	LBUS-LD13	1161.67
C90	PK14_LB_MIC-D1N	B17	MCSIC-D1N	LBUS-LD14	1076.36
C75	PK15_LB_MIC-D1P	A17	MCSIC-D1P	LBUS-LD15	1078.19
C87	PK22_LB_MID-CKN	E17	MCSID-CKN	LBUS-LD22	1045.88
C88	PK23_LB_MID-CKP	D17	MCSID-CKP	LBUS-LD23	1047.69
C81	PK18_LB_MID-D0N	D19	MCSID-D0N	LBUS-LD18	1057.66
C82	PK19_LB_MID-D0P	E19	MCSID-D0P	LBUS-LD19	1056.15
C84	PK20_LB_MID-D1N	E15	MCSID-D1N	LBUS-LD20	1006.6
C83	PK21_LB_MID-D1P	D15	MCSID-D1P	LBUS-LD21	1007.75
C19	PE0_LB	B9		LBUS-CS0	891.89
C18	PE1_LB	G9		LBUS-CS1	880.47
C58	PE10_LB	D9		LBUS-ALE	702.54
C57	PE11_LB	C10		LBUS-BURST0	723.58
C56	PE12_LB	A10		LBUS-BURST1	704.45
C35	PE13_LB	C9		LBUS-BURST2	799.01
C93	PE14_LB	B10		LBUS-LCLK	918.94
C73	PE15_LB	H13		LBUS-INTR	697.63
C74	PE16_LB	G13		LBUS-DRQ	692.85
C36	PE17_LB	F13		LBUS-LBE	822.86
C17	PE2_LB	F9		LBUS-CS2	905.79
C16	PE3_LB	G11		LBUS-CS3	965.05
C15	PE4_LB	F11		LBUS-DP0	903.68
C14	PE5_LB	E11		LBUS-DP1	864.55
C13	PE6_LB	D13		LBUS-DP2	711.04
C12	PE7_LB	E13		LBUS-DP3	742.66
C37	PE8_LB	E9		LBUS-WR	814.14
C38	PE9_LB	D11		LBUS-READY	878.4
D34	PJ3_MII0-CLKIN	U3	RGMII0-CLKIN		1043.85
D35	PJ10_MII0-2550M	U2	RGMII0-EPHY-25/50M		1093.12
D54	PJ8_MII0-MDC	P5	RGMII0-MDC		1228.68
D53	PJ9_MII0-MDIO	K5	RGMII0-MDIO		1224.94

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D80	PJ13_MII0-RXCK	T2	RGMII0-RXCK		1116.81
D69	PJ2_MII0-RXCTL	P3	RGMII0-RXCTL		1154.27
D79	PJ1_MII0-RXD0	N3	RGMII0-RXD0		1103.19
D78	PJ0_MII0-RXD1	P1	RGMII0-RXD1		1122.55
D77	PJ12_MII0-RXD2	P2	RGMII0-RXD2		1111.79
D76	PJ11_MII0-RXD3	N2	RGMII0-RXD3		1101.07
D51	PJ6_MII0-TXCK	T7	RGMII0-TXCK		1287.53
D52	PJ7_MII0-TXCTL	T6	RGMII0-TXCTL		1255.22
D68	PJ5_MII0-TXD0	T3	RGMII0-TXD0		1243.91
D67	PJ4_MII0-TXD1	P4	RGMII0-TXD1		1237.13
D66	PJ15_MII0-TXD2	T5	RGMII0-TXD2		1237.13
D65	PJ14_MII0-TXD3	T4	RGMII0-TXD3		1230.52
D48	PJ19_MII1-CLKIN	L1	RGMII1-CLKIN		840.87
D49	PJ26_MII1-2550M	M5	RGMII1-EPHY-25/50M		922.82
D63	PJ24_MII1-MDC	K4	RGMII1-MDC		973.17
D62	PJ25_MII1-MDIO	K3	RGMII1-MDIO		989.53
D46	PJ29_MII1-RXCK	K2	RGMII1-RXCK		1067.17
D47	PJ18_MII1-RXCTL	M2	RGMII1-RXCTL		1049.01
D32	PJ17_MII1-RXD0	M3	RGMII1-RXD0		1101.09
D31	PJ16_MII1-RXD1	M1	RGMII1-RXD1		1123.79
D30	PJ28_MII1-RXD2	K1	RGMII1-RXD2		1055.26
D29	PJ27_MII1-RXD3	M4	RGMII1-RXD3		1055.63
D08	PJ22_MII1-TXCK	P7	RGMII1-TXCK		1135.2
D09	PJ23_MII1-TXCTL	P6	RGMII1-TXCTL		1156.71
D13	PJ21_MII1-TXD0	R2	RGMII1-TXD0		1176.28
D12	PJ20_MII1-TXD1	R3	RGMII1-TXD1		1170.76
D11	PJ31_MII1-TXD2	M6	RGMII1-TXD2		1204.79
D10	PJ30_MII1-TXD3	M7	RGMII1-TXD3		1166.77
B62	PF2_SDC0-CLK	AH22	SDC0-CLK		598.57
B60	PF3_SDC0-CMD	AG22	SDC0-CMD		613.88
B74	PF1_SDC0-D0	AG21	SDC0-D0		609.63
B73	PF0_SDC0-D1	AH21	SDC0-D1		611.9
B72	PF5_SDC0-D2	AH23	SDC0-D2		675.04
B71	PF4_SDC0-D3	AJ23	SDC0-D3		613.14
C32	PG0_SDC1-CLK	R29	SDC1-CLK		1259.49
C31	PG1_SDC1-CMD	T27	SDC1-CMD		1242.22
C10	PG2_SDC1-D1	R28	SDC1-D0		1296.82
C09	PG3_SDC1-D0	R27	SDC1-D1		1238.9
C08	PG4_SDC1-D2	U29	SDC1-D2		1254.86
C07	PG5_SDC1-D3	U28	SDC1-D3		1268.64

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4.3.4. I/O Impedance Control

All high-speed signals of the ECK33-B series core board have impedance control and length control during PCB design. The impedance control parameters of the core board traces are shown in the table below.

Trace impedance control table

Serial number	Impedance Controlled Routing Classification	Impedance Control	Typical Model Network Name
1	USB differential signaling	90±10%Ω	USB0-DP / USB0-DM
2	PCIe Differential Signaling	100±10%Ω	U3-PCIE21-DP/U3-PCIE21-DN
3	LVDS, MIPI differential signal	100±10%Ω	PD4_LCD_DSI-CKP /PD5_LCD_DSI-CKN
4	General single-ended routing	50±10%Ω	

4.4.Electrical Characteristics

4.4.1. Power consumption

Note: The following parameters are measured on the ECK33-B2N4E32-I core board on the ECB33-PGB2N4E32-I single-board computer at room temperature. The measured power consumption does not include the baseboard power consumption. The measurement was run on the eMMC with the Linux system, the stress-ng test program running when the power consumption was heavy, no display, no baseboard TF card access, and connected to a Gigabit network. Factors such as test methods, usage functions, and ambient temperature will affect power consumption. The following power consumption data is for reference only.

Power Consumption Table

Power Status	Test environment	Supply voltage	Current	Power consumption
BOOT	Uboot status, kernel not booted	5 V	161mA	805mW
PWRUP	After the system starts, no application is running	5 V	238mA	1190mW
PWRUP	Software reload testing	5 V	563mA	2815 mW
SLEEP	Freeze mode hibernation	5 V	177mA	885 mW
SLEEP	mem mode sleep state	5 V	14mA	70mW
PWRDN	Software shutdown	5 V	0 mA	0 mW

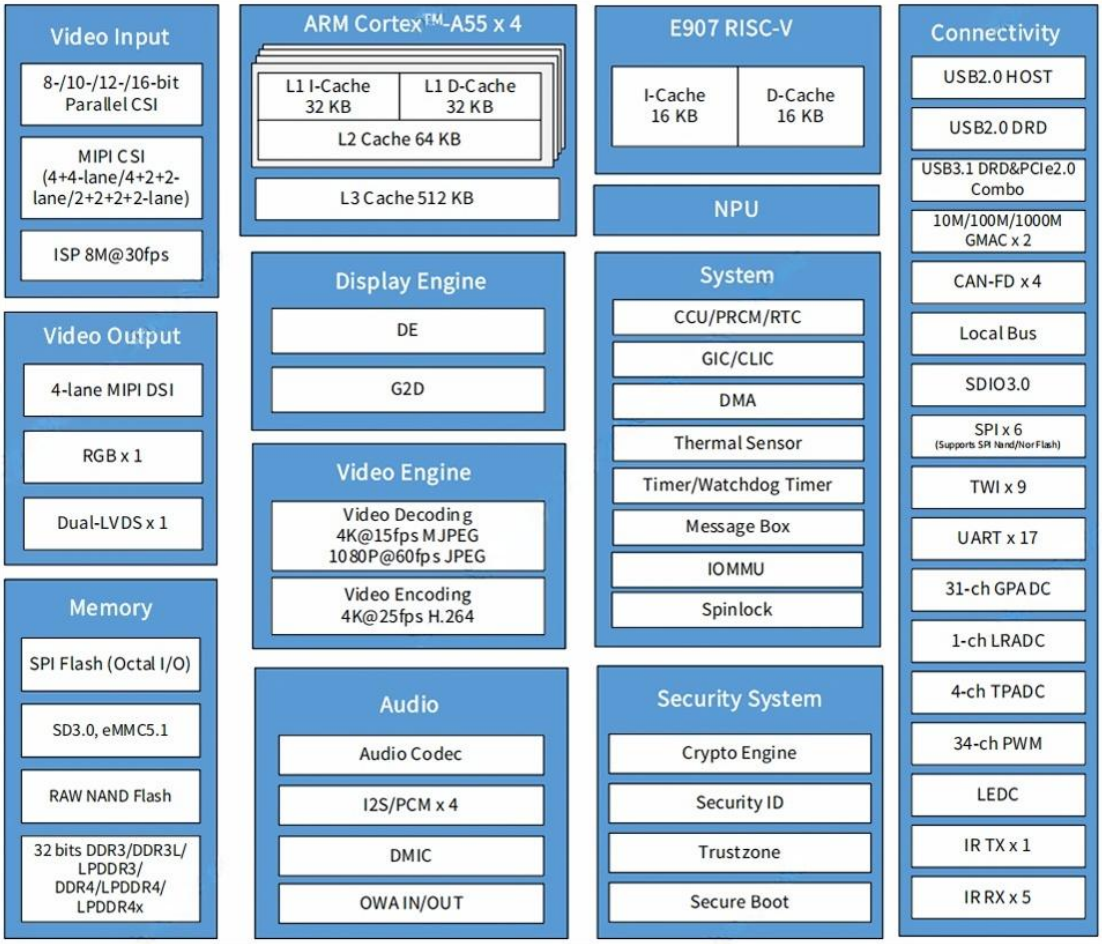
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5. Core board hardware design

5.1.processor

The Allwinner T536 series processor used in the ECK33-B series core board is a So C product with a high-performance quad-core Cortex-A55 AI platform, suitable for comme rcial, industrial and automotive fields. The functional block diagram of the T536 series pr ocessor is shown in the figure below.



T536 system functional block diagram

5.2.Memory

The ECK33-B series core board has one LPDDR4 SDRAM memory chip mounted on the board. It is designed with a 32-bit memory data width and currently provides 2GB/4 GB capacity options. The design memory can use domestic industrial-grade or domestic wi de-temperature devices. The memory chip models are shown in the table below.

Memory chip selection table

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factory	model	Single chip capacity	Operating temperature
YEESTOR	SGG1G32F5EI-S02	32Gbit	-40℃ ~ 95 ℃
YEESTOR	SGG512M32F5EI-S07	16Gbit	-40℃ ~ 95 ℃

Note: The specific model of the mounted memory chip shall be subject to the actual product.

5.3.clock

The ECK33-B series core board provides one 32.768KHz crystal (passive) oscillator circuit and one 24MHz crystal (passive) oscillator circuit as the processor system clock source. The crystal oscillator devices are all domestically produced industrial-grade crystal oscillators.

5.4.storage

The ECK33-B series core board has two storage media designed on the board. One is the eMMC storage medium. This storage medium has the characteristics of large storage capacity, low unit storage cost, fast read and write speed and easy use. The other storage medium is EEPROM, which is connected to the I2C bus. This storage medium has high reliability and is easy to use and can be used as user parameter storage. Both storage media are installed by default and do not need to be selected.

The eMMC memory of the ECK33-B series core board is connected to the processor through the SMHC2 (SDC2) bus, supports 150MHz HS400 mode, and the maximum read speed can reach 238MB/s. The device uses domestic industrial-grade eMMC storage chips.

The ECK33-B series core board EEPROM chip is connected to the processor through the TWI1 (I2C1) bus. The storage chip uses domestic industrial-grade EEPROM with a maximum capacity of 32Kbit.

The ECK33-B series core board storage chip models are shown in the table below.

Memory chip selection table

factory	model	capacity	Operating temperature
Longsys	FEMDRW032G-88A19	32GB	-40℃ ~ 85 ℃
Longsys	FEMDRW016G-88A43	16 GB	-40℃ ~ 85 ℃

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FMD	FT24C32A	32Kb	-40℃ ~ 85 ℃

Note: The specific model of the mounted memory chip shall be subject to the actual product.

5.5.power supply

The ECK33-B series core board adopts the original PMIC power solution and is desi gned in strict accordance with the voltage, power and timing requirements in the T536 ma nual. The selected PMIC solution chip models are: AXP717D and AXP323. The ECK33-B series core board is powered by a single DC +5V power supply. Only one VDD_IN_5V power input is required externally. Other power supplies are generated internally by the c ore board, and no additional power supply is required, which greatly simplifies the difficul ty of user power supply design.

The ECK33-B series core board also provides a power output VCC33-IO. This power supply is derived from the PMIC chip CLDO3, with a default operating voltage of 3.3V and a maximum output current of 300mA. It can be used to power low-power devices o n the baseboard and control the power-on timing of the baseboard I/O interface.

5.5.1. Core board power-on timing

The power supply and I/O interface of the ECK33-B series core board are roughly di vided into 6 stages :

Core board power supply and signal power-on timing table

Power-on stage	power supply	time
0	VDD_IN_5V , RTC	0ms
1	ALDO 4 , B LDO 2 , VCPUS , DCDC1, DCDC2, DCDC3	19 ms
2	CLDO1	21 ms
3	ALDO 3 , CLDO3	21 ms
4	RESET	56 ms
5	ALDO1, BLDO1, CLDO4, DCDC4	850 ms

the ECK33-B series core board is mainly divided into two stages. The first is the po wer supply that the core board PMIC automatically turns on after the 5V input power sup

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ply is valid (1, 2, 3); the second is the power supply that is turned off by default at pow er-on and configured to turn on after the software is started (5).

5.5.2. I/O power status when the core board is in sleep mode

When the ECK33-B series core board is in sleep mode, only the following power I/ Os are powered, so the core board can only be woken up through the GPIO on the PL.

I/O power status table when the core board is in sleep mode

power supply	Voltage	Typical I/O
RTC	1.8V	RESET、PWRON
ALDO3	3.3V	PL

5.6.On-board I/O assignment

Some functions on the ECK33-B series core board occupy the I/O functions of the T 536 processor. These I/O functions are not brought out to the LGA pins. Users should pa y attention to the function configuration of these I/Os when configuring the software. The specific occupied I/Os are shown in the following table.

Core board multiplexing I/O allocation table

MPU Pin	GPIO	Function
W27	PL0	PMU-SCK
Y28	PL1	PMU-SDA
V4	PC0	eMMC-DS
V3	PC1	eMMC-RST
V7	PC5	eMMC-CLK
V6	PC6	eMMC-CMD
V1	PC8	eMMC-D3
V2	PC9	eMMC-D4
W1	PC10	eMMC-D0
W2	PC11	eMMC-D5
Y1	PC13	eMMC-D1
Y2	PC14	eMMC-D6
AA1	PC15	eMMC-D2
AA2	PC16	eMMC-D7
E5	PH2	TWI1-SCK
D5	PH3	TWI1-SDA

6. Baseboard hardware design

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6.1.Power interface

For embedded product design, the design of the power supply system is crucial. It is necessary to consider not only the basic electrical parameters of the power supply itself, but also various factors such as the stability design and timing design of the power supply. The ECK33-B series core board has integrated complex power management and hardware circuits into the core board. The core board adopts a single power supply solution and provides power timing management signals to simplify the user's baseboard power supply design as much as possible.

6.1.1. Power Input

The ECK33-B series core board is powered by a single DC +5V power supply, and the power input pin is named VDD_IN_5V. The power supply voltage range is 5.0V±10%. The typical power consumption of the ECK33-B series core board is about 3W. When designing the power supply for the core board, the baseboard should consider the I/O output power consumption and the increased power consumption when more functions are running at the same time, and the increased power consumption of components at high temperatures. Therefore, it is recommended that the core board power supply current design should not be less than 1A.

The core board is powered by a DC-DC power supply, and the power margin should not be too large when designing the power supply. If the power design is too large, many power supplies will work in discontinuous PWM mode to ensure conversion efficiency, and the output power ripple will increase significantly, which is not conducive to the working stability of the digital signal system.

6.1.2. Power Output

The ECK33-B series core board also provides a power output pin named VCC33-IO, which can be used to power low-power devices on the baseboard or control the power-on timing of the baseboard I/O interface.

6.1.3. Backplane Power Sequencing

The power timing control of the baseboard mainly considers the power-on timing of t

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he core board I/O. The I/O interface of the ECK33-B series core board is mainly divided into two stages of power-on. The first stage is that the core board PMIC automatically turns on the power after the 5V input power is effective; the second stage is that the PMIC is turned off by default and the power is turned on after the software is started.

To ensure that the baseboard does not cause leakage current to the core board I/O interface, a simple way is to power on all I/O interface power supplies connected to the baseboard and the core board after the core board I/O is powered on (that is, after the core board software configuration turns on all I/O power supplies). You can use the core board's I/O that uses software-controlled power (for example, PD14 is powered by DCDC4, and the power supply of each I/O port can be queried in the pin list) to control the power supply of the baseboard I/O interface.

For I/O interfaces that need to be powered on before software works (such as SD card interface and debug serial port), if the power is small, you can directly use the VCC33-IO power supply. If the power is large, you can use the power supply controlled by VCC33-IO.

6.2.Launch Configuration

6.2.1. Boot order configuration

When the ECK33-B series core board starts, the processor will read the status of BOOT_Select and select the order of enumerating the media. BOOT_Select has a fixed configuration status on the core board, and the default startup order is: SMHC0->EMMC_BOOT->EMMC_USER->try (except SPI2)

6.2.2. FEL pin

The ECK33-B series core board supports the firmware forced burning pin FEL. When the ECK33-B series core board is not powered on, the FEL signal is grounded. After powering on, FEL is released, and the ECK33-B series core board will enter the firmware upgrade mode. Users can design buttons or jumpers on the baseboard to ground the FEL signal to force the processor to enter the firmware upgrade mode. Since the signal has been designed with a pull-up resistor on the core board, the baseboard design only needs to consider grounding and appropriate TVS protection. Do not arbitrarily design a pull-up resis

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tor for the FEL signal on the baseboard. If the FEL signal is not used, the signal can be left floating and the firmware can be upgraded through the SD card.

6.2.3. Pin Definition

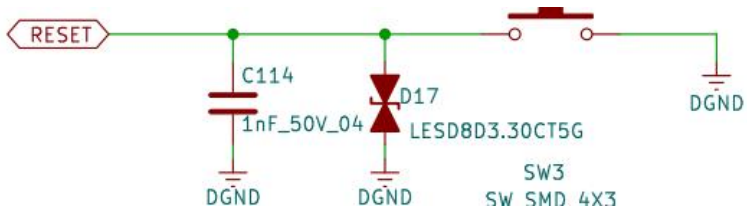
Startup configuration pin definition table

LGA	Pin Name	MPU	Power Rail	Type	Length	Comment
C 27	FEL	AD21	CLDO3/3.3V	DI		1nF pull down, 100Ω in series

6.3.Reset button

The RESET signal from the ECK33-B series core board can be connected to an external button to achieve reset control of the processor. The RESET signal is an input-output bidirectional signal. It can be used as an external reset input to reset the processor. It is also the internal power reset signal output of the processor. The RESET signal provides a 10K ohm pull-up resistor in the core board. Therefore, in the baseboard application, when the RESET signal is used as a manual reset input, do not connect the pull-up resistor, directly connect the button, or drive it through the OD gate. Do not drive the RESET signal through the push-pull output interface. When connecting the manual input button, you can place a small capacitor (capacitance value not greater than 1nF) and TVS to reduce interference and improve ESD performance. The button reference schematic is shown in the figure below.

6.3.1. References



Button reference schematic

Note: Do not pull up the reset and power button signals through resistors at will. If the pull-up power rail is incorrect, it will cause uncertain signals to be input to the button signal interface when the system is in standby or shutdown.

6.3.2. Pin Definition

Button pin definition table

LGA	Pin Name	MPU	Power Rail	Type	Length	Comment

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C04	AP-RESET	AF27	RTC/1.8V	I/O		1nF pull down,100Ω in series,10KΩ pull up

6.3.3. LAYOUT SUGGESTIONS

- The reset signal is a sensitive signal and can be processed in a package or away from signals with greater interference ;
- Place the reset signal TVS tube as close to the button as possible.

6.4.Reference Clock and NMI

The ECK33-B series core board provides two clock output signals. One is 24MHz cl ock output AP-CK24M-OUT, and the other is 32.768KHz clock output AP-CK32K-OUT. B oth clock outputs can be used for Wi-Fi modules.

6.4.1. NMI

Processor non-maskable interrupt signal, mainly used for PMIC management. This pin function is not recommended for users to use. It can be left floating when not in use.

6.4.2. Pin Definition

Button pin definition table

LGA	Pin Name	MPU	Power Rail	Type	Length	Comment
A14	AP-CK24M-OUT	AH28	ALDO4/1.8V	A14		
A15	AP-CK32K-OUT	AF28	RTC/1.8V	A15		10KΩ pull up
C28	AP-NMI	AE28	RTC/1.8V	C28		1nF pull down, 10KΩ pull up

6.5.Display interface

The ECK33-B series core board supports three types of LCD screen interfaces: RGB, LVDS, and MIPI-DSI. When designing a product, please select the corresponding interfac e according to the specific LCD specifications.

Interface information table of each display screen

LCD Interface	Maximum supported resolution
Single-Link LVDS	1366x768@60Hz
Dual-Link LVDS	1920x1080@60Hz
Single-Link MIPI DSI	1920x1 200 @60Hz
RGB	1920x1 200 @60Hz

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- When the PD port is used as a normal GPIO, the LVDS and MIPI DSI modules need to be turned off. Otherwise, the LVDS/MIPI-DSI and GPIO will be output together, affecting the GPIO output level.
- Make sure that the MIPI or LVDS interface signal differential pairs on the core board and LCD are correctly connected, and the positive and negative terminals cannot be reversed.
- The LCD backlight IC needs to be designed according to the specific LCD specifications. PWM dimming is used by default. When using PWM dimming, please note that the PWM frequency must be greater than 20KHz, otherwise the inductor will howl. It is recommended to adjust the PWM frequency to 30KHz ~ 50KHz according to the specifications of the backlight IC.
- Please confirm whether the IO voltage of LCD is consistent with the control IO voltage of core board . If not, please make sure to do level matching, such as LCD-RST signal.
- The length of the MIPI DSI differential line should be less than 2000 mil, and the reference plane of the line should be kept intact as much as possible.
- The LCD display interface recommends using the 18-bit color signal on the PD pin. These signals are all on a set of I/Os, which is convenient for controlling the trace length and operating level. When the PD pin is configured as LVDS or DSI function, it automatically switches to 1.8V level. When configured as GPIO or LCD function, it automatically switches to 3.3V level.

6.5.1. Interface Definition

LCD/LVDSDSI Interface Definition Table

LGA	Name	MPU	Power Rail	Type	Length	Comment
D01	PD0_LCD_DSI-D0P	B5	DCDC4/3.3V	I/O	1223.97	LCD-D2/LVDS0-D0P/DSI-D0P
D02	PD1_LCD_DSI-D0N	A5	DCDC4/3.3V	I/O	1225.8	LCD-D3/LVDS0-D0N/DSI-D0N
D23	PD2_LCD_DSI-D1P	B4	DCDC4/3.3V	I/O	1230.41	LCD-D4/LVDS0-D1P/DSI-D1P
D24	PD3_LCD_DSI-D1N	A4	DCDC4/3.3V	I/O	1228.63	LCD-D5/LVDS0-D1N/DSI-D1N
D04	PD4_LCD_DSI-CKP	B3	DCDC4/3.3V	I/O	1213.4	LCD-D6/LVDS0-D2P/DSI-CKP
D05	PD5_LCD_DSI-CKN	A3	DCDC4/3.3V	I/O	1211.52	LCD-D7/LVDS0-D2N/DSI-CKN
D43	PD6_LCD_DSI-D2P	C1	DCDC4/3.3V	I/O	1253.28	LCD-D10/LVDS0-CKP/DSI-D2P
D44	PD7_LCD_DSI-D2N	C2	DCDC4/3.3V	I/O	1251.41	LCD-D11/LVDS0-CKN/DSI-D2N

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D26	PD8_LCD_DSI-D3P	D1	DCDC4/3.3V	I/O	1235.41	LCD-D12/LVDS0-D3P/DSI-D3P
D27	PD9_LCD_DSI-D3N	D2	DCDC4/3.3V	I/O	1235.29	LCD-D13/LVDS0-D3N/DSI-D3N
C64	PD10_LCD_LV1-D0P	E1	DCDC4/3.3V	I/O	1344.47	LCD-D14/LVDS1-D0P
C44	PD11_LCD_LV1-D0N	E2	DCDC4/3.3V	I/O	1344.23	LCD-D15/LVDS1-D0N
C21	PD12_LCD_LV1-D1P	F1	DCDC4/3.3V	I/O	1436.86	LCD-D18/LVDS1-D1P
C23	PD13_LCD_LV1-D1N	F2	DCDC4/3.3V	I/O	1434.99	LCD-D19/LVDS1-D1N
C22	PD14_LCD_LV1-D2P	G1	DCDC4/3.3V	I/O	1407.99	LCD-D20/LVDS1-D2P
C45	PD15_LCD_LV1-D2N	G2	DCDC4/3.3V	I/O	1408.48	LCD-D21/LVDS1-D2N
D41	PD16_LCD_LV1-CKP	H1	DCDC4/3.3V	I/O	1428.69	LCD-D22/LVDS1-CKP
D40	PD17_LCD_LV1-CKN	H2	DCDC4/3.3V	I/O	1429.06	LCD-D23/LVDS1-CKN
C52	PD18_LCD_LV1-D3P	J1	DCDC4/3.3V	I/O	1419.35	LCD-CLK/LVDS1-D3P
C53	PD19_LCD_LV1-D3N	J2	DCDC4/3.3V	I/O	1417.94	LCD-DE/LVDS1-D3N
D58	PD20_LCD_HSYNC	K6	DCDC4/3.3V	I/O	819.99	LCD-HSYNC
D59	PD21_LCD_VSYNC	H6	DCDC4/3.3V	I/O	816.11	LCD-VSYNC
D01	PD0_LCD_DSI-D0P	B5	DCDC4/3.3V	I/O	1223.97	LCD-D2/LVDS0-D0P/DSI-D0P
D02	PD1_LCD_DSI-D0N	A5	DCDC4/3.3V	I/O	1225.8	LCD-D3/LVDS0-D0N/DSI-D0N

6.5.2. LAYOUT SUGGESTIONS

- LCD signal routing should be of equal length, with the length within the group contr olled within 500mil and single-ended impedance of 50 ohms. Pay attention to the cro sstalk of LCD clock signal and keep a certain distance from other signals.
- The single-ended impedance of the LVDS signal is 50 ohms, the differential impedan ce is 100 ohms, the line length difference within the differential pair is less than 10 mil, and the line length difference within the group is less than 100 mil;
- The single-ended impedance of the MIPI DSI signal is 50 ohms, the differential impe dance is 100 ohms, the line length difference within the differential pair is less than 10 mil, and the line length difference within the group is less than 100 mil;
- The reference plane for the displayed signal routing should be complete, the routing s hould not cross the division , and the signal line spacing should be at least 2W.

6.6.Camera interface

The ECK33-B series core board supports four MIPI-CSI interfaces. When designing t he hardware, in order to facilitate PCB The layout design can swap the correspondence be tween the A and B channels and the front and rear cameras, but the relevant software ada ptation is required at the same time. MCSIA and MCSIB, MCSIC and MCSID can be co

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mbined into 4 lane is used, MCSIA and MCSIB are used as 4 When the lane is connecte d, the CLK of MCSIA needs to be used. The CLK of MCSIB can be left floating or use d as a normal IO. MCSIA0, MCSIA1, MCSIB0, and MCSIB1 correspond to MCSI0/1/2/3 respectively; MCSIC and MCSID are used as 4 When using lane, the CLK of MCSIC n eeds to be used, and the CLK of MCSID can be left floating or used as a normal IO. M CSIC0, MCSIC1, MCSID0, and MCSID1 correspond to MCSI0/1/2/3 respectively.

6.6.1. Interface Definition

MCSI interface definition table

LGA	Pin Name	MPU	Power Rail	Type	Length	Comment
C61	PK4_LB_MIA-CKN	B12	DCDC4/3.3V	I/O	1068.11	MCSIA-CKN
C40	PK5_LB_MIA-CKP	A12	DCDC4/3.3V	I/O	1068.25	MCSIA-CKP
C42	PK0_LB_MIA-D0N	B13	DCDC4/3.3V	I/O	1116.38	MCSIA-D0N
C62	PK1_LB_MIA-D0P	A13	DCDC4/3.3V	I/O	1115.17	MCSIA-D0P
C41	PK2_LB_MIA-D1N	B11	DCDC4/3.3V	I/O	1074.07	MCSIA-D1N
C79	PK3_LB_MIA-D1P	A11	DCDC4/3.3V	I/O	1074.92	MCSIA-D1P
C77	PK10_LB_MIB-CKN	B15	DCDC4/3.3V	I/O	1220.21	MCSIB-CKN
C59	PK11_LB_MIB-CKP	A15	DCDC4/3.3V	I/O	1220.22	MCSIB-CKP
C78	PK6_LB_MIB-D0N	B16	DCDC4/3.3V	I/O	1318.93	MCSIB-D0N
C60	PK7_LB_MIB-D0P	A16	DCDC4/3.3V	I/O	1320.11	MCSIB-D0P
C92	PK8_LB_MIB-D1N	B14	DCDC4/3.3V	I/O	1232.84	MCSIB-D1N
C39	PK9_LB_MIB-D1P	A14	DCDC4/3.3V	I/O	1234.82	MCSIB-D1P
C69	PK16_LB_MIC-CKN	B18	DCDC4/3.3V	I/O	1070	MCSIC-CKN
C70	PK17_LB_MIC-CKP	A18	DCDC4/3.3V	I/O	1071.65	MCSIC-CKP
C91	PK12_LB_MIC-D0N	B19	DCDC4/3.3V	I/O	1163.49	MCSIC-D0N
C76	PK13_LB_MIC-D0P	A19	DCDC4/3.3V	I/O	1161.67	MCSIC-D0P
C90	PK14_LB_MIC-D1N	B17	DCDC4/3.3V	I/O	1076.36	MCSIC-D1N
C75	PK15_LB_MIC-D1P	A17	DCDC4/3.3V	I/O	1078.19	MCSIC-D1P
C87	PK22_LB_MID-CKN	E17	DCDC4/3.3V	I/O	1045.88	MCSID-CKN
C88	PK23_LB_MID-CKP	D17	DCDC4/3.3V	I/O	1047.69	MCSID-CKP
C81	PK18_LB_MID-D0N	D19	DCDC4/3.3V	I/O	1057.66	MCSID-D0N
C82	PK19_LB_MID-D0P	E19	DCDC4/3.3V	I/O	1056.15	MCSID-D0P
C84	PK20_LB_MID-D1N	E15	DCDC4/3.3V	I/O	1006.6	MCSID-D1N
C83	PK21_LB_MID-D1P	D15	DCDC4/3.3V	I/O	1007.75	MCSID-D1P

6.6.2. LAYOUT SUGGESTIONS

- The differential impedance of MIPI-CSI signals is 100 ohms, the difference in the len gth of the traces within the differential pair is less than 10 mil, and the difference in

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the length of the traces within the group is less than 300 mil;

- The NCSI signal routing should be of equal length. The length within the group can be controlled within 500mil, and the single-ended impedance is 50 ohms. Pay attention to the crosstalk of the clock signal and keep a certain distance from other signals.
- The length of the MIPI CSI differential line should be less than 3000 mil, and the reference plane of the line should be kept intact as much as possible.

6.7.PCIe interface

The ECK33-B series core board supports a set of PCIE2.1 x1 lane, 5Gbps/lane, multiplexed with USB3.1 interface IO, supports RC mode, supports dual virtual channels, 8 inbound windows and 8 outbound windows and message signaled interrupts.

Note that PCIE21-PERSTN/PCIE21-WAKEN/PCIE21-CLKREQN must use functional pins and cannot be simulated with GPIO.

A 100nF capacitor needs to be connected in series on the PCIE interface TXP/N and REFCLKP/N. When using PCIE as an inter-board connection, please place this capacitor close to the PCIE connector on the transmitting end; when using PCIE as an intra-board CHIP TO CHIP interconnection, please place this capacitor close to the transmitting end device. When the PCIE interface is not used, it is recommended to ground the PCIE-CLKP/N signal, and other signals can be floating.

6.7.1. Pin Definition

PCIe Interface Definition Table

LGA	Pin Name	MPU	Power Rail	Type	Length	Comment
B22	PCIE21-REFCLKN	A24	CLDO1/1.8V	AI/O	1000.38	PCIE21-REFCLKN
B21	PCIE21-REFCLKP	B24	CLDO1/1.8V	AI/O	1000.01	PCIE21-REFCLKP
B19	U3-PCIE21-RXN	A23	CLDO1/1.8V	AI	1021.3	PCIE21-RXN
B18	U3-PCIE21-RXP	B23	CLDO1/1.8V	AI	1021.47	PCIE21-RXP
B41	U3-PCIE21-TXN	A22	CLDO1/1.8V	AO	1009.71	PCIE21-TXN
B40	U3-PCIE21-TXP	B22	CLDO1/1.8V	AO	1011.23	PCIE21-TXP

6.7.2. LAYOUT SUGGESTIONS

- The PCIe signal differential impedance is 100 ohms, the line length difference within the differential pair is less than 10 mil, and there is no special requirement for the

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line length difference within the group;

- PCIe signal routing should reduce the number of via layer switching, the signal routing length should be controlled within 5000Mil, and the routing should avoid crossing plane layer splits.

6.8.SD/MMC card interface

The ECK33-B series core board is equipped with 3 SMHC (SD/MM host controller) controllers, including SMHC0, SMHC1, and SMHC2. SMHC0 complies with the Secure Digital Memory v3.0 protocol and is usually used to connect to SD cards. SMHC1 complies with the Secure Digital I/O v3.0 protocol and is usually used to connect to extended functions, such as Wi-Fi modules. SMHC2 complies with the Multimedia Card v5.0 protocol and is usually used to connect to eMMC storage chips. The ECK33-B series core uses SMHC2 to expand the on-board eMMC storage chip. It is recommended that the baseboard use SMHC0 to connect to the SD card. SMHC1 is recommended to expand other devices or not be used.

The SDC-CLK pin does not require a pull-up resistor. A 33-ohm resistor has been connected in series on the core board near the SoC end to reduce radiation interference on the CLK.

GPIO ports PF3 and PF6 have pull-up resistors inside the SoC (about 15K, which needs to be enabled in software). When designing the external SDC0-CMD and SDC0-DET circuits, cost-down can be done to eliminate the need for external pull-up design.

The ECK33-B series core board supports the SD3.0 protocol, and will automatically identify the type of Micro SD card and adjust the IO voltage. If the Micro SD card is an SD3.0 memory card, the core board will work in SD3.0 mode, the IO voltage will switch from 3.3V to 1.8V, and the PF port IO power supply will automatically switch inside the SoC .

The SD interface signal line is a high-speed signal line. If the SD3.0 mode is used, the parasitic capacitance of the TVS tube connected in parallel on the signal line is required to be ≤5pF. If only the SD2.0 mode is used, the parasitic capacitance of the TVS tube is required to be <35pF, otherwise it will affect the data transmission quality .

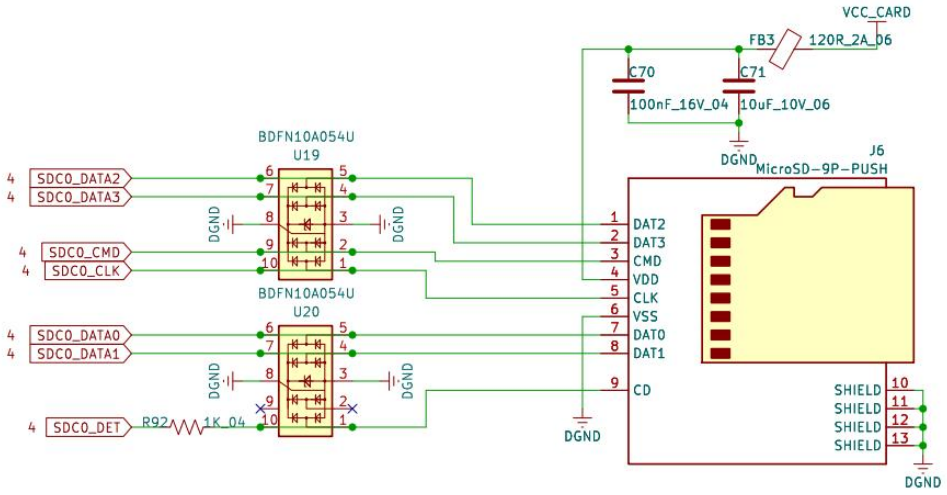
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It is recommended to keep the series resistor on the DET signal line to avoid signal undershoot when the Micro SD card is inserted, which affects the signal quality and impr oves the ESD performance of the IO signal.

To expand the Micro SD card through the SMHC0 interface, please refer to the follo wing schematic design.

6.8.1. References



SD card reference circuit diagram

6.8.2. Pin Definition

SMHC interface signal pin definition

LGA	Pin Name	MPU	Power Rail	Type	Length	Comment
B62	PF2_SDC0-CLK	AH22	CLDO3/3.3V	I/O	598.57	SDC0-CLK
B60	PF3_SDC0-CMD	AG22	CLDO3/3.3V	I/O	613.88	SDC0-CMD
B73	PF0_SDC0-D1	AH21	CLDO3/3.3V	I/O	611.9	SDC0-D1
B74	PF1_SDC0-D0	AG21	CLDO3/3.3V	I/O	609.63	SDC0-D0
B72	PF5_SDC0-D2	AH23	CLDO3/3.3V	I/O	675.04	SDC0-D2
B71	PF4_SDC0-D3	AJ23	CLDO3/3.3V	I/O	613.14	SDC0-D3
C32	PG0_SDC1-CLK	R29	BLDO1/3.3V	I/O	1259.49	SDC1-CLK
C31	PG1_SDC1-CMD	T27	BLDO1/3.3V	I/O	1242.22	SDC1-CMD
C10	PG2_SDC1-D0	R28	BLDO1/3.3V	I/O	1296.82	SDC1-D0
C09	PG3_SDC1-D1	R27	BLDO1/3.3V	I/O	1238.9	SDC1-D1
C08	PG4_SDC1-D2	U29	BLDO1/3.3V	I/O	1254.86	SDC1-D2
C07	PG5_SDC1-D3	U28	BLDO1/3.3V	I/O	1268.64	SDC1-D3

6.8.3. LAYOUT SUGGESTIONS

❖ SMHC signal is controlled according to the single-ended 50 ohm impedance, and the

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bottom board impedance control is recommended to be consistent;

- ❖ the SMHC signal base plate group is controlled within 150Mil;
- ❖ Insert a 1K ohm resistor in series with the detection signal to improve ESD performance;
- ❖ The distance between the clock signal and other signals follows the 3W rule.

6.9.USB interface

The ECK33-B series core board has three USB interfaces: USB0, USB1 and USB2. Here, '0 1 2' refers to the USB serial number, and '2.0' and '3.1' refer to the USB standard version. The USB0 and USB1 of the core board are USB 2.0 interfaces, and USB2 is a USB 3.1 interface. Note that the USB2.0 signal of USB2 shares the PHY with USB1, while the USB 3.1 signal of USB2 shares the 1 lane combo PHY with PCI. Therefore, the core board supports up to 2 USB2.0 interfaces at the same time, and the PCIe and USB3.1 SS interfaces cannot be used at the same time.

USB0 and USB2 support OTG function, USB1 only supports HOST function. Program burning can only be performed through USB0.

When using USB2, the USB1 interface is multiplexed as the USB 2.0 interface of USB2, so USB1 and USB2 cannot be used at the same time.

USB2.0 supports the following rates: HS, 480Mbit/s, FS, 12Mbit/s, LS, 1.5Mbit/s; USB3.1 supports the following rates: SS, 5Gbit/s, HS, 480Mbit/s, FS, 12Mbit/s. It is not recommended to use the data rate close to the maximum value during design.

USB interface information table

USB interface	Controller	Transmission speed level
USB0	USB2.0 OTG	HighSpeed, 480Mbps
USB1	USB2.0 Host	HighSpeed, 480Mbps
USB2	USB3.1 OTG	HighSpeed, 480Mbps
		SuperSpeed, 5Gbps

USB0 supports OTG function. When the firmware image is burned, the SoC defaults to Device. After the system is powered on, the system combines the level status of USB0-ID pin and USB0-VBUSDET pin to realize the status detection of USB0 as Host/Device. USB0-ID and USB0-VBUSDET pins can be replaced by other GPIOs.

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The PCIe2.1 controller and USB3.1 share the same PHY, and only one of them can be used at the same time. No matter whether you choose PCIe2.1 or USB3.0. When using USB3.0 instead of PCIe2.1, the PCIE-REF-CLKP and PCIE-REF-CLKN in the PCIe2.1 signal need to be grounded.

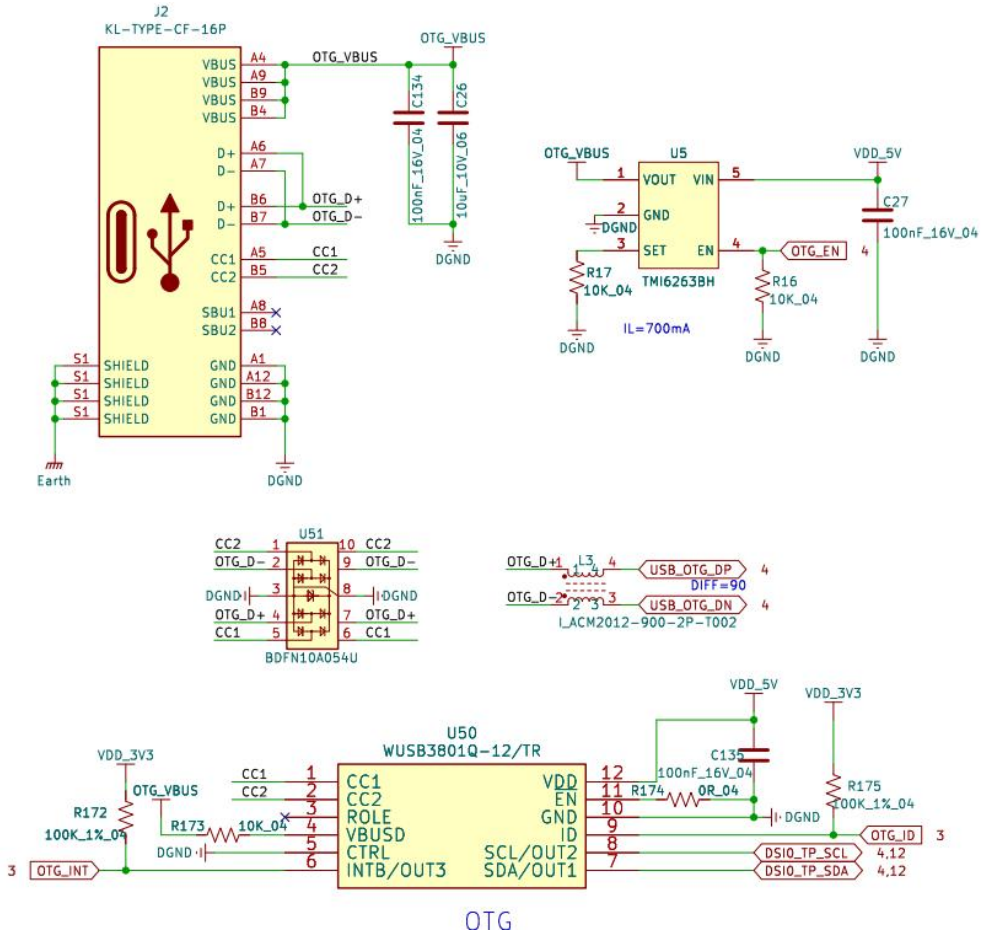
USB2.0 interface DM/DP and USB3.0 interface TX/RX signal lines need TVS protection. USB2.0 interface recommends that the parasitic capacitance of TVS device should be less than 2pF, USB3.0 interface requires that the parasitic capacitance of TVS tube connected to ground should be less than 0.5pF, and the clamping voltage capability should be as strong as possible, and the recommended clamping voltage should be less than 10V@8KV (IEC61000-4-2).

When TVS protection is used for the DM/DP signals of the USB OTG interface, it is recommended that the TVS should not be connected to the VBUS power supply of the OTG interface, because the power supply may be in the off state, which not only cannot provide effective ESD protection, but may also introduce interference.

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6.9.1. OTG interface reference circuit



OTG interface reference circuit diagram

6.9.2. Pin Definition

USB interface signal pin definition

LGA	Pin Name	MPU	Power Rail	Type	Length	Comment
B19	U3-PCIE21-RXN	A23	CLDO1/1.8V	AI	1021.3	USB2-U3-RXN
B18	U3-PCIE21-RXP	B23	CLDO1/1.8V	AI	1021.47	USB2-U3-RXP
B41	U3-PCIE21-TXN	A22	CLDO1/1.8V	AO	1009.71	USB2-U3-TXN
B40	U3-PCIE21-TXP	B22	CLDO1/1.8V	AO	1011.23	USB2-U3-TXP
C24	USB0-DM	B20	CLDO3/3.3V	AI/O	525.85	USB0-DM
C25	USB0-DP	A20	CLDO3/3.3V	AI/O	525.91	USB0-DP
C46	USB1-DM	B21	CLDO3/3.3V	AI/O	365.21	USB1-DM
C47	USB1-DP	A21	CLDO3/3.3V	AI/O	366.87	USB1-DP

6.9.3. LAYOUT SUGGESTIONS

❖ The USB signal routing is controlled to be of equal length , the error within the diff

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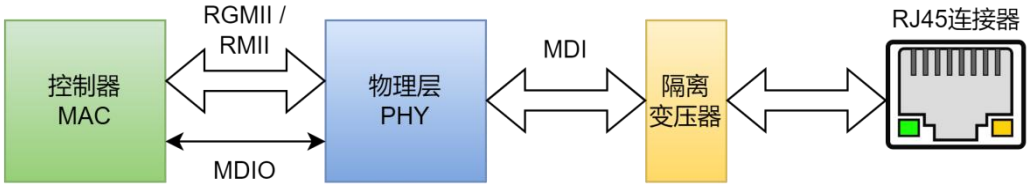
erential pair is no more than 50M il, and the spacing between adjacent differential pa irs is more than 3W;

- ❖ The differential impedance of the USB signal is controlled at 90 ohms ;
- ❖ The length of USB signal trace is less than 6000Mil .

6.10.Ethernet interface

The ECK33-B series core board supports 2 -way 10M/100M /1000M adaptive Etherne t controller . The Ethernet controller supports RGMII and RMII interfaces .

Usually an RJ45 Ethernet interface is mainly composed of an Ethernet controller MA C (Media Access Control), an Ethernet physical layer interface PHY (Physical Layer), an Ethernet transformer, and an RJ45 connector, as shown in the figure below.



RJ45 Ethernet components

The ECK33-B series core board does not have an Ethernet PHY circuit designed in i t. If the user uses the Ethernet function, the PHY interface chip circuit needs to be desig ned on the baseboard. The baseboard PHY interface chip circuit design can refer to the E byte single-board computer product drawings.

6.10.1. Pin Definition

Ethernet interface signal pin definition

LGA	Name	MPU	Power Rail	Type	Length	Comment
D79	PJ1_MII0-RXD0	N3	DCDC4/3.3V	I/O	1103.19	RGMII0-RXD0
D78	PJ0_MII0-RXD1	P1	DCDC4/3.3V	I/O	1122.55	RGMII0-RXD1
D77	PJ12_MII0-RXD2	P2	DCDC4/3.3V	I/O	1111.79	RGMII0-RXD2
D76	PJ11_MII0-RXD3	N2	DCDC4/3.3V	I/O	1101.07	RGMII0-RXD3
D69	PJ2_MII0-RXCTL	P3	DCDC4/3.3V	I/O	1154.27	RGMII0-RXCTL
D80	PJ13_MII0-RXCK	T2	DCDC4/3.3V	I/O	1116.81	RGMII0-RXCK
D68	PJ5_MII0-TXD0	T3	DCDC4/3.3V	I/O	1243.91	RGMII0-TXD0
D67	PJ4_MII0-TXD1	P4	DCDC4/3.3V	I/O	1237.13	RGMII0-TXD1
D66	PJ15_MII0-TXD2	T5	DCDC4/3.3V	I/O	1237.13	RGMII0-TXD2

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D65	PJ14_MII0-TXD3	T4	DCDC4/3.3V	I/O	1230.52	RGMII0-TXD3
D52	PJ7_MII0-TXCTL	T6	DCDC4/3.3V	I/O	1255.22	RGMII0-TXCTL
D51	PJ6_MII0-TXCK	T7	DCDC4/3.3V	I/O	1287.53	RGMII0-TXCK
D54	PJ8_MII0-MDC	P5	DCDC4/3.3V	I/O	1228.68	RGMII0-MDC
D53	PJ9_MII0-MDIO	K5	DCDC4/3.3V	I/O	1224.94	RGMII0-MDIO
D35	PJ10_MII0-2550M	U2	DCDC4/3.3V	I/O	1093.12	RGMII0-EPHY-25/50M
D34	PJ3_MII0-CLKIN	U3	DCDC4/3.3V	I/O	1043.85	RGMII0-CLKIN
D32	PJ17_MII1-RXD0	M3	DCDC4/3.3V	I/O	1101.09	RGMII1-RXD0
D31	PJ16_MII1-RXD1	M1	DCDC4/3.3V	I/O	1123.79	RGMII1-RXD1
D30	PJ28_MII1-RXD2	K1	DCDC4/3.3V	I/O	1055.26	RGMII1-RXD2
D29	PJ27_MII1-RXD3	M4	DCDC4/3.3V	I/O	1055.63	RGMII1-RXD3
D47	PJ18_MII1-RXCTL	M2	DCDC4/3.3V	I/O	1049.01	RGMII1-RXCTL
D46	PJ29_MII1-RXCK	K2	DCDC4/3.3V	I/O	1067.17	RGMII1-RXCK
D13	PJ21_MII1-TXD0	R2	DCDC4/3.3V	I/O	1176.28	RGMII1-TXD0
D12	PJ20_MII1-TXD1	R3	DCDC4/3.3V	I/O	1170.76	RGMII1-TXD1
D11	PJ31_MII1-TXD2	M6	DCDC4/3.3V	I/O	1204.79	RGMII1-TXD2
D10	PJ30_MII1-TXD3	M7	DCDC4/3.3V	I/O	1166.77	RGMII1-TXD3
D09	PJ23_MII1-TXCTL	P6	DCDC4/3.3V	I/O	1156.71	RGMII1-TXCTL
D08	PJ22_MII1-TXCK	P7	DCDC4/3.3V	I/O	1135.2	RGMII1-TXCK
D63	PJ24_MII1-MDC	K4	DCDC4/3.3V	I/O	973.17	RGMII1-MDC
D62	PJ25_MII1-MDIO	K3	DCDC4/3.3V	I/O	989.53	RGMII1-MDIO
D49	PJ26_MII1-2550M	M5	DCDC4/3.3V	I/O	922.82	RGMII1-EPHY-25/50M
D48	PJ19_MII1-CLKIN	L1	DCDC4/3.3V	I/O	840.87	RGMII1-CLKIN

6.10.2. LAYOUT SUGGESTIONS

- RGMII signal sending and receiving packets are controlled to be equal length, with a n error of 100M il and a line spacing of more than 2W;
- The network differential signal is controlled to be equal length, the error within the d ifferential pair is 10 mil , and the spacing between adjacent differential pairs is more than 3W;
- The network port transformer should be placed close to the PHY chip, and the recom mended distance is no more than 20 mm.
- The decoupling capacitor of the power pin of the PHY chip is placed close to the P HY chip .

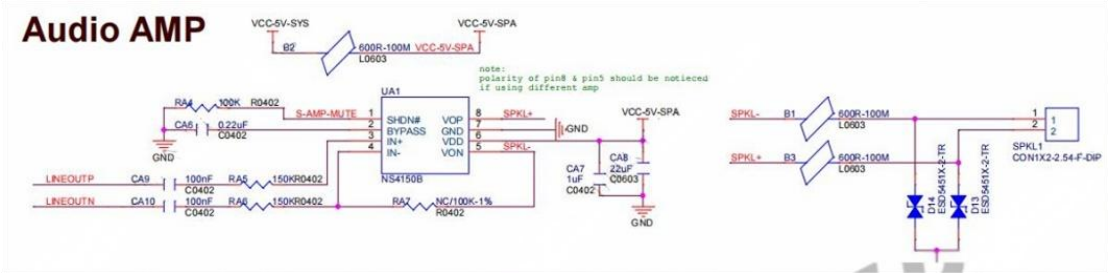
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6.11.Analog audio interface

The T536 chip integrates audio codec functions and can provide a simple analog audi o output interface. The ECK33-B core board leads to a single analog audio output interfac e (LINEOUTLP, LINEOUTLN), which can meet the needs of simple mono output applicat ions. The following figure shows the reference circuit of the Speaker output.

6.11.1. References



Audio Output Reference Schematic

6.11.2. Pin Definition

Analog audio signal pin definition

LGA	Name	MPU	Power Rail	Type	Length	Comment
C02	LINEOUTN	D29	ALDO4/1.8V	AO		
C01	LINEOUTP	D28	ALDO4/1.8V	AO		

6.11.3. LAYOUT SUGGESTIONS

- Place TVS close to the interface;
- Analog signal routing should be kept away from interference and can be wrapped wit h ground.

6.12.Digital Audio Interface

The ECK33-B core board can support 4-channel I2S/PCM, 4-channel DIMC, and 1-ch annel OWA digital audio interface . For the I2S/PCM interface, in the baseboard circuit d esign, it is necessary to connect the digital audio interface I2S/PCM signal to the audio c odec chip , and realize the audio interface functions such as headphones, microphones, an d speakers through the audio codec chip .

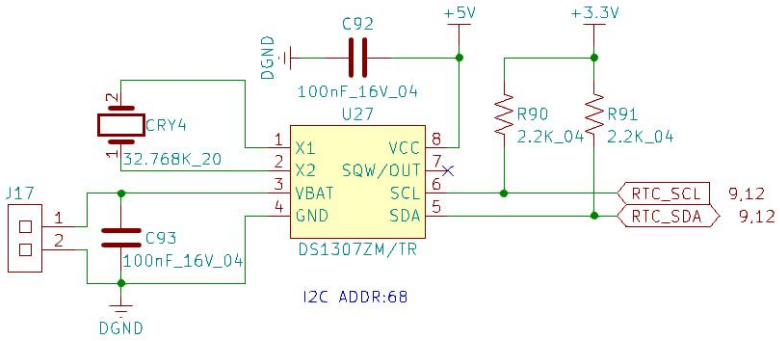
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6.13.RTC

the ECK33-B core board . If the user needs this RTC function, it can be expanded o n the baseboard through the I2C bus.

6.13.1. References



RTC reference circuit diagram

6.14.UART Interface

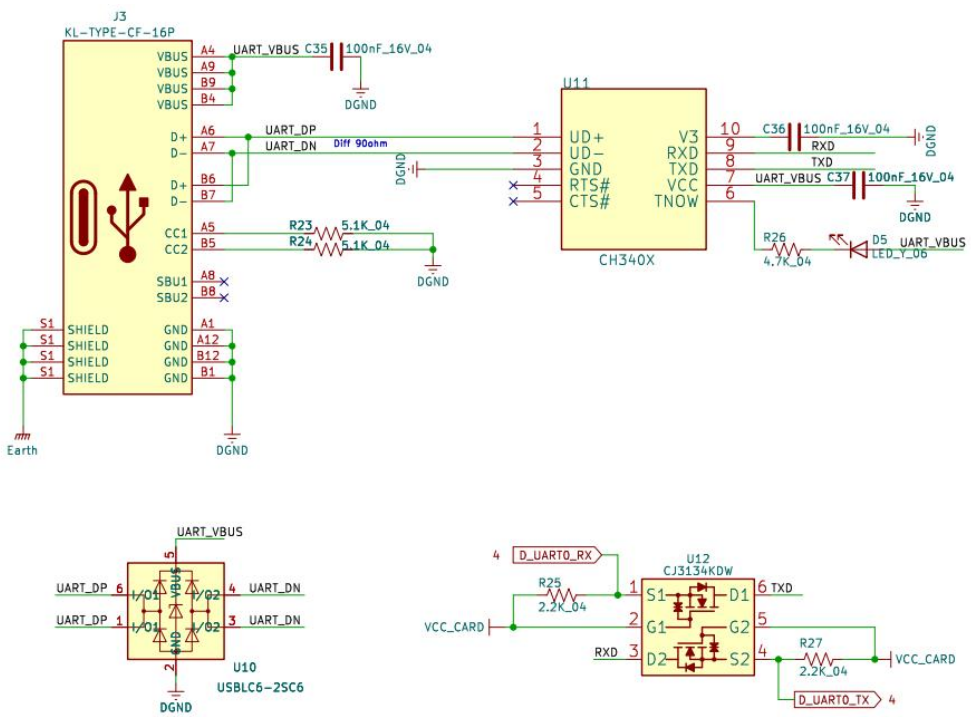
The ECK33-B core board supports up to 17 asynchronous serial ports , with a maxi mum baud rate of 10Mbps. For detailed serial port performance indicators, see the process or manual "T536_User Manual". The core board uses UART 0 as the debug serial port b y default. When designing the debug serial port on the baseboard, you need to pay attenti on to the serial port power-on timing.

6.14.1. References

For debugging convenience, the debug serial port can be brought out as a USB interf ace through the USB to serial port chip on the baseboard. The USB to serial port circuit schematic can be referred to in the figure below. The CH343G chip provides VIO power, which can effectively solve the problems of serial port I/O level compatibility and power domain power-on timing.

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USB debug serial port reference schematic

6.15.SPI interface

The ECK33-B series core board leads to 6 SPI interfaces , supporting master/slave m ode. The SPI signals include SPI_CLK, SPI_SS, SPI_MOSI and SPI_MISO. When designi ng, you must first confirm the relationship between the master and slave devices, and then confirm the direction of the MOSI and MISO signals. At the same time, the SPI interfac e of the ECK33-B series core board also supports DBI (display bus interface) mode.

6.16.I2C Interface

The ECK33-B series core board supports 9-way I2C (TWI) controller and 2 clock fre quency modes. The rate in standard mode is 100Kbit/s and the rate in fast mode is 400K bit/s.

Several devices can be mounted on the same I2C bus. The following points should b e noted when designing the schematic:

a) Check whether the device addresses on the same bus conflict;

b) Ensure that each I2C bus has a pair of pull-up resistors. The recommended resista nce is 2.2K~10K, but do not add duplicates.

c) The core board does not provide an I2C bus pull-up resistor, so the user needs to

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pull it up when using the baseboard;

d) Check whether the I2C interface level of the device is 3.3V. If not, a level conversion circuit needs to be added;

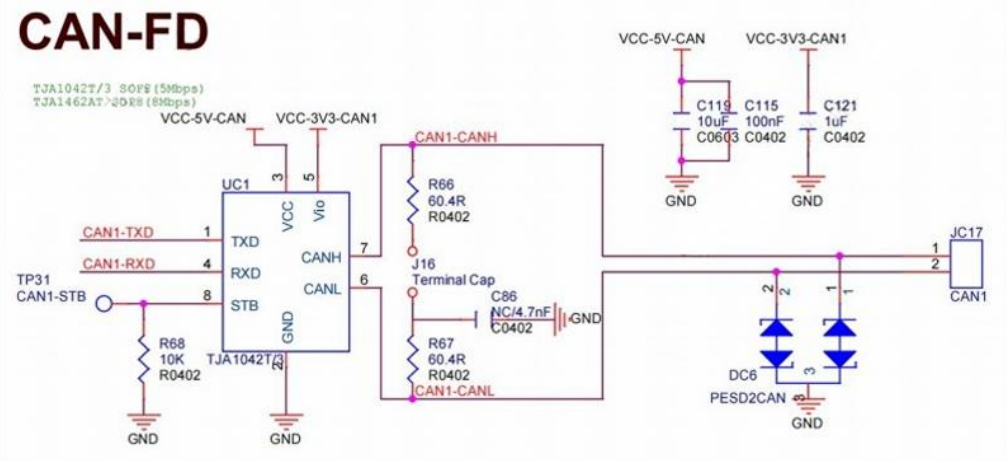
e) Check whether the I2C interface power rails are consistent. When I2C interfaces in different time domains are interconnected, the bus switch circuit needs to be considered;

f) Do not use too many devices on the same bus, otherwise it may exceed the 400pF load capacitance limit required by the I2C specification and affect the signal waveform.

6.17.CAN interface

The ECK33-B series core board supports 4-way CAN (CAN-FD) controllers and follows the ISO-11898 protocol . When designing, users need to select a CAN transceiver on the baseboard that can meet the application rate requirements. In addition, the CAN rate is also related to the cable length, networking conditions, etc.

6.17.1. References



CAN-FD Interface Reference Schematic

6.18.ADC Interface

The ECK33-B series core board provides two types of ADC interfaces, namely 1 LRADC (Low Rate ADC) and 18 (T536 has 21 GPADC, of which 3 are used to start related functions and cannot be used for ADC functions) dedicated GPADC (General Purpose ADC).

LRADC, 6-bit resolution, is used for key voltage recognition, with a maximum sampling rate of 2KHz and a sampling voltage range of 0~1.286V. When LRADC is used for

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key recognition, if the key adopts a voltage divider resistor, please ensure that the voltage interval between each key value is greater than 0.2V in the design. It is recommended to use 1% precision resistors. If no key is required and SDK compatibility is considered, LRADC must be added with a 100K pull-up resistor. Otherwise, it must be ensured that the software has turned off the LRADC related configuration before LRADC can float.

The specifications of GPADC are 12-bit sampling resolution and 10-bit accuracy, with a value range of 0V to 1.8V. It is recommended to reserve debugging filter capacitors when using them. When the external interface needs to use GPADC for acquisition, ESD tubes and series resistance can be added to enhance the anti-ESD capability. A 10nF capacitor can be reserved for the GPADC signal line to filter high-frequency noise.

The GPADC equivalent internal resistance is related to the sampling rate and the hold time. The higher the sampling rate and the shorter the hold time, the smaller the GPADC equivalent internal resistance. When using the resistor divider method to collect high voltage, it is important to note that the voltage divider resistor value cannot be too large. At the default 1MHz sampling rate, the sum of the two voltage divider resistor values cannot exceed 3.9K ohms. When using different sampling rates, it is important to note the corresponding maximum voltage divider resistor value and modify the corresponding hold time parameters.

The GPIO of the PA part is multiplexed with GPADC0-0~GPADC0-9. To ensure the accuracy of ADC, try to avoid the situation where the GPIO and GPADC of the PA group are used at the same time when allocating IO. That is, either the PA port function is only GPIO, or the PA port function is only GPADC. When mixed use is necessary, the following constraints need to be made: Regardless of output or input, the voltage frequency on the GPIO needs to be as low as possible and must not be higher than 80% of the sampling frequency of GPADC0.

6.18.1. Pin Definition

ADC interface pin definition

LGA	Name	MPU	Power Rail	Type	Length	Comment
A32	GPADC1-0	J29	ALDO4/1.8V	AI		1nF pull down
A33	GPADC1-1	H28	ALDO4/1.8V	AI		1nF pull down

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A34	GPADC1-2	J27	ALDO4/1.8V	AI		1nF pull down
A35	GPADC1-3	J28	ALDO4/1.8V	AI		1nF pull down
A70	GPADC1-7	K26	ALDO4/1.8V	AI		
A71	GPADC1-8	L28	ALDO4/1.8V	AI		
A72	GPADC1-9	M24	ALDO4/1.8V	AI		
A83	GPADC2-0	L27	ALDO4/1.8V	AI		
A84	GPADC2-1	M25	ALDO4/1.8V	AI		
A85	GPADC2-2	M26	ALDO4/1.8V	AI		
A86	GPADC2-3	M27	ALDO4/1.8V	AI		
A54	GPADC2-4	M28	ALDO4/1.8V	AI		
A50	GPADC2-5	N27	ALDO4/1.8V	AI		
A51	GPADC2-6	N28	ALDO4/1.8V	AI		
A55	GPADC2-7	N29	ALDO4/1.8V	AI		
A52	GPADC2-8	P26	ALDO4/1.8V	AI		
A53	GPADC2-9	P27	ALDO4/1.8V	AI		
A11	GPADC3-0	H27	ALDO4/1.8V	AI		
D73	PA_GPADC00	H24	CLDO4/3.3V	I/O		GPADC0-0
D74	PA_GPADC01	H25	CLDO4/3.3V	I/O		GPADC0-1
A21	PA_GPADC02	F27	CLDO4/3.3V	I/O		GPADC0-2
A42	PA_GPADC03	E28	CLDO4/3.3V	I/O		GPADC0-3
A43	PA_GPADC04	E29	CLDO4/3.3V	I/O		GPADC0-4
A41	PA_GPADC05	F28	CLDO4/3.3V	I/O		GPADC0-5
A20	PA_GPADC06	G29	CLDO4/3.3V	I/O		GPADC0-6
A44	PA_GPADC07	G28	CLDO4/3.3V	I/O		GPADC0-7
A45	PA_GPADC08	G27	CLDO4/3.3V	I/O		GPADC0-8
A22	PA_GPADC09	H26	CLDO4/3.3V	I/O		GPADC0-9

6.19.LocalBus Interface

The ECK33-B series core board supports 1 high-speed parallel bus LocalBus, with a maximum rate of 100M*16bit (due to pin multiplexing, the core board only supports 16 b its at most). It can be used to exchange data with FPGA. The evaluation board provides a set of 8-bit LocalBus interfaces for connecting FPGA devices.

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6.19.1. Pin Definition

LocalBus signal pin definition

LGA	Name	MPU	Power Rail	Type	Length	Comment
C93	PE14_LB	B10	DCDC4/3.3V	I/O	918.94	LBUS-LCLK
C58	PE10_LB	D9	DCDC4/3.3V	I/O	702.54	LBUS-ALE
C73	PE15_LB	H13	DCDC4/3.3V	I/O	697.63	LBUS-INTR
C74	PE16_LB	G13	DCDC4/3.3V	I/O	692.85	LBUS-DRQ
C36	PE17_LB	F13	DCDC4/3.3V	I/O	822.86	LBUS-LBE
C37	PE8_LB	E9	DCDC4/3.3V	I/O	814.14	LBUS-WR
C38	PE9_LB	D11	DCDC4/3.3V	I/O	878.4	LBUS-READY
C19	PE0_LB	B9	DCDC4/3.3V	I/O	891.89	LBUS-CS0
C18	PE1_LB	G9	DCDC4/3.3V	I/O	880.47	LBUS-CS1
C17	PE2_LB	F9	DCDC4/3.3V	I/O	905.79	LBUS-CS2
C16	PE3_LB	G11	DCDC4/3.3V	I/O	965.05	LBUS-CS3
C57	PE11_LB	C10	DCDC4/3.3V	I/O	723.58	LBUS-BURST0
C56	PE12_LB	A10	DCDC4/3.3V	I/O	704.45	LBUS-BURST1
C35	PE13_LB	C9	DCDC4/3.3V	I/O	799.01	LBUS-BURST2
C15	PE4_LB	F11	DCDC4/3.3V	I/O	903.68	LBUS-DP0
C14	PE5_LB	E11	DCDC4/3.3V	I/O	864.55	LBUS-DP1
C13	PE6_LB	D13	DCDC4/3.3V	I/O	711.04	LBUS-DP2
C12	PE7_LB	E13	DCDC4/3.3V	I/O	742.66	LBUS-DP3
C42	PK0_LB_MIA-D0N	B13	DCDC4/3.3V	I/O	1116.38	LBUS-LD0
C62	PK1_LB_MIA-D0P	A13	DCDC4/3.3V	I/O	1115.17	LBUS-LD1
C41	PK2_LB_MIA-D1N	B11	DCDC4/3.3V	I/O	1074.07	LBUS-LD2
C79	PK3_LB_MIA-D1P	A11	DCDC4/3.3V	I/O	1074.92	LBUS-LD3
C61	PK4_LB_MIA-CKN	B12	DCDC4/3.3V	I/O	1068.11	LBUS-LD4
C40	PK5_LB_MIA-CKP	A12	DCDC4/3.3V	I/O	1068.25	LBUS-LD5
C78	PK6_LB_MIB-D0N	B16	DCDC4/3.3V	I/O	1318.93	LBUS-LD6
C60	PK7_LB_MIB-D0P	A16	DCDC4/3.3V	I/O	1320.11	LBUS-LD7
C92	PK8_LB_MIB-D1N	B14	DCDC4/3.3V	I/O	1232.84	LBUS-LD8
C39	PK9_LB_MIB-D1P	A14	DCDC4/3.3V	I/O	1234.82	LBUS-LD9
C77	PK10_LB_MIB-CKN	B15	DCDC4/3.3V	I/O	1220.21	LBUS-LD10
C59	PK11_LB_MIB-CKP	A15	DCDC4/3.3V	I/O	1220.22	LBUS-LD11
C91	PK12_LB_MIC-D0N	B19	DCDC4/3.3V	I/O	1163.49	LBUS-LD12

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C76	PK13_LB_MIC-D0P	A19	DCDC4/3.3V	I/O	1161.67	LBUS-LD13
C90	PK14_LB_MIC-D1N	B17	DCDC4/3.3V	I/O	1076.36	LBUS-LD14
C75	PK15_LB_MIC-D1P	A17	DCDC4/3.3V	I/O	1078.19	LBUS-LD15

6.19.2. LAYOUT SUGGESTIONS

- The command lines (such as BURST signal , WR signal , RD signal) and address data lines (LD[31:0]) should be equal in length to the reference clock signal. Designed for 150MHz, it is recommended that the length be controlled within 300mil and not exceed 500mil.
- To meet the 3W principle, the number of vias for signal lines should be as similar as possible ;
- Reference plane complete, etc.

6.20.GPIO interface

The ECK33-B series core board can provide up to 199 GPIO interfaces, but most of them have multiplexing functions. Users can flexibly configure GPIO according to their own needs.

6.21.Hardware Design Checklist

- Power rail: Check whether there is an inconsistent power rail problem in the I/O interface application, such as connecting a 1.8V signal to a 3.3V signal. If there is a need to connect signals with different power rails, a level conversion circuit should be used.
- Power-on sequence: Check whether the signals connecting the baseboard and the core board are powered on first, or whether the power-on time of the two board signals is very different.
- Pull-up and pull-down resistors: The output state of the multiplexed I/O interface is uncertain before the power-on software configuration. If the signal needs to maintain a stable level when powered on, pull-up and pull-down resistors should be designed on the baseboard. Some functional signals also need to be designed with pull-up or pull-down resistors on the baseboard, such as I2C signals. When designing pull-up resist

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ors, attention should be paid to the design of the pull-up power rail.

- ESD protection: The corresponding ESD protection design should be considered for the external interface signal. The selection of ESD solution should take into account the requirements of signal rate, communication protocol and application environment.
- High-speed signals should be of equal length: High-speed signals should consider the equal length design of PCB, including USB, Ethernet, SDIO, display, etc.
- Impedance control: High-speed signals should consider PCB impedance control. The key to impedance control is to maintain impedance continuity. The baseboard should be designed with reference to the impedance of the core board signal.

7. Software Resources

The ECB33-PGB single-board computer is equipped with an operating system based on the Linux 5.10 kernel. The single-board computer comes with the cross-compilation tool chain Buildroot source code, U-boot source code, Linux kernel and various driver module source code required for embedded Linux system development, as well as various development and debugging tools suitable for Windows desktop environment and Linux desktop environment.

operating system:

1. Linux file system built by Buildroot
2. Linux file system transplanted by Ubuntu

System source code:

1.U-boot 2023

2. Kernel 5.10

3.BuildRoot 2022.05

4.Ubuntu 24.04

Development environment and tools:

1.USB burning tool: PhoenixSuit

2. SD card burning tool: PhoenixCard

System software resources are shown in the following table:

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System Software Resource Table

category	name	describe	Source code
SPL	spl-pub	Boot0, boot uboot	<SDK>/ brandy/brandy-2.0/spl-pub /
BOOT	u-boot 2 023.04	Bootloader	<SDK>/brandy/brandy-2.0/u-boot-20 23 /
Kernel	Kernel 5.10	Linux Kernel	<SDK> /kernel/linux-5.10* /
Device Driver	Audio	Built-in audio driver	<SDK> /bsp/drivers/sound/platform/*
	AWlink	CAN Driver	<SDK> /bsp/drivers/can
	GMAC	Built-in MAC driver	<SDK> /bsp/drivers/gmac
	GPADC	GPADC Driver	<SDK> /bsp/drivers/gpadc
	GPIO	GPIO Driver	<SDK> /bsp/drivers/pinctrl/
	DRM	Display Driver	<SDK> /bsp/drivers/drm/panel/*
	LRADC	Button module driver	<SDK> /bsp/drivers/lradc
	MMC	MMC Driver	<SDK> /bsp/drivers/mmc
	SPI	SPI Driver	<SDK> /bsp/drivers/spi
	TWI	I2C Driver	<SDK> /bsp/drivers/twi
	UART	Serial port driver	<SDK> /bsp/drivers/uart
	P CIE	PCIE driver	<SDK> /bsp/drivers/ pcie
	LocalBus	LocalBus Driver	<SDK> /bsp/drivers/ lb c
	V IN	Specific camera drivers	<SDK> /bsp/drivers/vin/modules/sensor/
operating system	Buildroot 20 2205	Buildroot 202205 version	<SDK>/buildroot/buildroot -202205
	U buntu	Ubuntu 24.04	<SDK>/ buildroot/ubuntu
Development Tools	PhoenixSuit	USB burning tool	/tools/ PhoenixSuit
	PhoenixCard	SD card burning tool	/tools/PhoenixCard

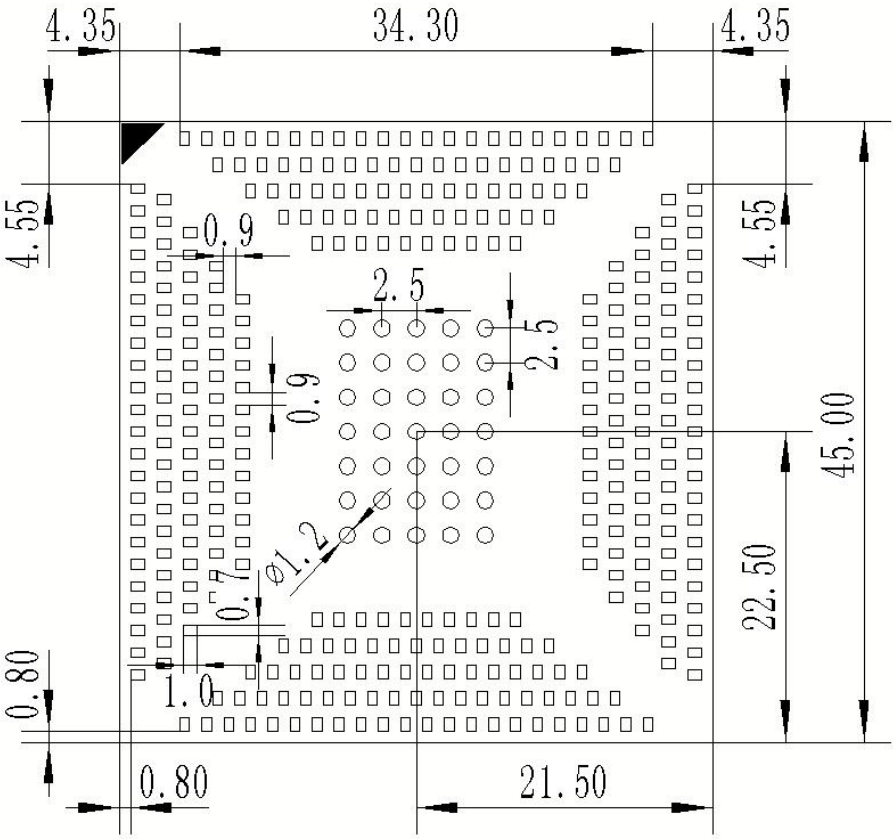
8. Structural dimensions

The ECK33-B series core board adopts 381 PIN, LGA interface, and can be SMT sol dered. There are no components on the bottom of the core board, no exposed wiring, and the bottom board design is simple.

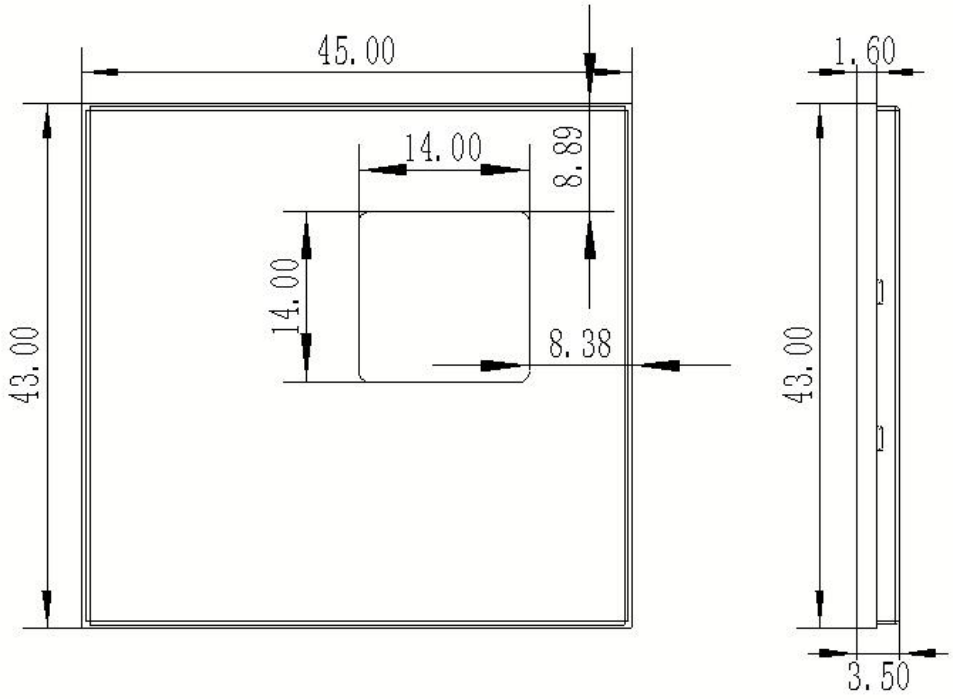
The ECK33-B series core board is 45.0mm long and 43.0mm wide, with 346 rectang ular pads (1.0×0.7mm) and 35 round pads (1.2mm in diameter). The structural dimension s are shown in the figure below. The following dimensions are in millimeters (mm), the s tructural dimension tolerance is ±0.1mm, and the PCB thickness tolerance is 10%.

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LGA core board structure dimensions (top view)



LGA core board shielding cover structure size drawing

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9. Welding Instructions

Note: For LGA interface core modules, to ensure the quality of the solder paste on the module pads, the recommended stencil thickness for the corresponding pads is 0.15–0.18 mm.

9.1.Reflow temperature

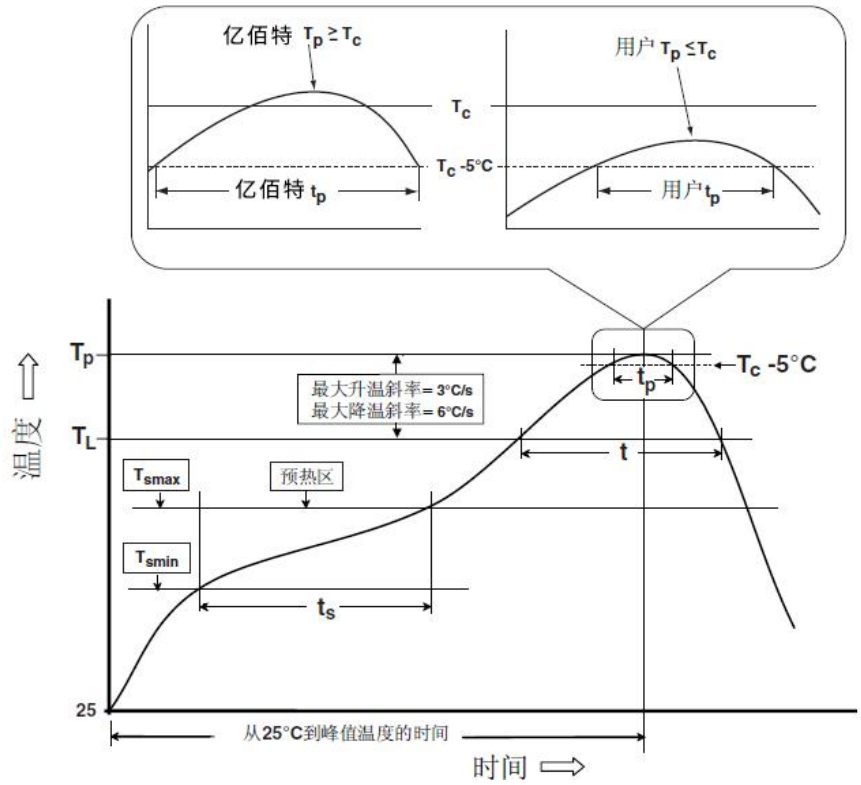
Reflow Temperature Table

Reflow profile characteristics		Leaded process assembly	Lead-free assembly
Preheating/keeping	Minimum temperature (Tsmin)	100℃	150℃
	Maximum temperature (Tsmax)	150℃	200℃
	Time (Tsmin~Tsmin)	60-120 seconds	60-120 seconds
Heating slope (TL~Tp)		3℃/sec, max.	3℃/sec, max.
Liquidus temperature (TL)		183℃	217℃
Keep time above TL		60~ 90 seconds	60~ 90 seconds
Package peak temperature Tp		Users must not exceed the temperature stated on the product's "Moisture Sensitivity" label.	Users must not exceed the temperature stated on the product's "Moisture Sensitivity" label.
The time (Tp) within 5° C of the specified classification temperature (Tc) is shown in the figure below.		20 seconds	30 seconds
Cooling slope (Tp~TL)		6℃/sec, max.	6℃/sec, max.
Time from room temperature to peak temperature		6 minutes, longest	8 minutes, longest
※The peak temperature (Tp) tolerance of the temperature curve is defined as the upper limit of the user			

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9.2.Reflow Oven Profile



Reflow Oven Profile

10. Revision Notes

Revision Notes Table

Version	Modifications	Modification time	prepared by	Proofreading	Approval
V1.0	First Draft	25-07-03	WFX	Wlq	WFX
V1.1	Correct the number of TWI and SPI functions; Add stencil thickness requirements for LGA.; Change USB2.0 DRD to 1 channel;	25-08-26	WFX	Wlq	WFX

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