Product Manual
ECK32-T527B core board



Chengdu Ebyte Electronic Technology Co.,Ltd.

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1. Product Overview

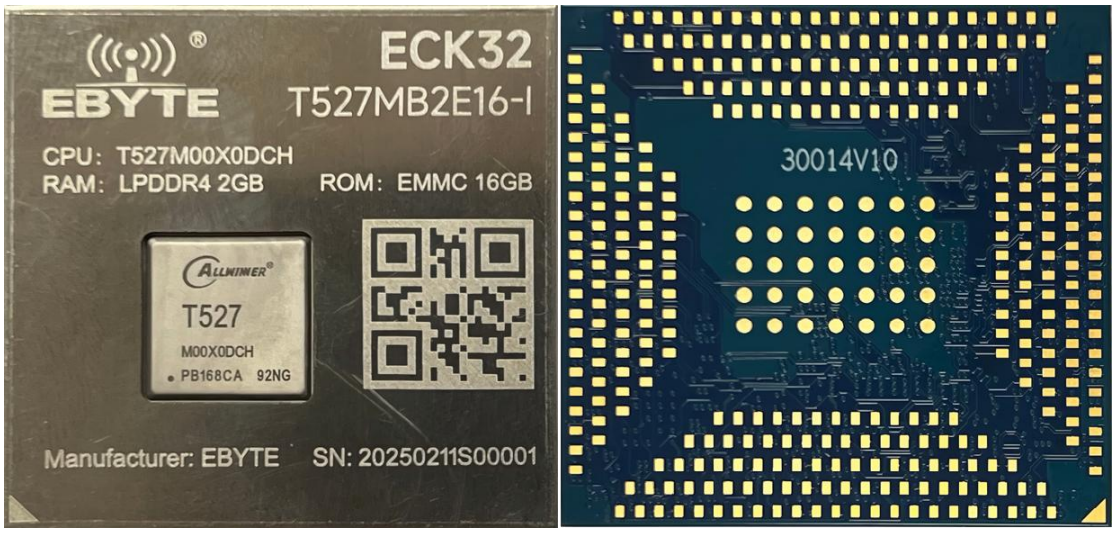
1.1.Product Introduction

Ebyte ECK32-T527B series core board is carefully designed based on Allwinner's T527 series processor, and adopts a new LGA interface form of high performance, low power consumption, high reliability, and domestically produced industrial-grade embedded core board. It can be widely used in content sharing and self-service terminals, intelligent manufacturing, and other electronic business and industrial equipment.

Allwinner T527 series is a SOC product with high-performance octa-core Cortex-A55 AI platform, suitable for commercial, industrial and automotive fields. The chip family integrates octa-core Cortex-A55 CPU, HiFi4 DSP, 2 TOPS NPU, ARM G57 MC1 GPU, 32-bit DDR3/DDR3L/DD4/LPDDR3/LPDDR4/LPDDR4X DRAM, high-speed interface (PCIe2.1 and USB3.1), automotive interface (CAN), multiple video output interface (2*RGB/2*Dual-LVDS/2*MIPI-DSI/HDMI/eDP) and video input interface (MIPI CSI). The chip family supports 4K@60fps H.265 decoder, 4K@30fps H.264 decoder, 4K@25fps H.264 encoder, DI and AWonder system, providing users with smooth experience and professional AI visual effects.

The ECK32-T527B series core board includes 4 specific product models, all of which are designed with domestically produced industrial-grade devices. They mainly differ in NPU support, DRAM memory capacity, eMMC storage capacity, operating temperature environment, etc. Customers can choose the appropriate model according to their needs. For product selection, please refer to the product selection section.

The physical picture of the ECK32-T527B series core board (no components on the bottom of the product) is as follows:



Physical picture

1.2.Features

1. Processor: Allwinner LT527M/MN series processor;

- Quad-core ARM CortexTM-A55@1.8GHz, Quad-core ARM CortexTM-A55@1.4GHz;

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- HiFi4 DSP@600MHz;
- RISC-V@200MHz;
- NPU 2TOPS (supported only by T527MN);

2. show:

- GPU: ARM G57 MC1;
- VPU: H.265 4K@60fps decoding, H.264 4K@60fps decoding, H.264 4K@25fps encoding;

3. Memory: LPDDR4 2GB/4GB, 32bits;

4. Storage: 16GB/32GB eMMC optional;

5. Video Output:

- 1 HDMI 2.0, supports 4K@60fps ;
- 1-way eDP, supporting 2.5K@60fps/4K@30fps ;
- 2-way dual-link LVDS , support 1080p@60fps ;
- 2-way RGB video output interface , supporting 1080p@60fps ;
- 2-way 4-lane or 1-way 4 + 4 -lane MIPI-DSI, supporting 2K@60fps /2.5K@60fps/4K@45fps;

6. Video Input:

- 1-channel DVP camera input, 16 bits;
- 4+4-lane or 4+2+2-lane or 2+2+2+2-lane MIPI-CSI input;

7. Audio:

- 2-channel DAC, 3-channel ADC, 3-channel audio output, 3-channel audio input;
- 4-way I2S/PCM interface;
- 1 SPIF I/O;

8. Network: 2-way Gigabit Ethernet controller, supporting RGMII/RMII interface;

9. PCIE : 1-channel PCIe2.1, RC mode (multiplexed with USB3.1);

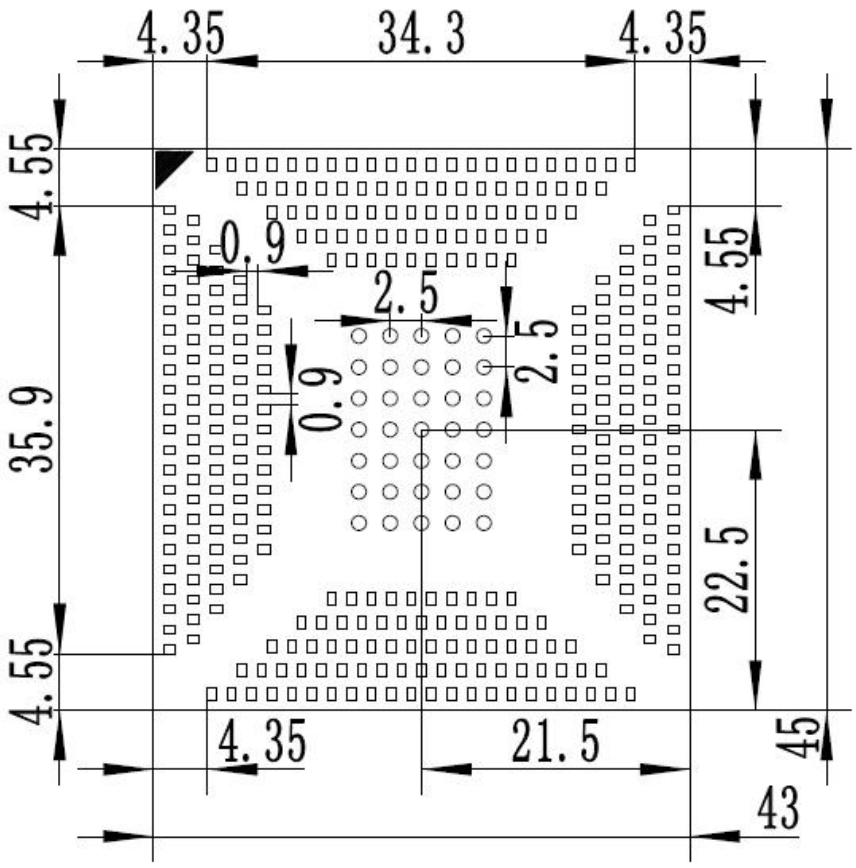
10. USB: 1-channel USB2.0 DRD, 1-channel USB2.0 HOST;

- 1-channel USB2.0 DRD ;
- 1-way USB2.0 Host ;
- 1 USB3.1 DRD (multiplexed with PCIe2.1) ;

11. SDIO: SDIO3.0/ EMMC5.0 controller;

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12. 10-channel UART;
13. 2-way CAN ;
14. 8-way I2C;
15. 30 -channel PWM;
16. 4-way SPI;
17. 8-channel GPADC, 12 bits; 2-channel LRADC, 6 bits;
18. 2 CIR RX, 1 CIR TX;
19. GPIO 187;
20. Operating system: Ubuntu;
21. power supply:
    - Single DC +5V±10%@2A power input;
    - 1 3.3V@500mA power output;
22. Interface type: LGA 381 PIN;
23. Size: 45×43×1.6mm, as shown in the figure below:



Dimensions

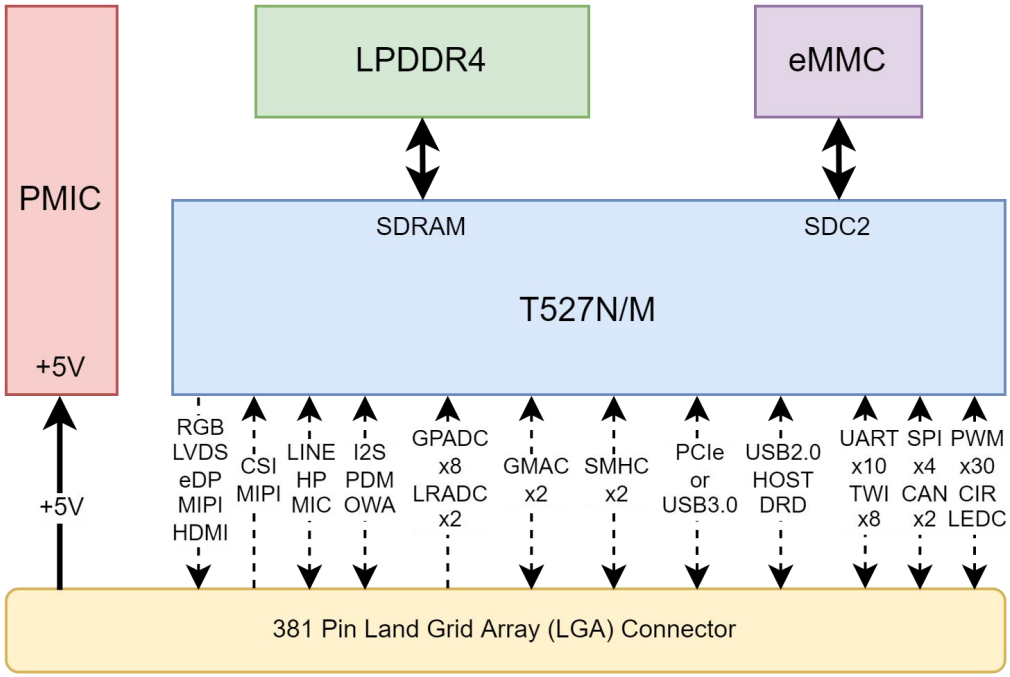
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24.Operating Temperature:

- Wide temperature range: -25℃-85℃;
- Industrial grade: -40℃-85℃;

25.PCB process: 12-layer board design, immersion gold, lead-free process;

1.3.Core board functional block diagram



Functional Block Diagram

1.4.Typical Applications

- Smart home;
- Smart toys;
- Smart cities;
- Tablet computer ;
- IoT Gateway ;
- Advertising all-in-one machine ;
- Industrial all-in-one machine ;
- Industrial control motherboard;
- Robots and drones.

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2. Product Selection

2.1.Model configuration

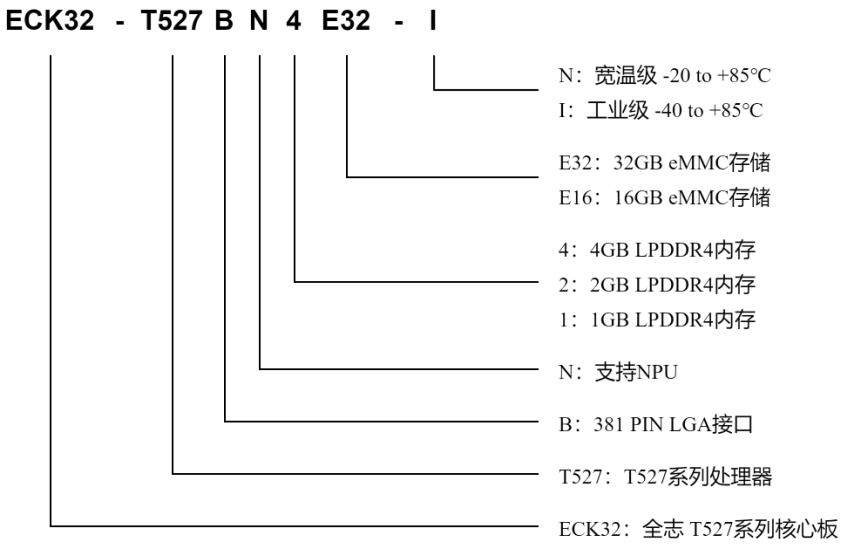
The ECK32-T527B series core board selection and configuration table is as follows:

Product Selection and Configuration Table

Serial number	Product Model	Processor model	Memory	storage	Operating temperature
1	ECK32-T527BN4E32-I	T527M02X0DCH	4GB LPDDR4	32GB eMMC	Domestic industrial grade -40℃ ~ 85℃
2	ECK32-T527BN4E32-N	T527M02X0DCH	4GB LPDDR4	32GB eMMC	Domestic wide temperature grade -25℃ ~ 85℃
3	ECK32-T527B2E16-I	T527M00X0DCH	2GB LPDDR4	16 GB eMMC	Domestic industrial grade -40℃ ~ 85℃
4	ECK32-T527B4E32-N	T527M00X0DCH	4GB LPDDR4	32GB eMMC	Domestic wide temperature grade -25℃ ~ 85℃

2.2.Model code

The product model coding is shown in the figure below:



Model code description

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3. Quick Experience

Choosing Ebyte ECB32-PGB series single board computer products, you can quickly experience the typical application functions of ECK32-T527B core board products, and understand the development methods such as baseboard hardware design and software development.

4. Features and parameters

4.1.Product Features

The ECK32-T527B series core board mainly integrates the processor, DRAM memory, eMMC storage and PMIC power system, and leads out all the I/O pins on the processor. Users can design the baseboard to apply the I/O resources on the core board according to their needs and reuse the I/O into the functional interface they need.

The following table lists the main function parameters of the ECK32-T527B series core board integrated on the board, and the function parameters of the reusable I/O resources. The description of each I/O function is the maximum indicator that the core board can use the I/O function without using other I/O functions (for example, after using the 24-bit color RGB interface function and the network interface function, all UART functions cannot be realized).

Product Features

Function	Functional Description
CPU	T527M/MN ; Octa-core ARM CortexTM-A55, up to 1.8 GHz; RISC-V CPU, up to 200 MHz; HiFi4 Audio DSP; ARM G57 MC1 GPU; Up to 2 TOPS NPU(T527M not supported);
MEM	On board 2GB LPDDR4 / 4GB LPDDR4 ;
FLASH	On board 16GB / 32GB eMMC ;
Video Engine	H.265 MP and VP9 decoder up to 4K@60fps ; H.264 BL/MP/HP decoder up to 4K@30fps ; H.264 BP/MP/HP encoder up to 4K@25fps ; MJPEG encoder up to 4K@15fps, JPEG encoder up to 8K x 8K resolution ;
Video Output	2x dual-link LVDS interfaces, up to 1080p@60fps; 2x RGB interfaces with DE/SYNC mode, up to 1080p@60fps; 1x eDP 1.3, up to 2.5K@60fps and 4K@30fps; 4+4-lane MIPI-DSI output interface up to 2.5K@60fps and 4K@45fps; 1x HDMI2.0 TX interface, supporting HDCP1.4;

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Video Input	8/10/12/16-bit parallel CSI, support BT.1120 up to 4 x 1080P@30fps ; 4+4-lane, 4+2+2-lane, or 2+2+2+2-lane MIPI CSI, up to 2.0 Gbit/s per lane ; Compliant with MIPI-CSI2 V1.1 and MIPI DPHY V1.1 ; Maximum video capture resolution of 8M@30fps for MIPI CSI ;
Audio	3x audio outputs: LINEOUTLP/N, LINEOUTRP/N, HPOUTL/R ; 2x audio inputs: MICIN1P/N, MICIN2P/N ; 4x I2S/PCM external interfaces: I2S0, I2S1, I2S2, and I2S3 ; 8 x digital PDM microphones (DMIC) ; 1x OWA RX and 1x OWA TX, compliance with S/PDIF interface ;
GMAC	2 x GMAC (10/100/1000 Mbps port with RGMII and RMII interfaces) ;
SMHC	2 x SD/MMC host controller (SMHC) interfaces ; SMHC0, compliant with the protocol Secure Digital Memory (SD3.0); SMHC1, compliant with the protocol Secure Digital I/O (SDIO3.0);
PCIe	1 x PCIe2.1&USB3.1 combo PHY ; Compliance to PCI Express Base Specification, Revision 2.1 ; Supports 1 Lane link width , Root Complex (RC) mode;
USB	2x USB2.0 Host ; 1 x USB2.0 DRD ; 1 x USB3.1 DRD&PCIe2.1 Combo ;
UART	Up to 10 UART controllers ; Compatible with industry-standard 16450/16550 UARTs ; Speed up to 10 Mbit/s with 160 MHz APB clock ;
TWI	8x TWI controllers ; Standard mode (up to 100 Kbit/s) and fast mode (up to 400 Kbit/s) ;
SPI	4x SPI controllers ; SPI0, SPI2, and S_SPI0, supporting SPI mode ; SPI1, supporting SPI mode and display bus interface (DBI) mode ;
CAN	2x CAN controllers , supports the CAN 2.0A and 2.0B protocol specification;
PWM	30x PWM channels and 4x PWM controllers ;
CIR	2x CIR_RX interfaces, 1x CIR_TX interface;
LEDC	Maximum 1024 LEDs serial connect ;
GPADC	8x GPADC input; 12-bit sampling resolution and 10-bit precision ; Maximum sampling frequency up to 1 MHz ;
LRADC	2x LRADC input ; 6-bit resolution ; Sampling rate up to 2 kHz ;
JTAG	ARM , RISC-V , HiFi4 DSP JTAG ;
GPIO	187x GPIO , Supports Interrupt input ;

4.2.Environmental characteristics

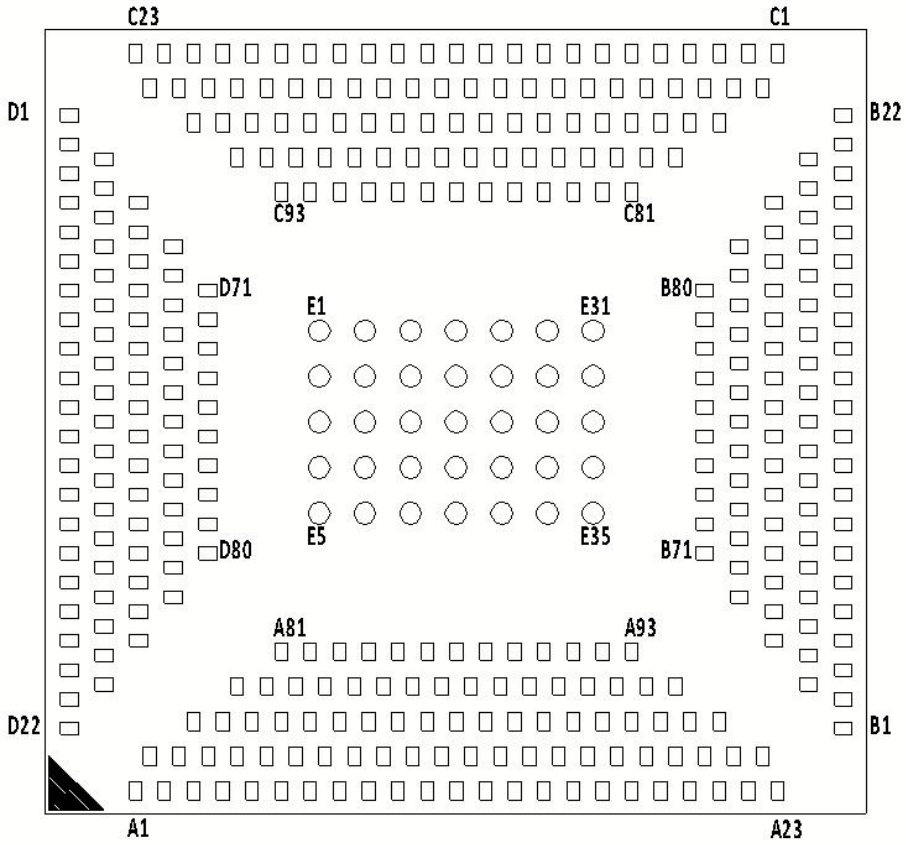
Environmental characteristics table

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Operating temperature	Wide temperature range	-25℃ ~ 85℃;
	Industrial Grade	-40℃ ~ 85℃;
Storage temperature	-40℃ ~ 85℃;	
Operating humidity	5% to 95% humidity, non-condensing;	
Storage humidity	60℃@95% humidity, non-condensing;	

4.3.I/O Features

4.3.1. Pin numbering diagram



Pin Numbering Diagram (Top View)

Note: The above picture is a top view, which is a mirror image of the pins observed from the bottom of the actual object.

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4.3.2. Pin Definition Table

The ECK32-T527B core board interface pin definitions are shown in the following table. If you need to change the pin function, please modify the relevant driver configuration code.

Pin Definition Table

LGA	Pin Name	MPU	Power Rail	Type	Comment
A01	PK13	C9	BLDO3/1.8V/DCDC4/3.3V	I/O	
A02	PK12	B9	BLDO3/1.8V/DCDC4/3.3V	I/O	
A03	GND		GND/0V	PWR	
A04	PK19	B6	BLDO3/1.8V/DCDC4/3.3V	I/O	
A05	PK18	A6	BLDO3/1.8V/DCDC4/3.3V	I/O	
A06	GND		GND/0V	PWR	
A07	PJ12	J4	BLDO3/1.8V/DCDC4/3.3V	I/O	
A08	PJ11	G5	BLDO3/1.8V/DCDC4/3.3V	I/O	
A09	GND		GND/0V	PWR	
A10	PG10	U5	BLDO1/3.3V	I/O	
A11	PG11	U4	BLDO1/3.3V	I/O	
A12	PG12	U3	BLDO1/3.3V	I/O	
A13	MICIN1P	AD1	ALDO4/1.8V	AI	
A14	MICIN2N	AD2	ALDO4/1.8V	AI	
A15	GND		GND/0V	PWR	
A16	GPADC3	W4	ALDO4/1.8V	AI	
A17	GPADC8	AA1	ALDO4/1.8V	AI	
A18	GND		GND/0V	PWR	
A19	PE5	B3	DCDC4/3.3V	I/O	
A20	PE6	A3	DCDC4/3.3V	I/O	
A21	PE7	A2	DCDC4/3.3V	I/O	
A22	PL10	AK9	ALDO3/3.3V	I/O	
A23	PL11	AJ9	ALDO3/3.3V	I/O	
A24	PK15	B8	BLDO3/1.8V/DCDC4/3.3V	I/O	
A25	PK14	A8	BLDO3/1.8V/DCDC4/3.3V	I/O	
A26	GND		GND/0V	PWR	
A27	PK21	B5	BLDO3/1.8V/DCDC4/3.3V	I/O	
A28	PK20	A5	BLDO3/1.8V/DCDC4/3.3V	I/O	
A29	PJ13	J5	BLDO3/1.8V/DCDC4/3.3V	I/O	
A30	PJ1	D2	BLDO3/1.8V/DCDC4/3.3V	I/O	
A31	PJ0	D1	BLDO3/1.8V/DCDC4/3.3V	I/O	
A32	GND		GND/0V	PWR	
A33	PG13	U2	BLDO1/3.3V	I/O	
A34	PG14	U1	BLDO1/3.3V	I/O	
A35	MICIN2N	AE1	ALDO4/1.8V	AI	
A36	MICIN2P	AE2	ALDO4/1.8V	AI	

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A37	MBIAS	AK1	CLDO3/3.3V	PWR	
A38	GND		GND/0V	PWR	
A39	GPADC6	Y2	ALDO4/1.8V	AI	
A40	LRADC0	V3	ALDO4/1.8V	AI	
A41	PE0	E6	DCDC4/3.3V	I/O	
A42	PE8	B2	DCDC4/3.3V	I/O	
A43	PE9	B1	DCDC4/3.3V	I/O	
A44	GND		GND/0V	PWR	
A45	GND		GND/0V	PWR	
A46	PK17	C7	BLDO3/1.8V/DCDC4/3.3V	I/O	
A47	PK16	B7	BLDO3/1.8V/DCDC4/3.3V	I/O	
A48	GND		GND/0V	PWR	
A49	PJ8	H2	BLDO3/1.8V/DCDC4/3.3V	I/O	
A50	PJ9	H3	BLDO3/1.8V/DCDC4/3.3V	I/O	
A51	PJ3	E2	BLDO3/1.8V/DCDC4/3.3V	I/O	
A52	PJ2	E1	BLDO3/1.8V/DCDC4/3.3V	I/O	
A53	PG0	R1	BLDO1/3.3V	I/O	
A54	PG1	R2	BLDO1/3.3V	I/O	
A55	HPOUTFB	AM1	BLDO3/1.8V	AI	
A56	HPOUTL	AL2	BLDO3/1.8V	AO	
A57	HPOUTR	AM2	BLDO3/1.8V	AO	
A58	GND		GND/0V	PWR	
A59	GPADC4	W5	ALDO4/1.8V	AI	
A60	GPADC9	AA2	ALDO4/1.8V	AI	
A61	GND		GND/0V	PWR	
A62	NC	/	/	/	
A63	GND		GND/0V	PWR	
A64	PL7	AM8	ALDO3/3.3V	I/O	
A65	PK23	B4	BLDO3/1.8V/DCDC4/3.3V	I/O	
A66	PK22	A4	BLDO3/1.8V/DCDC4/3.3V	I/O	
A67	PJ15	L5	BLDO3/1.8V/DCDC4/3.3V	I/O	
A68	PJ14	L4	BLDO3/1.8V/DCDC4/3.3V	I/O	
A69	PJ10	G4	BLDO3/1.8V/DCDC4/3.3V	I/O	
A70	GND		GND/0V	PWR	
A71	PG2	P3	BLDO1/3.3V	I/O	
A72	PG3	P2	BLDO1/3.3V	I/O	
A73	HP-DET	AJ2	ALDO4/1.8V	AI	
A74	LINEOUTLP	AG2	ALDO4/1.8V	AO	
A75	LINEOUTLN	AG1	ALDO4/1.8V	AO	
A76	GND		GND/0V	PWR	
A77	GPADC7	Y3	ALDO4/1.8V	AI	
A78	LRADC1	V2	ALDO4/1.8V	AI	
A79	PE10	C2	DCDC4/3.3V	I/O	

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A80	PL6	AN8	ALDO3/3.3V	I/O	
A81	PJ6	G1	BLDO3/1.8V/DCDC4/3.3V	I/O	
A82	PJ7	G2	BLDO3/1.8V/DCDC4/3.3V	I/O	
A83	PJ5	F2	BLDO3/1.8V/DCDC4/3.3V	I/O	
A84	PJ4	F1	BLDO3/1.8V/DCDC4/3.3V	I/O	
A85	PG4	T3	BLDO1/3.3V	I/O	
A86	PG5	T2	BLDO1/3.3V	I/O	
A87	GND		GND/0V	PWR	
A88	LINEOUTRP	AH2	ALDO4/1.8V	AO	
A89	LINEOUTRN	AH1	ALDO4/1.8V	AO	
A90	GND		GND/0V	PWR	
A91	GPADC5	W6	ALDO4/1.8V	AI	
A92	GPADC10	AA3	ALDO4/1.8V	AI	
A93	GND		GND/0V	PWR	
B01	PE1	C4	DCDC4/3.3V	I/O	
B02	PE2	E5	DCDC4/3.3V	I/O	
B03	PE4	C3	DCDC4/3.3V	I/O	
B04	PE12	C1	DCDC4/3.3V	I/O	
B05	PJ20	K3	DCDC4/3.3V	I/O	
B06	PL12	AK7	ALDO3/3.3V	I/O	
B07	PG8	R4	BLDO1/3.3V	I/O	
B08	GND		GND/0V	PWR	
B09	PJ16	J1	BLDO3/1.8V/DCDC4/3.3V	I/O	
B10	PI6	AK15	DCDC4/3.3V	I/O	
B11	PI7	AH15	DCDC4/3.3V	I/O	
B12	PI0	AH13	DCDC4/3.3V	I/O	
B13	PI1	AG13	DCDC4/3.3V	I/O	
B14	PI11	AM17	DCDC4/3.3V	I/O	
B15	PM2	AM4	BLDO1/3.3V	I/O	
B16	GND		GND/0V	PWR	
B17	GND		GND/0V	PWR	
B18	GND		GND/0V	PWR	
B19	VDD_CORE_5V		5V IN/5V	PWR	
B20	VDD_CORE_5V		5V IN/5V	PWR	
B21	VDD_CORE_5V		5V IN/5V	PWR	
B22	VDD_CORE_5V		5V IN/5V	PWR	
B23	PE3	E4	DCDC4/3.3V	I/O	
B24	PE11	J7	DCDC4/3.3V	I/O	
B25	PE14	L7	DCDC4/3.3V	I/O	
B26	PJ22	L2	DCDC4/3.3V	I/O	
B27	PL2	AN7	ALDO3/3.3V	I/O	
B28	GND		GND/0V	PWR	
B29	PI2	AL15	DCDC4/3.3V	I/O	

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B30	PI3	AN15	DCDC4/3.3V	I/O	
B31	PI8	AL16	DCDC4/3.3V	I/O	
B32	PI12	AL17	DCDC4/3.3V	I/O	
B33	GND		GND/0V	PWR	
B34	PI9	AM16	DCDC4/3.3V	I/O	
B35	PM0	AN3	BLDO1/3.3V	I/O	
B36	GND		GND/0V	PWR	
B37	GND		GND/0V	PWR	
B38	GND		GND/0V	PWR	
B39	VDD_CORE_5V		5V IN/5V	PWR	
B40	VDD_CORE_5V		5V IN/5V	PWR	
B41	VDD_CORE_5V		5V IN/5V	PWR	
B42	PE13	G6	DCDC4/3.3V	I/O	
B43	PJ21	K2	DCDC4/3.3V	I/O	
B44	PL13	AJ7	ALDO3/3.3V	I/O	
B45	PG6	R6	BLDO1/3.3V	I/O	
B46	PJ24	M3	DCDC4/3.3V	I/O	
B47	PI4	AM15	DCDC4/3.3V	I/O	
B48	PI5	AJ15	DCDC4/3.3V	I/O	
B49	PM5	AL5	BLDO1/3.3V	I/O	
B50	PJ26	N2	DCDC4/3.3V	I/O	
B51	PJ27	N1	DCDC4/3.3V	I/O	
B52	PI14	AM18	DCDC4/3.3V	I/O	
B53	PM3	AM3	BLDO1/3.3V	I/O	
B54	GND		GND/0V	PWR	
B55	GND		GND/0V	PWR	
B56	VDD_CORE_5V		5V IN/5V	PWR	
B57	VDD_CORE_5V		5V IN/5V	PWR	
B58	PJ23	L1	DCDC4/3.3V	I/O	
B59	PL3	AM6	ALDO3/3.3V	I/O	
B60	PG9	U6	BLDO1/3.3V	I/O	
B61	PJ18	N4	BLDO3/1.8V/DCDC4/3.3V	I/O	
B62	PJ19	N5	BLDO3/1.8V/DCDC4/3.3V	I/O	
B63	PM4	AN4	BLDO1/3.3V	I/O	
B64	PL8	AN9	ALDO3/3.3V	I/O	
B65	PL9	AM9	ALDO3/3.3V	I/O	
B66	PI10	AN17	DCDC4/3.3V	I/O	
B67	PM1	AN2	BLDO1/3.3V	I/O	
B68	GND		GND/0V	PWR	
B69	GND		GND/0V	PWR	
B70	GND		GND/0V	PWR	
B71	PG7	R5	BLDO1/3.3V	I/O	
B72	PJ25	M2	DCDC4/3.3V	I/O	

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B73	PJ17	J2	BLDO3/1.8V/DCDC4/3.3V	I/O	
B74	GND		GND/0V	PWR	
B75	CK32K-OUT	AL11	RTC/1.8V	AO	10KΩ pull up
B76	CK24M-OUT	AM14	ALDO4/1.8V	AO	
B77	PE15	N7	DCDC4/3.3V	I/O	
B78	PI13	AK17	DCDC4/3.3V	I/O	
B79	VCC-CARD		CLDO3/3.3V	PWR	
B80	VCC-CARD		CLDO3/3.3V	PWR	
C01	PB9	R28	CLDO3/3.3V	I/O	
C02	PB11	R30	CLDO3/3.3V	I/O	
C03	PB13	R32	CLDO3/3.3V	I/O	
C04	PB1	N29	CLDO3/3.3V	I/O	
C05	GND		GND/0V	PWR	
C06	PD21	L29	DCDC4/3.3V	I/O	
C07	GND		GND/0V	PWR	
C08	GND		GND/0V	PWR	
C09	PB8	P32	CLDO3/3.3V	I/O	
C10	GND		GND/0V	PWR	
C11	PWRON	/	RTC/1.8V	I/O	100Ω in series
C12	GND		GND/0V	PWR	
C13	PD17	J33	BLDO3/1.8V/DCDC4/3.3V	I/O	
C14	PD16	J32	BLDO3/1.8V/DCDC4/3.3V	I/O	
C15	GND		GND/0V	PWR	
C16	PD7	F33	BLDO3/1.8V/DCDC4/3.3V	I/O	
C17	PD6	F32	BLDO3/1.8V/DCDC4/3.3V	I/O	
C18	GND		GND/0V	PWR	
C19	EDP-AUXN	C33	BLDO3/1.8V	I/O	
C20	EDP-AUXP	C32	BLDO3/1.8V	I/O	
C21	EDP-HPD	C29	BLDO3/1.8V	I/O	
C22	EDP-TX3N	B33	BLDO3/1.8V	I/O	
C23	EDP-TX3P	B32	BLDO3/1.8V	I/O	
C24	PB10	R29	CLDO3/3.3V	I/O	
C25	PB12	R31	CLDO3/3.3V	I/O	
C26	PB0	N28	CLDO3/3.3V	I/O	
C27	PB3	M32	CLDO3/3.3V	I/O	
C28	PD23	L32	DCDC4/3.3V	I/O	
C29	GND		GND/0V	PWR	
C30	NC		/	/	
C31	GND		GND/0V	PWR	
C32	PC3	U29	CLDO1/1.8V	I/O	
C33	PC7	W29	CLDO1/1.8V	I/O	
C34	PC12	U33	CLDO1/1.8V	I/O	
C35	PD19	K32	BLDO3/1.8V/DCDC4/3.3V	I/O	

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C36	PD18	K31	BLDO3/1.8V/DCDC4/3.3V	I/O	
C37	GND		GND/0V	PWR	
C38	PD9	G31	BLDO3/1.8V/DCDC4/3.3V	I/O	
C39	PD8	G30	BLDO3/1.8V/DCDC4/3.3V	I/O	
C40	GND		GND/0V	PWR	
C41	PD1	D33	BLDO3/1.8V/DCDC4/3.3V	I/O	
C42	PD0	D32	BLDO3/1.8V/DCDC4/3.3V	I/O	
C43	GND		GND/0V	PWR	
C44	EDP-TX2N	B31	BLDO3/1.8V	I/O	
C45	EDP-TX2P	A31	BLDO3/1.8V	I/O	
C46	PB14	R33	CLDO3/3.3V	I/O	
C47	PB2	M31	CLDO3/3.3V	I/O	
C48	PD22	L31	DCDC4/3.3V	I/O	
C49	PI15	AH17	DCDC4/3.3V	I/O	
C50	PI16	AJ17	DCDC4/3.3V	I/O	
C51	WREQIN	AK13	BLDO1/3.3V	I/O	
C52	PB6	N33	CLDO3/3.3V	I/O	
C53	PC2	U30	CLDO1/1.8V	I/O	
C54	PC4	U28	CLDO1/1.8V	I/O	
C55	AP-NMI	AM10	RTC/1.8V	I/O	1nF pull down 10KΩ pull up
C56	PH11	A16	CLDO3/3.3V	I/O	
C57	PD15	J30	BLDO3/1.8V/DCDC4/3.3V	I/O	
C58	PD14	J29	BLDO3/1.8V/DCDC4/3.3V	I/O	
C59	GND		GND/0V	PWR	
C60	PD3	E31	BLDO3/1.8V/DCDC4/3.3V	I/O	
C61	PD2	E30	BLDO3/1.8V/DCDC4/3.3V	I/O	
C62	GND		GND/0V	PWR	
C63	EDP-TX1N	B30	BLDO3/1.8V	I/O	
C64	EDP-TX1P	A30	BLDO3/1.8V	I/O	
C65	RESET	AJ11	RTC/1.8V	I/O	1nF pull down 10KΩ pull up 100Ω in series
C66	PD20	L28	DCDC4/3.3V	I/O	
C67	GND		GND/0V	PWR	
C68	GND		GND/0V	PWR	
C69	GND		GND/0V	PWR	
C70	PL4	AM7	ALDO3/3.3V	I/O	
C71	PL5	AL7	ALDO3/3.3V	I/O	
C72	GND		GND/0V	PWR	
C73	PH8	D16	CLDO3/3.3V	I/O	
C74	GND		GND/0V	PWR	
C75	GND		GND/0V	PWR	

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C76	PD11	G33	BLDO3/1.8V/DCDC4/3.3V	I/O	
C77	PD10	G32	BLDO3/1.8V/DCDC4/3.3V	I/O	
C78	GND		GND/0V	PWR	
C79	EDP-TX0N	B29	BLDO3/1.8V	I/O	
C80	EDP-TX0P	A29	BLDO3/1.8V	I/O	
C81	GND		GND/0V	PWR	
C82	GND		GND/0V	PWR	
C83	GND		GND/0V	PWR	
C84	PB7	P31	CLDO3/3.3V	I/O	
C85	GND		GND/0V	PWR	
C86	FEL	F16	CLDO3/3.3V	I/O	1nF pull down 100Ω in series
C87	PH19	C13	CLDO3/3.3V	I/O	
C88	PH12	C15	CLDO3/3.3V	I/O	
C89	PD13	H32	BLDO3/1.8V/DCDC4/3.3V	I/O	
C90	PD12	H31	BLDO3/1.8V/DCDC4/3.3V	I/O	
C91	GND		GND/0V	PWR	
C92	PD5	E33	BLDO3/1.8V/DCDC4/3.3V	I/O	
C93	PD4	E32	BLDO3/1.8V/DCDC4/3.3V	I/O	
D01	HTX0P	B27	BLDO3/1.8V	I/O	
D02	HTX0N	C27	BLDO3/1.8V	I/O	
D03	GND		GND/0V	PWR	
D04	HTX2P	B25	BLDO3/1.8V	I/O	
D05	HTX2N	C25	BLDO3/1.8V	I/O	
D06	HHPD	D28	BLDO3/1.8V	I/O	
D07	GND		GND/0V	PWR	
D08	USB0-DP	A24	CLDO3/3.3V	I/O	
D09	USB0-DM	B24	CLDO3/3.3V	I/O	
D10	GND		GND/0V	PWR	
D11	PF2	C19	BLDO3/1.8V/CLDO3/3.3V	I/O	22Ω in series
D12	PF3	B19	BLDO3/1.8V/CLDO3/3.3V	I/O	
D13	PF1	A20	BLDO3/1.8V/CLDO3/3.3V	I/O	
D14	GND		GND/0V	PWR	
D15	PK0	A12	BLDO3/1.8V/DCDC4/3.3V	I/O	
D16	PK1	B12	BLDO3/1.8V/DCDC4/3.3V	I/O	
D17	GND		GND/0V	PWR	
D18	PK4	A10	BLDO3/1.8V/DCDC4/3.3V	I/O	
D19	PK5	B10	BLDO3/1.8V/DCDC4/3.3V	I/O	
D20	GND		GND/0V	PWR	
D21	PK10	E8	BLDO3/1.8V/DCDC4/3.3V	I/O	
D22	PK11	D8	BLDO3/1.8V/DCDC4/3.3V	I/O	
D23	HTX1P	A26	BLDO3/1.8V	I/O	
D24	HTX1N	B26	BLDO3/1.8V	I/O	

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D25	GND		GND/0V	PWR	
D26	HSDA	E26	BLDO3/1.8V	I/O	5V TOL
D27	HSCL	D26	BLDO3/1.8V	I/O	5V TOL
D28	GND		GND/0V	PWR	
D29	USB1-DP	D24	CLDO3/3.3V	I/O	
D30	USB1-DM	E24	CLDO3/3.3V	I/O	
D31	GND		GND/0V	PWR	
D32	PF0	B20	BLDO3/1.8V/CLDO3/3.3V	I/O	
D33	PF5	A18	BLDO3/1.8V/CLDO3/3.3V	I/O	
D34	PH9	C16	CLDO3/3.3V	I/O	
D35	PH10	B16	CLDO3/3.3V	I/O	
D36	GND		GND/0V	PWR	
D37	PK2	B11	BLDO3/1.8V/DCDC4/3.3V	I/O	
D38	PK3	C11	BLDO3/1.8V/DCDC4/3.3V	I/O	
D39	GND		GND/0V	PWR	
D40	PK8	E10	BLDO3/1.8V/DCDC4/3.3V	I/O	
D41	PK9	D10	BLDO3/1.8V/DCDC4/3.3V	I/O	
D42	GND		GND/0V	PWR	
D43	HTXCP	A28	BLDO3/1.8V	I/O	
D44	HTXCN	B28	BLDO3/1.8V	I/O	
D45	GND		GND/0V	PWR	
D46	USB2-DP	D22	DCDC4/3.3V	I/O	
D47	USB2-DM	E22	DCDC4/3.3V	I/O	
D48	GND		GND/0V	PWR	
D49	PF4	B18	BLDO3/1.8V/CLDO3/3.3V	I/O	
D50	PF6	D20	BLDO3/1.8V/CLDO3/3.3V	I/O	
D51	GND		GND/0V	PWR	
D52	PH5	E16	CLDO3/3.3V	I/O	
D53	PH4	B17	CLDO3/3.3V	I/O	
D54	PH18	A14	CLDO3/3.3V	I/O	
D55	GND		GND/0V	PWR	
D56	PK6	E12	BLDO3/1.8V/DCDC4/3.3V	I/O	
D57	PK7	D12	BLDO3/1.8V/DCDC4/3.3V	I/O	
D58	HCEC	E28	BLDO3/1.8V	I/O	5V TOL
D59	PCIE-TX0-DP	A22	BLDO3/1.8V	I/O	
D60	PCIE-TX0-DN	B22	BLDO3/1.8V	I/O	
D61	GND		GND/0V	PWR	
D62	PCIE-RX0-DP	B23	BLDO3/1.8V	I/O	
D63	PCIE-RX0-DN	C23	BLDO3/1.8V	I/O	
D64	GND		GND/0V	PWR	
D65	PH16	B14	CLDO3/3.3V	I/O	
D66	PH1	E18	CLDO3/3.3V	I/O	
D67	PH2	D18	CLDO3/3.3V	I/O	

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D68	PH7	F14	CLDO3/3.3V	I/O	
D69	PH17	B13	CLDO3/3.3V	I/O	
D70	PH6	G12	CLDO3/3.3V	I/O	
D71	GND		GND/0V	PWR	
D72	GND		GND/0V	PWR	
D73	PCIE-CLKP	B21	BLDO3/1.8V	I/O	100nF in series
D74	PCIE-CLKN	C21	BLDO3/1.8V	I/O	100nF in series
D75	GND		GND/0V	PWR	
D76	PH0	F18	CLDO3/3.3V	I/O	
D77	PH15	D14	CLDO3/3.3V	I/O	
D78	PH14	E14	CLDO3/3.3V	I/O	
D79	PH13	B15	CLDO3/3.3V	I/O	
D80	PH3	C17	CLDO3/3.3V	I/O	
E01	GND		GND/0V	PWR	
E02	GND		GND/0V	PWR	
E03	GND		GND/0V	PWR	
E04	GND		GND/0V	PWR	
E05	GND		GND/0V	PWR	
E06	GND		GND/0V	PWR	
E07	GND		GND/0V	PWR	
E08	GND		GND/0V	PWR	
E09	GND		GND/0V	PWR	
E10	GND		GND/0V	PWR	
E11	GND		GND/0V	PWR	
E12	GND		GND/0V	PWR	
E13	GND		GND/0V	PWR	
E14	GND		GND/0V	PWR	
E15	GND		GND/0V	PWR	
E16	GND		GND/0V	PWR	
E17	GND		GND/0V	PWR	
E18	GND		GND/0V	PWR	
E19	GND		GND/0V	PWR	
E20	GND		GND/0V	PWR	
E21	GND		GND/0V	PWR	
E22	GND		GND/0V	PWR	
E23	GND		GND/0V	PWR	
E24	GND		GND/0V	PWR	
E25	GND		GND/0V	PWR	
E26	GND		GND/0V	PWR	
E27	GND		GND/0V	PWR	
E28	GND		GND/0V	PWR	
E29	GND		GND/0V	PWR	
E30	GND		GND/0V	PWR	

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E31	GND		GND/0V	PWR	
E32	GND		GND/0V	PWR	
E33	GND		GND/0V	PWR	
E34	GND		GND/0V	PWR	
E35	GND		GND/0V	PWR	

Note:

- AI: analog input;
- AO: analog output;
- DI: digital input;
- DO: digital output;
- I/O: digital input and output;
- PWR: power supply;
- The unit of trace length is mil;
- For detailed LGA pin multiplexing functions, please refer to the "ECK32-T527B Pin List" file.

4.3.3. I/O Impedance Control

All high-speed signals of the ECK32-T527B series core board have impedance control and length control during PCB design. The impedance control parameters of the core board traces are shown in the table below.

Trace impedance control table

Serial number	Impedance Controlled Routing Classification	Impedance Control	Typical Model Network Name
1	USB differential signaling	90±10%Ω	USB0-DP / USB0-DM
2	PCIe differential signaling	100±10%Ω	PCIE-RX0-DP/PCIE-RX0-DN
3	EDP differential signal	100±10%Ω	EDP-TX0P /EDP-TX0N
4	HDMI differential signal	100±10%Ω	HTX0P /HTX0N
5	LVDS, MIPI differential signal	100±10%Ω	LVDS0-D0P /LVDS0-D0N
6	General single-ended routing	50±10%Ω	

4.4.Electrical Characteristics

4.4.1. Power consumption

Note: The following parameters are measured on the ECK32-T527BN4E32-I core board on

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the ECB32-PGBN4E32-I single-board computer at room temperature. The measured power consumption does not include the baseboard power consumption. The measurement was run on the eMMC with the Debian system, the stress-ng test program running when the power consumption was heavy, HDMI display, no baseboard TF card access, and connected to a Gigabit network. Factors such as test methods, usage functions, and ambient temperature will affect power consumption. The following power consumption data is for reference only.

Power Consumption Table

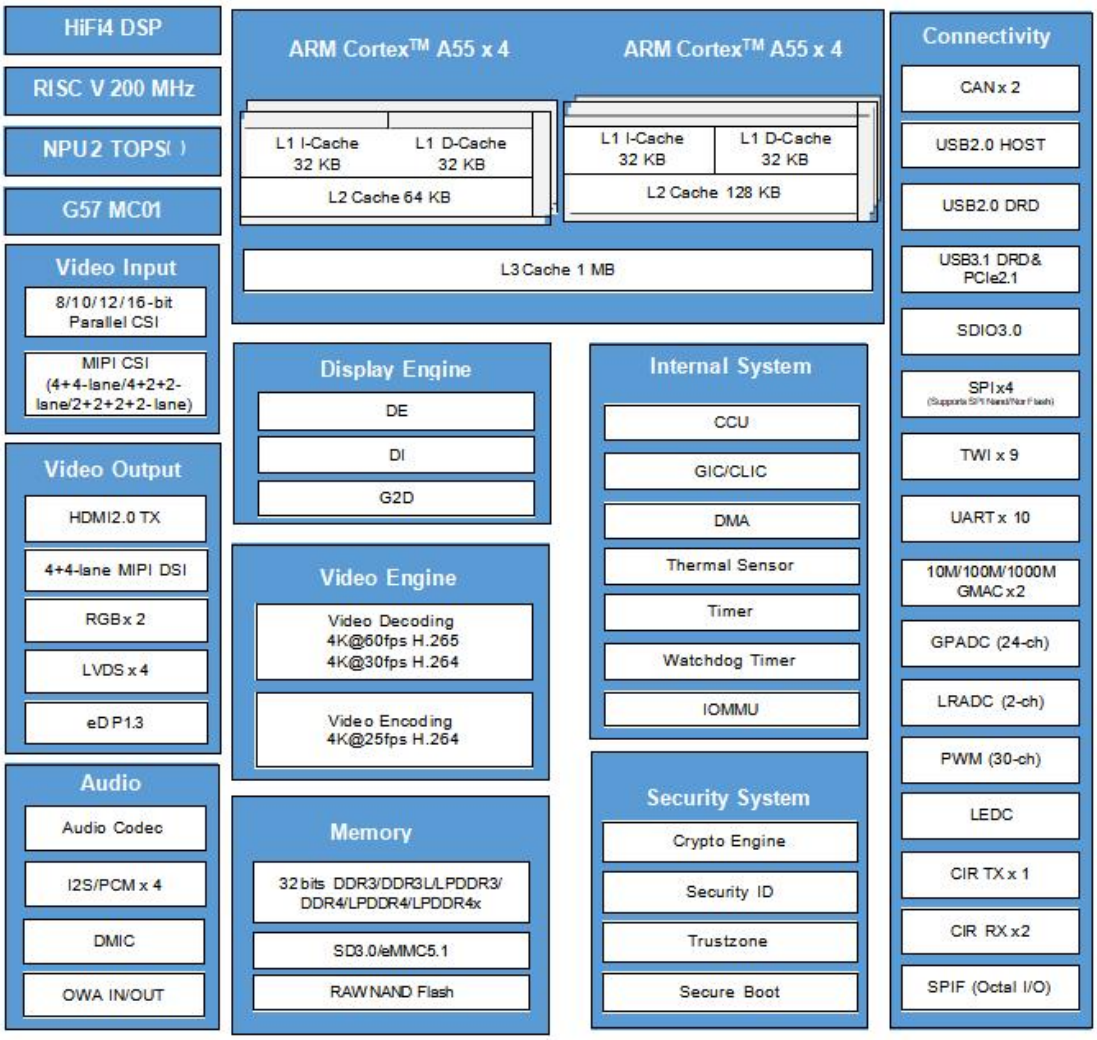
Power Status	Test environment	Supply voltage	Current	Power consumption
BOOT	UBOOT is running	5 V	0.278 A	1.39 W
PWRUP	Entering the system without running the application	5 V	0.318 A	1.59 W
PWRUP	Software reload testing	5 V	1.378 A	6.89 W
SLEEP	Freeze mode hibernation	5 V	0.137 A	0.685 W
SLEEP	mem mode sleep state	5 V	0.009 A	0.045 W
PWROFF	Software shutdown	5 V	0 A	0

5. Core board hardware design

5.1.processor

The Allwinner T527 series processor used in the ECK32-T527B series core board is a high-performance octa-core Cortex-A55 AI platform SOC product suitable for commercial, industrial and automotive fields. The functional block diagram of the T527 series processor is shown in the figure below.

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T527 system functional block diagram

5.2.Memory

The ECK32-T527B series core board has one LPDDR4 SDRAM memory chip mounted o n the board. It is designed with a 32-bit memory data width and currently provides two capaci ties of 2GB and 4GB. The design memory can use domestic industrial-grade or domestic wide -temperature devices. The memory chip models are shown in the table below.

Memory chip selection table

factory	model	Single chip capacity	Operating temperature
YEESTOR	SGG1G32F5EI-S02	32Gbit	-40℃ ~ 95 ℃
YEESTOR	SGG512M32F5EI-S07	16Gbit	-40℃ ~ 95 ℃
Longsys	FLXC2004G-N1	16Gbit	-25 ℃ ~ 85 ℃

Note: The specific model of the mounted memory chip shall be subject to the actual product.

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5.3.clock

The ECK32-T527B series core board provides one 32.768KHz crystal (passive) oscillator circuit and one 24MHz crystal (passive) oscillator circuit as the processor system clock source. The crystal oscillator devices are all domestically produced industrial-grade crystal oscillators.

5.4.storage

The ECK32-T527B series core board has two storage media designed on the board. One is the eMMC storage medium. This storage medium has the characteristics of large storage capacity, low unit storage cost, fast read and write speed and easy use. The other storage medium is EEPROM, which is connected to the I2C bus. This storage medium has high reliability and is easy to use and can be used as user parameter storage. Both storage media are installed by default and do not need to be selected.

The ECK32-T527B series core board eMMC memory is connected to the processor through the SMHC2 (SDC2) bus, supports 150MHz HS400 mode, and the maximum read speed can reach 232MB/s. The device uses domestic industrial-grade or wide-temperature eMMC storage chips.

The ECK32-T527B series core board EEPROM chip is connected to the processor through the TWI1 (I2C1) bus. The storage chip uses domestic industrial-grade EEPROM with a maximum capacity of 32Kbit.

The ECK32-T527B series core board storage chip models are shown in the table below.

Memory chip selection table

factory	model	capacity	Operating temperature
Longsys	FEMDRW032G-88A19	32GB	-40℃ ~ 85 ℃
Longsys	FEMDRW016G-88A43	16 GB	-40℃ ~ 85 ℃
YEESTOR	SGM8200C-S32BBG	32GB	-25 ℃ ~ 85 ℃
FMD	FT24C32A	32Kb	-40℃ ~ 85 ℃

Note: The specific model of the mounted memory chip shall be subject to the actual product.

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5.5.power supply

The ECK32-T527B series core board adopts the original PMIC power supply solution and is designed strictly in accordance with the voltage, power and timing requirements in the T527 manual. The selected PMIC solution chip models are: AXP717B and AXP323. The ECK32-T527B series core board is powered by a single DC +5V power supply. Only one VDD_CORE_5V power input is required externally. Other power supplies are generated internally by the core board, and no additional power supply is required, which greatly simplifies the difficulty of user power supply design.

The ECK32-T527B series core board also provides a power output VCC-CARD. This power supply is derived from the PMIC chip CLDO3, with a default operating voltage of 3.3V and a maximum output current of 500mA. It can be used to power low-power devices on the baseboard and control the power-on timing of the baseboard I/O interface.

5.5.1. Core board power-on timing

The power supply and I/O interface of the ECK32-T527B series core board are roughly divided into 4 stages:

Core board power supply and signal power-on timing table

Power-on stage	power supply	time
RANK 1	Power on the core board with 5V power supply	0ms
RANK 2	RTC, ALDO4, CLDO1, CLDO3, ALDO3,	20ms
RANK 3	RESET	70ms
RANK 4	BLDO1, BLDO3, DCDC4	700ms

5.5.2. I/O power status when the core board is in sleep mode

When the E CK32-T527B series core board is in sleep mode, only the following power I/Os are powered, so the core board can only be woken up through the GPIO on the PL.

I/O power status table when the core board is in sleep mode

power supply	Voltage	Typical I/O
RTC	1.8V	RESET、PWRON
ALDO3	3.3V	PL

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5.5.3. Core board I/O interface power rail

The ECK32-T527B series is mainly divided into two stages. The first stage is that th e core board PMIC automatically turns on the power supply (RANK1) after the 5V input power supply is valid; the second stage is that the PMIC is turned off by default and the power supply is turned on after the software is started (RANK4).

I/O Power Rails and Power-Up Sequencing

Pin Name	Power Rail	Voltage	Rank
VDD_CORE_5V	5V IN	5V	RANK 0
AP-NMI , PWRON , RESET	RTC	1.8V	RANK 1
FEL , MBIAS , USB , PB , PH , VCC-CARD	CLDO3	3.3V	RANK 1
PC	CLDO1	1.8V	RANK 1
PF	BLDO3/CLDO3	1.8V/3.3V	RANK 1
CK24M-OUT , HDMI-DET , LRADC , GPADC , LINEOUT , MIC	ALDO4	1.8V	RANK 1
PL	ALDO3	3.3V	RANK 1
PE 、 PI	DCDC4	3.3V	RANK 4
PD , PJ , PK	BLDO3/DCDC4	1.8V/3.3V	RANK 4
EDP , HDMI , HEADPHONE , PCIE	BLDO3	1.8V	RANK 4
CK32K-OUT , PG , PM , WREQIN	BLDO1	3.3 V	RANK 4

5.6.On-board I/O assignment

Some functions on the ECK32-T527B series core board occupy the I/O functions of the T 527 processor. These I/O functions are not brought out to the LGA pins. Users should pay att ention to the function configuration of these I/Os when configuring the software. The specific occupied I/Os are shown in the following table.

Core board multiplexing I/O allocation table

MPU Pin	GPIO	Function
AN6	PL0	PMU-SCK
AN5	PL1	PMU-SDA
W28	PC0	eMMC-DS
Y31	PC1	eMMC-RST
Y32	PC5	eMMC-CLK
W33	PC6	eMMC-CMD
W32	PC8	eMMC-D3
W31	PC9	eMMC-D4
V32	PC10	eMMC-D0
V31	PC11	eMMC-D5

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U32	PC13	eMMC-D1
U31	PC14	eMMC-D6
T32	PC15	eMMC-D2
T31	PC16	eMMC-D7
N31	PB4	TWI1-SCK
N32	PB5	TWI1-SDA

6. Baseboard hardware design

6.1.Power interface

For embedded product design, the design of the power supply system is crucial. It is necessary to consider not only the basic electrical parameters of the power supply itself, but also various factors such as the stability design and timing design of the power supply. The ECK32-T527B series core board has integrated complex power management and hardware circuits into the core board. The core board adopts a single power supply solution and provides power timing management signals to simplify the user's baseboard power supply design as much as possible.

6.1.1. Power Input

The ECK32-T527B series core board is powered by a single DC +5V power supply, and the power input pin is named VDD_CORE_5V. The power supply voltage range is 5.0V±10%. The typical power consumption of the ECK32-T527B series core board is about 6 W. When designing the power supply for the core board, the baseboard should consider the I/O output power consumption and the increased power consumption when more functions are running at the same time, and the increased power consumption of components at high temperature. Therefore, it is recommended that the core board power supply current design should not be less than 2 A.

The core board is powered by a DC-DC power supply, and the power margin should not be too large when designing the power supply. If the power design is too large, many power supplies will work in discontinuous PWM mode to ensure conversion efficiency, and the output power ripple will increase significantly, which is not conducive to the working stability of the digital signal system.

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6.1.2. Power Output

The ECK32-T527B series core board also provides 1 power output pin named VCC-CARD, which can be used to power low-power devices on the baseboard or control the power-on timing of the baseboard I/O interface.

6.1.3. Backplane Power Sequencing

The power sequence control of the baseboard mainly considers the power-on sequence of the core board I/O. The I/O interface of the ECK32-T527B series core board is mainly powered on in two stages. The first stage is the power automatically turned on by the core board PMIC after the 5V input power is valid; the second stage is the power turned on by the PMIC by default after the software is started. To ensure that the baseboard does not cause leakage current to the core board I/O interface, a simple way is to power on all I/O interface power supplies connected to the baseboard and the core board after the core board I/O is powered on (that is, after the core board software is configured to turn on all I/O power supplies). You can use an I/O on the core board PE or PI (for example, PE15) to control the power on of the baseboard I/O interface. For I/O interfaces that need to be powered on before the software works (such as SD card interfaces and debug serial ports), if the power is small, you can directly use the VCC-CARD power supply. If the power is large, you can use the power supply controlled by VCC-CARD.

6.2.Launch Configuration

6.2.1. Boot order configuration

When the ECK32-T527B series core board starts, the processor will read the status of BOOT_Select and select the order of enumerating media. BOOT_Select has a fixed configuration status on the core board, and the default startup sequence is: SMHC0->EMMC_BOOT->EMMC_USER->try (except SPI in PJ)

6.2.2. FEL pin

The ECK32-T527B series core board supports the firmware forced burning pin FEL. When the ECK32-T527B series core board is not powered on, the FEL signal is grounded. After power-on, the FEL is released, and the ECK32-T527B series core board will enter the firmware

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upgrade mode. Users can design buttons or jumpers on the baseboard to ground the FEL signal to force the processor to enter the firmware upgrade mode. Since the signal has been designed with a pull-up resistor on the core board, the baseboard design only needs to consider grounding and appropriate TVS protection. Do not arbitrarily design a pull-up resistor for the FEL signal on the baseboard. If the FEL signal is not used, the signal can be left floating and the firmware can be upgraded through the SD card.

6.2.3. Pin Definition

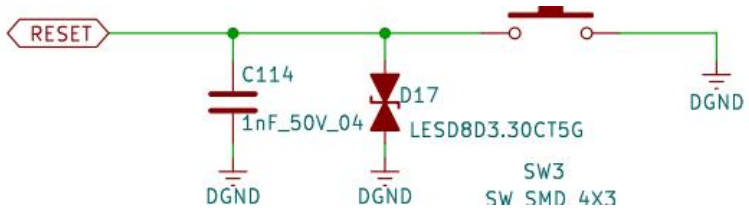
Startup configuration pin definition table

LGA	Pin Name	MPU	Power Rail	Type	Length	Comment
C86	FEL	F16	CLDO3/3.3V	I/O		1nF pull down 100Ω in series

6.3.Reset button

The RESET signal from the ECK32-T527B series core board can be connected to an external button to achieve reset control of the processor. The RESET signal is an input-output bidirectional signal. It can be used as an external reset input to reset the processor. It is also the internal power reset signal output of the processor. The RESET signal provides a 10K ohm pull-up resistor in the core board. Therefore, in the baseboard application, when the RESET signal is used as a manual reset input, do not connect the pull-up resistor, directly connect the button, or drive it through the OD gate. Do not drive the RESET signal through the push-pull output interface. When connecting the manual input button, you can place a small capacitor (capacitance value not greater than 1nF) and TVS to reduce interference and improve ESD performance. The button reference schematic is shown in the figure below.

6.3.1. References



Button reference schematic

Note: Do not pull up the reset and power button signals through resistors at will. If the pull-up power rail is incorrect, it will cause uncertain signals to be input to the button signal i

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nterface when the system is in standby or shutdown.

6.3.2. Pin Definition

Button pin definition table

LGA	Pin Name	MPU	Power Rail	Type	Length	Comment
C65	RESET	AJ11	RTC/1.8V	I/O		1nF pull down 10KΩ pull up 100Ω in series

6.3.3. LAYOUT SUGGESTIONS

- The reset signal is a sensitive signal and can be processed in a package or away fro m signals with greater interference ;
- Place the reset signal TVS tube as close to the button as possible.

6.4.Reference Clock and NMI

The ECK32-T527B series core board provides 2 clock output signals. One is 24MHz cloc k output CK24M-OUT, and the other is 32.768KHz clock output CK32K-OUT. Both clock out puts can be used for Wi-Fi modules. Note: CK32K-OUT here is the PM power domain.

6.4.1. REFCLK_OUT

The processor DCXO clock module can fan out a clock signal with the same frequency a s the main clock through the REFCLK_OUT_J2 pin. This clock signal can be provided to the devices on the baseboard as clock input, such as the Wi-Fi module. When using this clock re ference output, consider whether the clock level, accuracy, and power-on sequence are suitable for the baseboard device. If not, it is recommended not to use this clock signal.

6.4.2. NMI

Processor non-maskable interrupt signal, mainly used for PMIC management. This pin func tion is not recommended for users to use. It can be left floating when not in use.

6.4.3. Pin Definition

Button pin definition table

LGA	Pin Name	MPU	Power Rail	Type	Length	Comment
C55	AP-NMI	AM10	RTC / 1.8V	I/O		1nF pull down 10KΩ pull up
B76	CK24M-OUT	AM14	ALDO4/1.8V	AO		

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B75	CK32K-OUT	AL11	BLDO1/3.3V	AO		10KΩ pull up

6.5.Display interface

The ECK32-T527B series core board supports four interface LCD screens: RGB, LVDS, MIPI-DSI, and EDP. When designing a product, please select the corresponding interface accor ding to the specific LCD specifications.

Interface information of each display screen

LCD Interface	Maximum supported resolution
Single-Link LVDS	1366x768@60Hz
Dual-Link LVDS	1920x1080@60Hz
Single-Link MIPI DSI	1920x1080@60Hz
Dual-Link MIPI DSI	2560x1600@60Hz or 4K@45Hz
eDP	2.5K@60Hz
RGB888	1920x1080@60Hz

- When the PD and PJ ports are used as ordinary GPIOs, the LVDS and MIPI DSI modul es need to be turned off. Otherwise, the LVDS/MIPI-DSI and GPIO will be output togeth er, affecting the GPIO output level.
- Make sure that the MIPI or LVDS interface signal differential pairs between the AP and LCD are correctly connected, and the positive and negative terminals cannot be reversed.
- The LCD backlight IC needs to be designed according to the specific LCD specifications. PWM dimming is used by default. When using PWM dimming, please note that the PW M frequency needs to be greater than 20KHz, otherwise inductor howling will occur.
- Please confirm whether the IO voltage of LCD is consistent with the control IO voltage of AP. If not, please make sure to do level matching, such as LCD-RST signal.
- The differential line length of MIPI DSI should be less than 2000 mil, and the reference plane of the line should be kept intact as much as possible.
- A 100nF capacitor needs to be connected in series to eDP TXN/P and AUXN/P.
- The LCD display interface recommends using the 18-bit color signal on the PD pin. Thes e signals are all on a set of I/Os, which is convenient for controlling the trace length an d operating level. When the PD pin is configured as LVDS or DSI function, it automatic

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ally switches to 1.8V level. When configured as GPIO or LCD function, it automatically switches to 3.3V level.

6.5.1. Interface Definition

LCD0/LVDS0/1DSI0/1 Interface Definition Table

LGA	Name	MPU	Power Rail	Type	Length	Comment
C42	PD0	D32	BLDO3/1.8V/DCDC4/3.3V	I/O	862.95	LCD0-D2/LVDS0-D0P/DSI0-D0P
C41	PD1	D33	BLDO3/1.8V/DCDC4/3.3V	I/O	863.13	LCD0-D3/LVDS0-D0N/DSI0-D0N
C61	PD2	E30	BLDO3/1.8V/DCDC4/3.3V	I/O	884.93	LCD0-D4/LVDS0-D1P/DSI0-D1P
C60	PD3	E31	BLDO3/1.8V/DCDC4/3.3V	I/O	884.31	LCD0-D5/LVDS0-D1N/DSI0-D1N
C93	PD4	E32	BLDO3/1.8V/DCDC4/3.3V	I/O	857.61	LCD0-D6/LVDS0-D2P/DSI0-CKP
C92	PD5	E33	BLDO3/1.8V/DCDC4/3.3V	I/O	858.96	LCD0-D7/LVDS0-D2N/DSI0-CKN
C17	PD6	F32	BLDO3/1.8V/DCDC4/3.3V	I/O	869.05	LCD0-D10/LVDS0-CKP/DSI0-D2P
C16	PD7	F33	BLDO3/1.8V/DCDC4/3.3V	I/O	869.99	LCD0-D11/LVDS0-CKN/DSI0-D2N
C39	PD8	G30	BLDO3/1.8V/DCDC4/3.3V	I/O	856.68	LCD0-D12/LVDS0-D3P/DSI0-D3P
C38	PD9	G31	BLDO3/1.8V/DCDC4/3.3V	I/O	856.84	LCD0-D13/LVDS0-D3N/DSI0-D3N
C77	PD10	G32	BLDO3/1.8V/DCDC4/3.3V	I/O	855.65	LCD0-D14/LVDS1-D0P/DSI1-D0P
C76	PD11	G33	BLDO3/1.8V/DCDC4/3.3V	I/O	856.31	LCD0-D15/LVDS1-D0N/DSI1-D0N
C90	PD12	H31	BLDO3/1.8V/DCDC4/3.3V	I/O	915.06	LCD0-D18/LVDS1-D1P/DSI1-D1P
C89	PD13	H32	BLDO3/1.8V/DCDC4/3.3V	I/O	916.57	LCD0-D19/LVDS1-D1N/DSI1-D1N
C58	PD14	J29	BLDO3/1.8V/DCDC4/3.3V	I/O	871.29	LCD0-D20/LVDS1-D2P/DSI1-CKP
C57	PD15	J30	BLDO3/1.8V/DCDC4/3.3V	I/O	872.15	LCD0-D21/LVDS1-D2N/DSI1-CKN
C14	PD16	J32	BLDO3/1.8V/DCDC4/3.3V	I/O	952.17	LCD0-D22/LVDS1-CKP/DSI1-D2P
C13	PD17	J33	BLDO3/1.8V/DCDC4/3.3V	I/O	952.73	LCD0-D23/LVDS1-CKN/DSI1-D2N

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C36	PD18	K31	BLDO3/1.8V/DCDC4/3.3V	I/O	957.25	LCD0-CLK/LVDS1-D3P/DSI1-D3P
C35	PD19	K32	BLDO3/1.8V/DCDC4/3.3V	I/O	955.26	LCD0-DE/LVDS1-D3N/DSI1-D3N
C66	PD20	L28	DCDC4/3.3V	I/O		LCD0-HSYNC
C06	PD21	L29	DCDC4/3.3V	I/O		LCD0-VSYNC

EDP Interface Definition Table

LGA	Pin Name	MPU	Power Rail	Type	Length	Comment
C19	EDP-AUXN	C33	BLDO3/1.8V	I/O	836.16	EDP-AUXN
C20	EDP-AUXP	C32	BLDO3/1.8V	I/O	837.4	EDP-AUXP
C21	EDP-HPD	C29	BLDO3/1.8V	I/O		EDP-HPD
C79	EDP-TX0N	B29	BLDO3/1.8V	I/O	855.76	EDP-TX0N
C80	EDP-TX0P	A29	BLDO3/1.8V	I/O	856.57	EDP-TX0P
C63	EDP-TX1N	B30	BLDO3/1.8V	I/O	868.3	EDP-TX1N
C64	EDP-TX1P	A30	BLDO3/1.8V	I/O	866.48	EDP-TX1P
C44	EDP-TX2N	B31	BLDO3/1.8V	I/O	759.37	EDP-TX2N
C45	EDP-TX2P	A31	BLDO3/1.8V	I/O	757.39	EDP-TX2P
C22	EDP-TX3N	B33	BLDO3/1.8V	I/O	859.52	EDP-TX3N
C23	EDP-TX3P	B32	BLDO3/1.8V	I/O	861.31	EDP-TX3P

6.5.2. LAYOUT SUGGESTIONS

- LCD signal routing should be of equal length, with the length within the group controlled within 500mil and single-ended impedance of 50 ohms. Pay attention to the crosstalk of LCD clock signal and keep a certain distance from other signals.
- The single-ended impedance of the LVDS signal is 50 ohms, the differential impedance is 100 ohms, the line length difference within the differential pair is less than 10 mil, and the line length difference within the group is less than 100 mil;
- The single-ended impedance of the MIPI DSI signal is 50 ohms, the differential impedance is 100 ohms, the line length difference within the differential pair is less than 10 mil, and the line length difference within the group is less than 100 mil;
- The differential impedance of EDP signal is 100 ohms, the difference in the length of the trace within the differential pair is less than 10 mil, and there is no special requirement for the difference in the length of the trace within the group;

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❖ The reference plane for the displayed signal routing should be complete, the routing should not cross the division , and the signal line spacing should be at least 2W.

6.6.Display interface

The ECK32-T527B series core board provides a dedicated HDMI display interface, supporting HDMI 2.0 and HDCP1.4 protocols, and supports up to 4K@60fps 2D display or 4K@30fps 3D display.

The I2C and CEC pins of the ECK32-T527B series core board HDMI have built-in Level shift circuits. They are 5V voltage-resistant pins and support direct connection to the device without the need for an external level conversion chip.

The 5V power supply of HDMI must be connected in series with a Schottky diode to prevent leakage at the device end after shutdown. Because the voltage drop of ordinary diodes is high, it is easy to cause the power supply of HDMI to be lower than 4.75V. To avoid compatibility issues, please choose a Schottky diode with a low on-state voltage drop.

6.6.1. Interface Definition

HDMI Interface Definition Table

LGA	Pin Name	MPU	Power Rail	Type	Length	Comment
D58	HCEC	E28	BLDO3/1.8V	I/O		HCEC
D06	HHPD	D28	BLDO3/1.8V	I/O		HHPD
A73	HP-DET	AJ2	ALDO4/1.8V	AI		HP-DET
D27	HSCL	D26	BLDO3/1.8V	I/O		HSCL
D26	HSDA	E26	BLDO3/1.8V	I/O		HSDA
D02	HTX0N	C27	BLDO3/1.8V	I/O	969.62	HTX0N
D01	HTX0P	B27	BLDO3/1.8V	I/O	971.6	HTX0P
D24	HTX1N	B26	BLDO3/1.8V	I/O	971.97	HTX1N
D23	HTX1P	A26	BLDO3/1.8V	I/O	971.48	HTX1P
D05	HTX2N	C25	BLDO3/1.8V	I/O	973.13	HTX2N
D04	HTX2P	B25	BLDO3/1.8V	I/O	973.35	HTX2P
D44	HTXCN	B28	BLDO3/1.8V	I/O	964.57	HTXCN
D43	HTXCP	A28	BLDO3/1.8V	I/O	964.08	HTXCP

6.6.2. LAYOUT SUGGESTIONS

❖ The differential impedance of HDMI signal is 100 ohms, the difference in the length of the line within the differential pair is less than 10 mil, the difference in the length of the line within the group is less than 200 mil, and the longest length of the line should be

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less than 2000 mil;

- The ESD device is close to the HDMI socket, and the distance from the ESD device to the HDMI connector is less than or equal to 500 mil ;
- The reference plane for the displayed signal routing should be complete, the routing should not cross the division , and the signal line spacing should be at least 2W.

6.7.Camera interface

- The ECK32-T527B series core board supports two 4-lane MIPI-CSI interfaces and one 16-bit parallel NCSI interface.
- The ECK32-T527B series core board can support the simultaneous access and processing of 6-channel camera data . It is recommended to use the MIPI-CSI interface to access no more than 4-channel camera data .
- The MIPI-CSI interface supports up to 8M@30fps input;
- The NCSI interface supports 8-bit DVP interface, BT1120 interface, BT656 interface and BT601 interface input. The parallel NCSI interface can support a maximum pixel clock of 148.5MHz, and the BT656 interface can support 4*720P@30fps input in clock double-edge sampling mode.
- MCSIA and MCSIB, MCSIC and MCSID can be combined into 4-lane.
- When MCSIA and MCSIB are used as 4-lane, the CLK of MCSIA must be used. The CLK of MCSIB can be left floating or used as a normal IO. MCSIA0, MCSIA1, MCSIB0, and MCSIB1 correspond to MCSI0/1/2/3 respectively.
- When MCSIC and MCSID are used as 4-lane, the CLK of MCSIC must be used. The CLK of MCSID can be left floating or used as a normal IO. MCSIC0, MCSIC1, MCSID0, and MCSID1 correspond to MCSI0/1/2/3 respectively.
- It is recommended to use PK group I/O to implement the CSI interface. When the I/O is configured as MIPI-CSI function, it automatically switches to 1.8V level. When the I/O is configured as NCSI or GPIO function, it automatically switches to 3.3V level.

6.7.1. Interface Definition

MCSI/NCSI interface definition table

LGA	Pin Name	MPU	Power Rail	Type	Length	Comment

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D15	PK0	A12	BLDO3/1.8V/DCDC4/3.3V	I/O	504.97	MCSIA-D0N
D16	PK1	B12	BLDO3/1.8V/DCDC4/3.3V	I/O	504.43	MCSIA-D0P
D37	PK2	B11	BLDO3/1.8V/DCDC4/3.3V	I/O	600.3	MCSIA-D1N
D38	PK3	C11	BLDO3/1.8V/DCDC4/3.3V	I/O	602.08	MCSIA-D1P
D18	PK4	A10	BLDO3/1.8V/DCDC4/3.3V	I/O	586.36	MCSIA-CKN
D19	PK5	B10	BLDO3/1.8V/DCDC4/3.3V	I/O	587.37	MCSIA-CKP
D56	PK6	E12	BLDO3/1.8V/DCDC4/3.3V	I/O	725.23	MCSIB-D0N
D57	PK7	D12	BLDO3/1.8V/DCDC4/3.3V	I/O	726.84	MCSIB-D0P
D40	PK8	E10	BLDO3/1.8V/DCDC4/3.3V	I/O	725.15	MCSIB-D1N
D41	PK9	D10	BLDO3/1.8V/DCDC4/3.3V	I/O	723.19	MCSIB-D1P
D21	PK10	E8	BLDO3/1.8V/DCDC4/3.3V	I/O	809.57	MCSIB-CKN
D22	PK11	D8	BLDO3/1.8V/DCDC4/3.3V	I/O	811	MCSIB-CKP
A02	PK12	B9	BLDO3/1.8V/DCDC4/3.3V	I/O	1006.84	MCSIC-D0N/NCSI-PCLK
A01	PK13	C9	BLDO3/1.8V/DCDC4/3.3V	I/O	1008.65	MCSIC-D0P/NCSI-MCLK
A25	PK14	A8	BLDO3/1.8V/DCDC4/3.3V	I/O	917.76	MCSIC-D1N/NCSI-HS
A24	PK15	B8	BLDO3/1.8V/DCDC4/3.3V	I/O	917.58	MCSIC-D1P/NCSI-VS
A47	PK16	B7	BLDO3/1.8V/DCDC4/3.3V	I/O	912.35	MCSIC-CKN/NCSI-D0
A46	PK17	C7	BLDO3/1.8V/DCDC4/3.3V	I/O	910.67	MCSIC-CKP/NCSI-D1
A05	PK18	A6	BLDO3/1.8V/DCDC4/3.3V	I/O	655.39	MCSID-D0N/NCSI-D2
A04	PK19	B6	BLDO3/1.8V/DCDC4/3.3V	I/O	655.99	MCSID-D0P/NCSI-D3
A28	PK20	A5	BLDO3/1.8V/DCDC4/3.3V	I/O	557.5	MCSID-D1N/NCSI-D4
A27	PK21	B5	BLDO3/1.8V/DCDC4/3.3V	I/O	557.67	MCSID-D1P/NCSI-D5
A66	PK22	A4	BLDO3/1.8V/DCDC4/3.3V	I/O	562.63	MCSID-CKN/NCSI-D6
A65	PK23	B4	BLDO3/1.8V/DCDC4/3.3V	I/O	561.36	MCSID-CKP/NCSI-D7

6.7.2. LAYOUT SUGGESTIONS

- The differential impedance of MIPI-CSI signals is 100 ohms, the difference in the length of the traces within the differential pair is less than 10 mil, and the difference in the len gth of the traces within the group is less than 300 mil;
- The NCSI signal routing should be of equal length. The length within the group can be c ontrolled within 500mil, and the single-ended impedance is 50 ohms. Pay attention to the crosstalk of the clock signal and keep a certain distance from other signals.
- The length of the MIPI CSI differential line should be less than 3000 mil, and the refere nce plane of the line should be kept intact as much as possible.

6.8.PCIe interface

The ECK32-T527B series core board supports a set of PCIE2.1 x1 lane, 5Gbps/lane, multi

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plexed with USB3.1 interface IO, supports RC mode, supports dual virtual channels, 8 inbound windows and 8 outbound windows and message signaled interrupts.

When using the PCIE interface, you need to connect the three signals PERSTn, WAKEN, and CLKREQN. These three signals are fixedly multiplexed in PG2, PG3, PG4 and PH11, P H12, PH19. When using PCIE, you can multiplex from one of the groups.

A 100nF capacitor needs to be connected in series on the PCIE interface TXP/N (PCIE-C LKP/N has already been connected in series with a capacitor in the core). When using PCIE a s an inter-board connection, please place this capacitor close to the PCIE connector on the tra nsmitting end; when using PCIE as an intra-board CHIP TO CHIP interconnection, please plac e this capacitor close to the transmitting end device. When the PCIE interface is not used, it i s recommended to ground the PCIE-CLKP/N signal.

6.8.1. Pin Definition

PCIe Interface Definition Table

LGA	Pin Name	MPU	Power Rail	Type	Length	Comment
D74	PCIE-CLKN	C21	BLDO3/1.8V	I/O	355.38	PCIE-CLKN
D73	PCIE-CLKP	B21	BLDO3/1.8V	I/O	355.64	PCIE-CLKP
D63	PCIE-RX0-DN	C23	BLDO3/1.8V	I/O	341.68	PCIE-RX0-DN
D62	PCIE-RX0-DP	B23	BLDO3/1.8V	I/O	340.98	PCIE-RX0-DP
D60	PCIE-TX0-DN	B22	BLDO3/1.8V	I/O	1102.29	PCIE-TX0-DN
D59	PCIE-TX0-DP	A22	BLDO3/1.8V	I/O	1100.36	PCIE-TX0-DP

6.8.2. LAYOUT SUGGESTIONS

- The PCIe signal differential impedance is 100 ohms, the line length difference within the differential pair is less than 10 mil, and there is no special requirement for the line lengt h difference within the group;
- PCIe signal routing should reduce the number of via layer switching, the signal routing le ngth should be controlled within 5000Mil, and the routing should avoid crossing plane lay er splits.

6.9.SD/MMC card interface

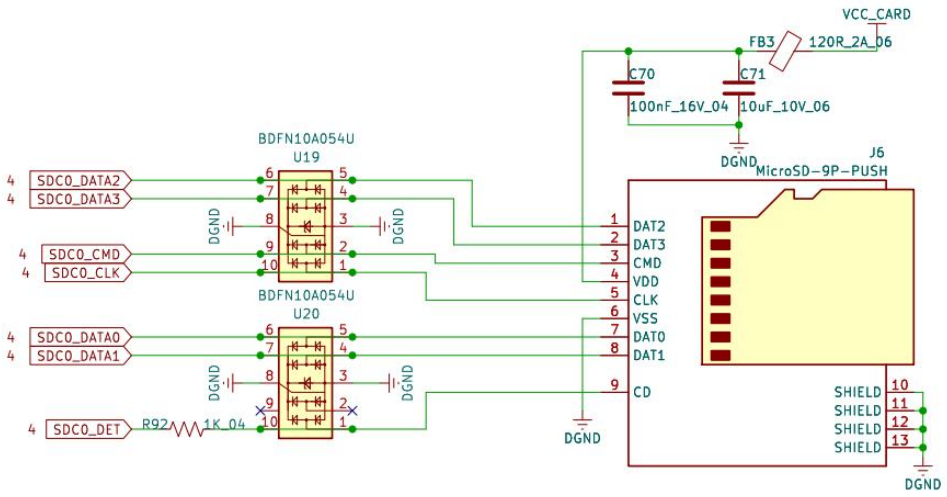
The ECK32-T527B series core board is equipped with 3 SMHC (SD/MM host controller) controllers, including SMHC0, SMHC1, and SMHC2. SMHC0 complies with the Secure Digital

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Memory v3.0 protocol and is usually used to connect to SD cards. SMHC1 complies with th e Secure Digital I/O v3.0 protocol and is usually used to connect to extended functions, such as Wi-Fi modules. SMHC2 complies with the Multimedia Card v5.0 protocol and is usually us ed to connect to eMMC storage chips. The ECK32-T527B series core uses SMHC2 to expand the on-board eMMC storage chip. It is recommended that the baseboard use SMHC0 to conn ect to the SD card. SMHC1 is recommended to expand other devices or not be used.

The processor's I/O can be configured with on-chip pull-up resistors. These pull-up resistor s can meet the pull-up requirements when the SD card interface is expanded, and the user des ign does not require external pull-up resistors. The core board has already connected a 22-ohm matching resistor in series with the PF2 clock signal, and the user design does not require ex ternal series resistors. If the expanded SD needs to be used to start the system, the SD card must be powered by the VCC-CARD power supply or a power supply controlled by VCC-CA RD. To expand the Micro SD card through the SMHC0 interface, refer to the following schem atic design.

6.9.1. References



SD card reference circuit diagram

6.9.2. Pin Definition

SMHC interface signal pin definition

LGA	Pin Name	MPU	Power Rail	Type	Length	Comment
D32	PF0	B20	BLDO3/1.8V/CLDO3/3.3V	I/O	602.2	SDC0-D1
D13	PF1	A20	BLDO3/1.8V/CLDO3/3.3V	I/O	580.83	SDC0-D0
D11	PF2	C19	BLDO3/1.8V/CLDO3/3.3V	I/O	672	SDC0-CLK

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D12	PF3	B19	BLDO3/1.8V/CLDO3/3.3V	I/O	578.68	SDC0-CMD
D49	PF4	B18	BLDO3/1.8V/CLDO3/3.3V	I/O	749.86	SDC0-D3
D33	PF5	A18	BLDO3/1.8V/CLDO3/3.3V	I/O	606.06	SDC0-D2
A53	PG0	R1	BLDO1/3.3V	I/O	411.99	SDC1-CLK
A54	PG1	R2	BLDO1/3.3V	I/O	503.98	SDC1-CMD
A71	PG2	P3	BLDO1/3.3V	I/O	407.33	SDC1-D0
A72	PG3	P2	BLDO1/3.3V	I/O	475.62	SDC1-D1
A85	PG4	T3	BLDO1/3.3V	I/O	465.45	SDC1-D2
A86	PG5	T2	BLDO1/3.3V	I/O	407.34	SDC1-D3

6.9.3. LAYOUT SUGGESTIONS

- SMHC signal is controlled according to the single-ended 50 ohm impedance, and the bottom board impedance control is recommended to be consistent;
- the SMHC signal base plate group is controlled within 150Mil;
- Insert a 1K ohm resistor in series with the detection signal to improve ESD performance;
- The distance between the clock signal and other signals follows the 3W rule.

6.10.USB interface

The ECK32-T527B series core board integrates 3 USB controllers, including:

- 1 USB2.0 OTG controller, the corresponding interface is USB0.
- 1 USB2.0 Host controller, the corresponding interface is USB1.
- 1 USB3.1 OTG controller, compatible with USB2.0 OTG, corresponding interfaces are USB2 and USB3.

USB interface information table

USB interface	Controller	Transmission speed level
USB0	USB2.0 OTG	HighSpeed, 480Mbps
USB1	USB2.0 Host	HighSpeed, 480Mbps
USB2	USB3.1 OTG	HighSpeed, 480Mbps
USB3		SuperSpeed, 5Gbps

The USB0 and USB2 ports of T527 have OTG function, while the USB1 port only has HOST function. The burning program can only use the USB0 port. It is necessary to pay attention to the difference in the product function definition.

Because the USB2 port and USB3 port share a set of controllers, they cannot be used in

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dependently at the same time. The precautions for use are as follows:

- When only USB2 port is used, it can be connected to a USB socket or USB device. At this time, USB3 port is unavailable.
- When only the USB3 port is used, it can be connected to an external USB socket o r USB device. At this time, the USB2 port is unavailable.
- When using the USB3.1 TypeA and TypeC interface sockets, it is recommended that both USB2 and USB3 be connected to the interface socket via cables, so that the int erface can achieve a physical interface compatible with USB3.0 and USB2.0 devices.

When USB3.0 and PCIE2.1 are not used, PCIE-REF-CLKP and PCIE-REF-CLKN are gro unded, and other signals can be floating. When USB3.0 is used, PCIE-REF-CLKP and PCIE-R EF-CLKN are grounded.

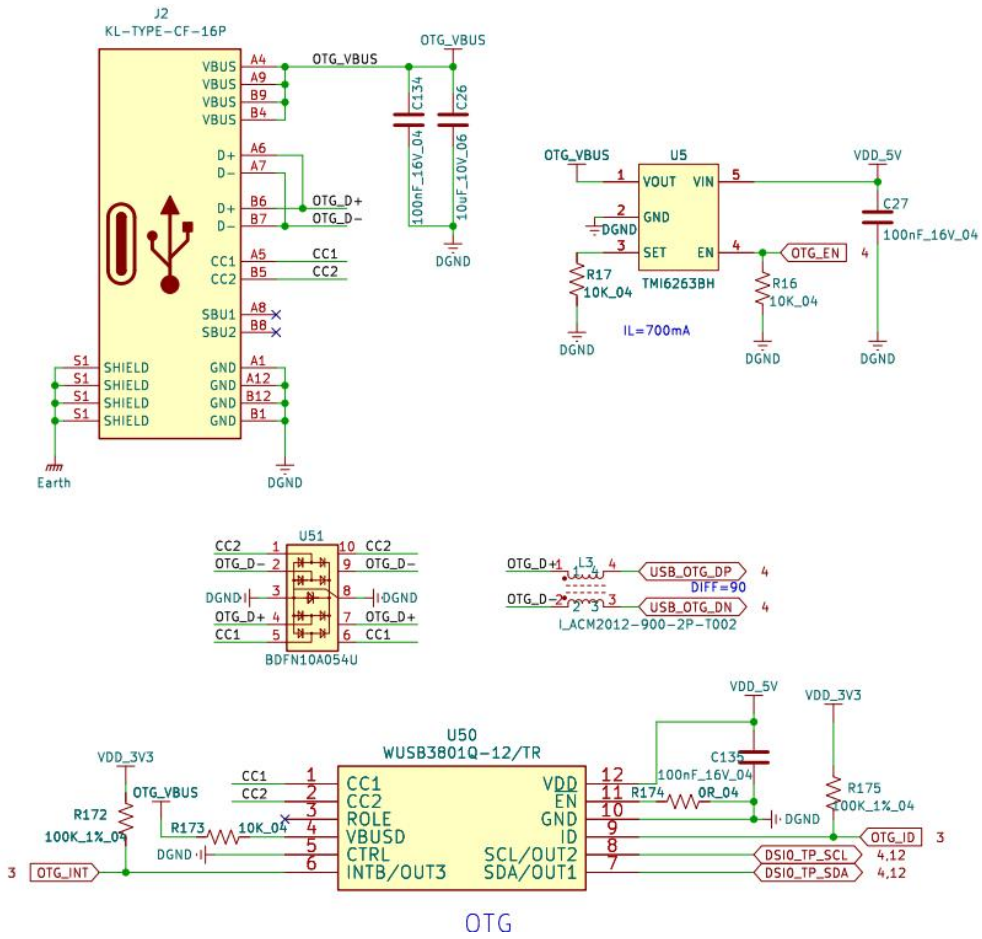
The USB OTG interface can be configured as an ID detection pin by configuring the GPI O pin and pull it up to the corresponding power domain of the GPIO through a resistor. If th e ID detection is low, the host recognizes that the USB peripheral is inserted and the USB w orks in Host mode. Otherwise, the USB works in Device mode. The USB can also be configu red by software to work only in Host mode or Device mode. It is recommended to connect a resistor in series with the ID detection signal to improve the ESD performance of the ID det ection I/O.

USB2.0 interface DM/DP and USB3.0 interface TX/RX signal lines need TVS protection. USB2.0 interface recommends that the parasitic capacitance of TVS device should be less than 2pF, USB3.0 interface requires that the parasitic capacitance of TVS tube connected to ground should be less than 0.5pF, and the clamping voltage capability should be as strong as possibl e, and the recommended clamping voltage should be less than 10V@8KV (IEC61000-4-2).

When TVS protection is used for the DM/DP signals of the USB OTG interface, it is rec ommended that the TVS should not be connected to the VBUS power supply of the OTG inte rface, because the power supply may be in the off state, which not only cannot provide effecti ve ESD protection, but may also introduce interference.

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6.10.1. OTG interface reference circuit



OTG interface reference circuit diagram

6.10.2. Pin Definition

USB interface signal pin definition

LGA	Pin Name	MPU	Power Rail	Type	Length	Comment
D09	USB0-DM	B24	CLDO3/3.3V	I/O	589.27	USB0-DM
D08	USB0-DP	A24	CLDO3/3.3V	I/O	590.76	USB0-DP
D30	USB1-DM	E24	CLDO3/3.3V	I/O	718.78	USB1-DM
D29	USB1-DP	D24	CLDO3/3.3V	I/O	719.32	USB1-DP
D47	USB2-DM	E22	DCDC4/3.3V	I/O	530.77	USB2-DM
D46	USB2-DP	D22	DCDC4/3.3V	I/O	530.98	USB2-DP

6.10.3. LAYOUT SUGGESTIONS

❖ The USB signal routing is controlled to be of equal length , the error within the different ial pair is no more than 50M il, and the spacing between adjacent differential pairs is mo

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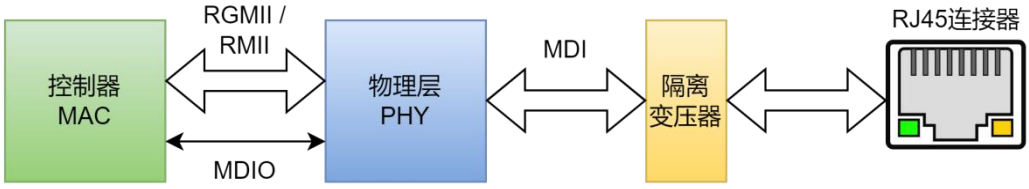
re than 3W;

- The differential impedance of the USB signal is controlled at 90 ohms ;
- The length of the USB signal trace is less than 6000Mil .

6.11.Ethernet interface

The ECK32-T527B series core board supports 2 -way 10M/100M /1000M adaptive Ethern et controller . The Ethernet controller supports RG MII and RMII interfaces. The ECK32-T527 B series core board MII interface is reused for PH/PJ pins.

Usually an RJ45 Ethernet interface is mainly composed of an Ethernet controller MAC (Media Access Control), an Ethernet physical layer interface PHY (Physical Layer), an Ethernet transformer, and an RJ45 connector, as shown in the figure below.



RJ45 Ethernet components

The ECK32-T527B series core board does not have an Ethernet PHY circuit designed in i t. If the user uses the Ethernet function, the PHY interface chip circuit needs to be designed o n the baseboard. The baseboard PHY interface chip circuit design can refer to the Ebyte single -board computer product drawings.

6.11.1. Pin Definition

Ethernet interface signal pin definition

LGA	Pin Name	MPU	Power Rail	Type	Length	Function
D80	PH3	C17	CLDO3/3.3V	I/O		RGMII0-CLKIN/RMII0-RXER
D79	PH13	B15	CLDO3/3.3V	I/O		RGMII0-EPHY-25M
D34	PH9	C16	CLDO3/3.3V	I/O		RGMII0-MDC
D35	PH10	B16	CLDO3/3.3V	I/O		RGMII0-MDIO
D65	PH16	B14	CLDO3/3.3V	I/O	694.47	RGMII0-RXCK/RMII0-NULL
D67	PH2	D18	CLDO3/3.3V	I/O	603.32	RGMII0-RXCTL/RMII0-CRS-DV
D66	PH1	E18	CLDO3/3.3V	I/O	646.3	RGMII0-RXD0/RMII0-RXD0
D76	PH0	F18	CLDO3/3.3V	I/O	624.77	RGMII0-RXD1/RMII0-RXD1
D77	PH15	D14	CLDO3/3.3V	I/O	600.87	RGMII0-RXD2/RMII0-NULL
D78	PH14	E14	CLDO3/3.3V	I/O	604.19	RGMII0-RXD3/RMII0-NULL
D70	PH6	G12	CLDO3/3.3V	I/O	500.59	RGMII0-TXCK/RMII0-TXCK

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D68	PH7	F14	CLDO3/3.3V	I/O	413.53	RGMII0-TXCTL/RMII0-TXEN
D52	PH5	E16	CLDO3/3.3V	I/O	586.12	RGMII0-TXD0/RMII0-TXD0
D53	PH4	B17	CLDO3/3.3V	I/O	426.55	RGMII0-TXD1/RMII0-TXD1
D54	PH18	A14	CLDO3/3.3V	I/O	426.59	RGMII0-TXD2/RMII0-NULL
D69	PH17	B13	CLDO3/3.3V	I/O	556.18	RGMII0-TXD3/RMII0-NULL
A51	PJ3	E2	DCDC4/3.3V	I/O		RGMII1-CLKIN/RMII1-RXER
A69	PJ10	G4	DCDC4/3.3V	I/O		RGMII1-EPHY-25M
A49	PJ8	H2	DCDC4/3.3V	I/O		RGMII1-MDC
A50	PJ9	H3	DCDC4/3.3V	I/O		RGMII1-MDIO
A29	PJ13	J5	DCDC4/3.3V	I/O	604.71	RGMII1-RXCK/RMII1-NULL
A52	PJ2	E1	DCDC4/3.3V	I/O	609.45	RGMII1-RXCTL/RMII1-CRS-DV
A30	PJ1	D2	DCDC4/3.3V	I/O	661.56	RGMII1-RXD0/RMII1-RXD0
A31	PJ0	D1	DCDC4/3.3V	I/O	610.6	RGMII1-RXD1/RMII1-RXD1
A07	PJ12	J4	DCDC4/3.3V	I/O	632.35	RGMII1-RXD2/RMII1-NULL
A08	PJ11	G5	DCDC4/3.3V	I/O	702.93	RGMII1-RXD3/RMII1-NULL
A81	PJ6	G1	DCDC4/3.3V	I/O	502.6	RGMII1-TXCK/RMII1-TXCK
A82	PJ7	G2	DCDC4/3.3V	I/O	504.43	RGMII1-TXCTL/RMII1-TXEN
A83	PJ5	F2	DCDC4/3.3V	I/O	524.7	RGMII1-TXD0/RMII1-TXD0
A84	PJ4	F1	DCDC4/3.3V	I/O	507.69	RGMII1-TXD1/RMII1-TXD1
A67	PJ15	L5	DCDC4/3.3V	I/O	601.7	RGMII1-TXD2/RMII1-NULL
A68	PJ14	L4	DCDC4/3.3V	I/O	502.15	RGMII1-TXD3/RMII1-NULL

6.11.2. LAYOUT SUGGESTIONS

- RGMII signal sending and receiving packets are controlled to be equal length, with an err or of 100M il and a line spacing of more than 2W;
- The network differential signal is controlled to be equal length, the error within the differ ential pair is 10 mil , and the spacing between adjacent differential pairs is more than 3 W;
- The network port transformer should be placed close to the PHY chip, and the recommen ded distance is no more than 20 mm.
- The decoupling capacitor of the power pin of the PHY chip is placed close to the PHY chip .

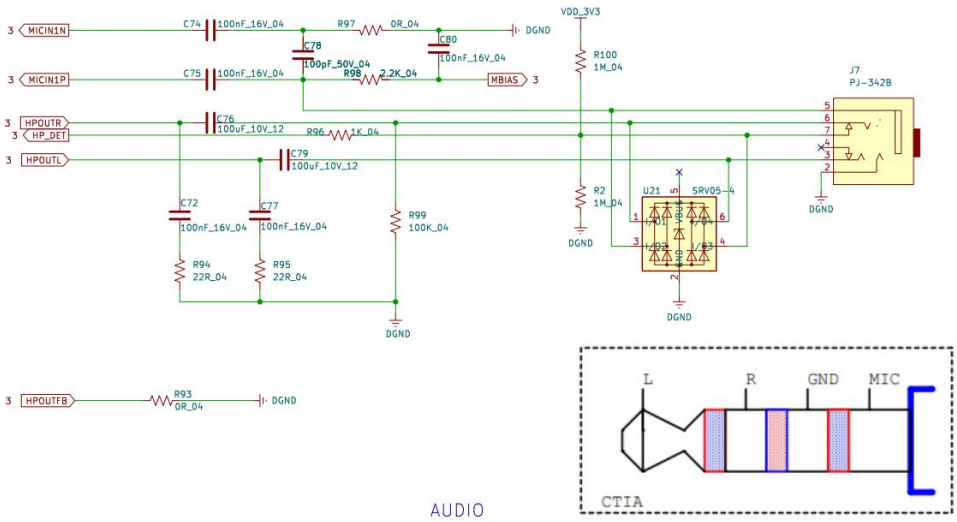
6.12.Analog audio interface

The T527 chip integrates audio codec function and provides analog audio interface. The E CK32-T527B core board leads to 2 analog audio output interfaces (LINEOUT, HPOUT) and 2

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analog audio input interfaces (MICIN*2).

6.12.1. References



Analog Audio Headset Interface Schematic

6.12.2. Pin Definition

Analog audio signal pin definition

LGA	Pin Name	MPU	Power Rail	Type	Length	Function
A55	HPOUTFB	AM1	BLDO3/1.8V	AI		HPOUTFB
A56	HPOUTL	AL2	BLDO3/1.8V	AO		HPOUTL
A57	HPOUTR	AM2	BLDO3/1.8V	AO		HPOUTR
A75	LINEOUTLN	AG1	ALDO4/1.8V	AO		LINEOUTLN
A74	LINEOUTLP	AG2	ALDO4/1.8V	AO		LINEOUTLP
A89	LINEOUTRN	AH1	ALDO4/1.8V	AO		LINEOUTRN
A88	LINEOUTRP	AH2	ALDO4/1.8V	AO		LINEOUTRP
A13	MICIN1P	AD1	ALDO4/1.8V	AI		MICIN1P
A14	MICIN1N	AD2	ALDO4/1.8V	AI		MICIN1N
A35	MICIN2N	AE1	ALDO4/1.8V	AI		MICIN2N
A36	MICIN2P	AE2	ALDO4/1.8V	AI		MICIN2P

6.12.3. LAYOUT SUGGESTIONS

- Place TVS close to the interface;
- Analog signal routing should be kept away from interference and can be wrapped wit h ground.

6.13.Digital Audio Interface

The ECK32-T527B core board can support 4-channel I2S/PCM, 8-channel DIMC, and

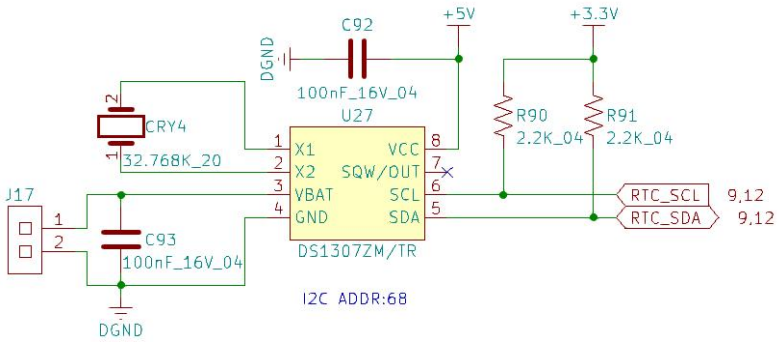
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1-channel OWA digital audio interface . For the I2S/PCM interface, in the baseboard circuit d esign, it is necessary to connect the digital audio interface I2S/PCM signal to the audio codec chip , and realize the audio interface functions such as headphones, microphones, and speaker s through the audio codec chip .

6.14.RTC

The ECK32-T527B core board does not have a battery-backed RTC. If the user needs this RTC function, the function can be expanded on the baseboard through the I2C bus.

6.14.1. References



RTC reference circuit diagram

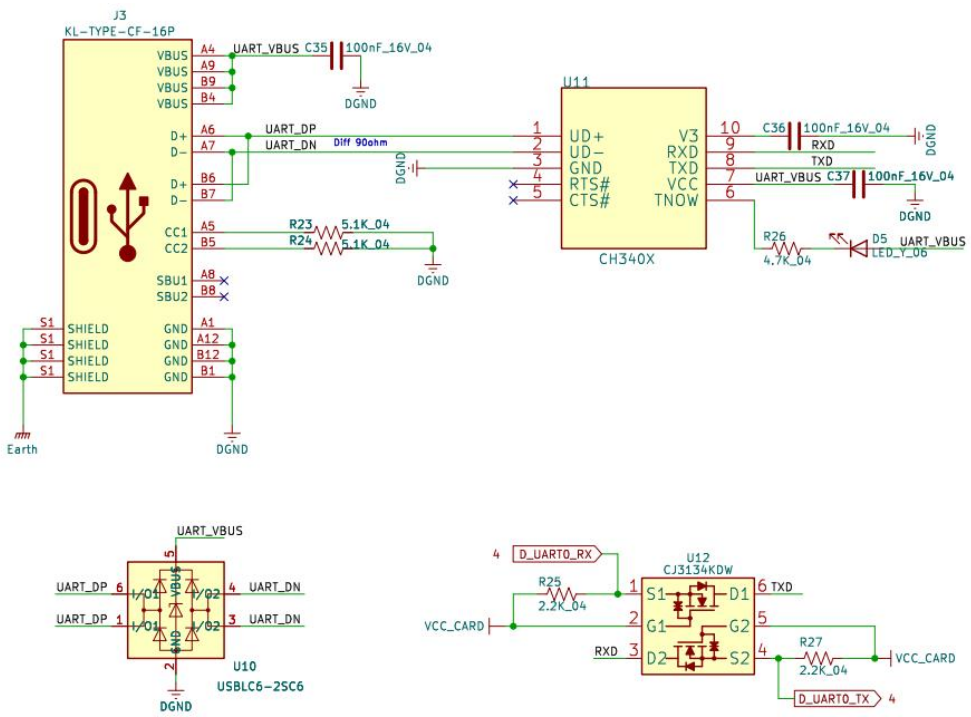
6.15.UART Interface

The ECK32-T527B core board supports up to 10 asynchronous serial ports and a baud rat e of up to 10Mbps. The core board uses UART 0 as the debug serial port by default. When designing the debug serial port on the baseboard, you need to pay attention to the serial port power-on timing.

6.15.1. References

For debugging convenience, the debug serial port can be brought out as a USB interf ace through the USB to serial port chip on the baseboard. The USB to serial port circuit schematic can be referred to in the figure below. The CH343G chip provides VIO power, which can effectively solve the problems of serial port I/O level compatibility and power domain power-on timing.

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USB debug serial port reference schematic

6.16.SPI interface

The ECK32-T527B series core board leads to 4 SPI interfaces , supporting master/slave m ode. SPI signals include SPI_CLK, SPI_SS, SPI_MOSI and SPI_MISO. When designing, you must first confirm the relationship between the master and slave devices, and then confirm the direction of the MOSI and MISO signals.

6.17.I2C Interface

The ECK32-T527B series core board supports 8-way I2C (TWI) controller and 2 clock fre quency modes. The rate in standard mode is 100Kbit/s and the rate in fast mode is 400Kbit/s.

Several devices can be mounted on the same I2C bus. The following points should be not ed when designing the schematic:

a) Check whether the device addresses on the same bus conflict;

b) Ensure that each I2C bus has a pair of pull-up resistors. The recommended resistance i s 2.2K~10K, but do not add duplicates.

c) The core board does not provide an I2C bus pull-up resistor, so the user needs to pull it up when using the baseboard;

d) Check whether the I2C interface level of the device is 3.3V. If not, a level conversion

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circuit needs to be added;

e) Check whether the I2C interface power rails are consistent. When I2C interfaces in diff erent time domains are interconnected, the bus switch circuit needs to be considered;

f) Do not use too many devices on the same bus, otherwise it may exceed the 400pF loa d capacitance limit required by the I2C specification and affect the signal waveform.

6.18.CAN interface

The ECK32-T527B series core board supports 2-way CAN controllers and CAN 2.0A and CAN 2.0B protocols. It only needs an external CAN transceiver to perform CAN communicat ion.

6.19.ADC Interface

The ECK32-T527B series core board provides two types of ADC interfaces, namely 2-way LRADC (Low Rate ADC) and 8-way GPADC (General Purpose ADC).

LRADC:

- 6-bit resolution, used for key voltage recognition, maximum sampling rate 2KHz, sam pling voltage range: 0~1.35V;
- When LRADC is used for key recognition, if the key adopts voltage-dividing resistor mode, it is recommended to use 1% precision resistor;

GPADC:

- 12bit resolution, maximum sampling rate 1MHz, sampling voltage range: 0~1.8V;
- GPADC is not recommended for external I/O voltage identification with surge or hig h voltage to avoid damage to the chip interface.

6.19.1. Pin Definition

ADC interface pin definition

LGA	Pin Name	MPU	Power Rail	Type	Length	Comment
A92	GPADC10	AA3	ALDO4/1.8V	AI		GPADC10
A16	GPADC3	W4	ALDO4/1.8V	AI		GPADC3
A59	GPADC4	W5	ALDO4/1.8V	AI		GPADC4
A91	GPADC5	W6	ALDO4/1.8V	AI		GPADC5
A39	GPADC6	Y2	ALDO4/1.8V	AI		GPADC6
A77	GPADC7	Y3	ALDO4/1.8V	AI		GPADC7
A17	GPADC8	AA1	ALDO4/1.8V	AI		GPADC8

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A60	GPADC9	AA2	ALDO4/1.8V	AI		GPADC9
A40	LRADC0	V3	ALDO4/1.8V	AI		LRADC0
A78	LRADC1	V2	ALDO4/1.8V	AI		LRADC1

6.20.GPIO interface

The ECK32-T527B series core board can provide up to 187 GPIO interfaces, but most of them have multiplexing functions. Users can flexibly configure GPIO according to their own needs.

6.21.Hardware Design Checklist

- Power rail: Check whether there is an inconsistent power rail problem in the I/O interface application, such as connecting a 1.8V signal to a 3.3V signal. If there is a need to connect signals with different power rails, a level conversion circuit should be used.
- Power-on sequence: Check whether the signals connecting the baseboard and the core board are powered on first, or whether the power-on time of the two board signals is very different.
- Pull-up and pull-down resistors: The output state of the multiplexed I/O interface is uncertain before the power-on software configuration. If the signal needs to maintain a stable level when powered on, pull-up and pull-down resistors should be designed on the baseboard. Some functional signals also need to be designed with pull-up or pull-down resistors on the baseboard, such as I2C signals. When designing pull-up resistors, attention should be paid to the design of the pull-up power rail.
- ESD protection: The corresponding ESD protection design should be considered for the external interface signal. The selection of ESD solution should take into account the requirements of signal rate, communication protocol and application environment.
- High-speed signals should be of equal length: High-speed signals should consider the equal length design of PCB, including USB, Ethernet, SDIO, display, etc.
- Impedance control: High-speed signals should consider PCB impedance control. The key to impedance control is to maintain impedance continuity. The baseboard should be designed with reference to the impedance of the core board signal.

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7. Software Resources

The ECB32-T527B single-board computer is equipped with an operating system based on the Linux 5.15 kernel. The single-board computer comes with the cross-compilation tool chain Buildroot source code, U-boot source code, Linux kernel and various driver module source cod e required for embedded Linux system development, as well as various development and debug ging tools suitable for Windows desktop environment and Linux desktop environment.

operating system:

1. Linux file system built by Buildroot

2. Linux file system transplanted from Debian

System source code:

1.U-boot 2018

2. Kernel 5.15

3.BuildRoot 2022.05

4. Debian 11

Development environment and tools:

1.USB burning tool: PhoenixSuit

2. SD card burning tool: PhoenixCard

System software resources are shown in the following table:

System Software Resource Table

category	name	describe	Source code
SPL	spl-pub	Boot0, boot uboot	<SDK>/ brandy/brandy-2.0/spl-pub /
BOOT	u-boot 2018.07	Bootloader	<SDK>/brandy/brandy-2.0/u-boot-2018/
Kernel	Kernel 5. 15 . 147	Linux Kernel	<SDK> /kernel/linux-5.15 /
Bsp	BSP	The device tree of the kernel driver related to Allwinner, etc.	<SDK>/ bsp/
Device Driver	Audio	Built-in audio driver	bsp/drivers/sound/platform /*
	AWlink	CAN Driver	bsp/awlink
	GMAC	Built-in MAC driver	bsp/gmac
	STMMAC	Built-in MAC driver	Bsp/stmmac
	GPADC	GPADC Driver	bsp/gpadc

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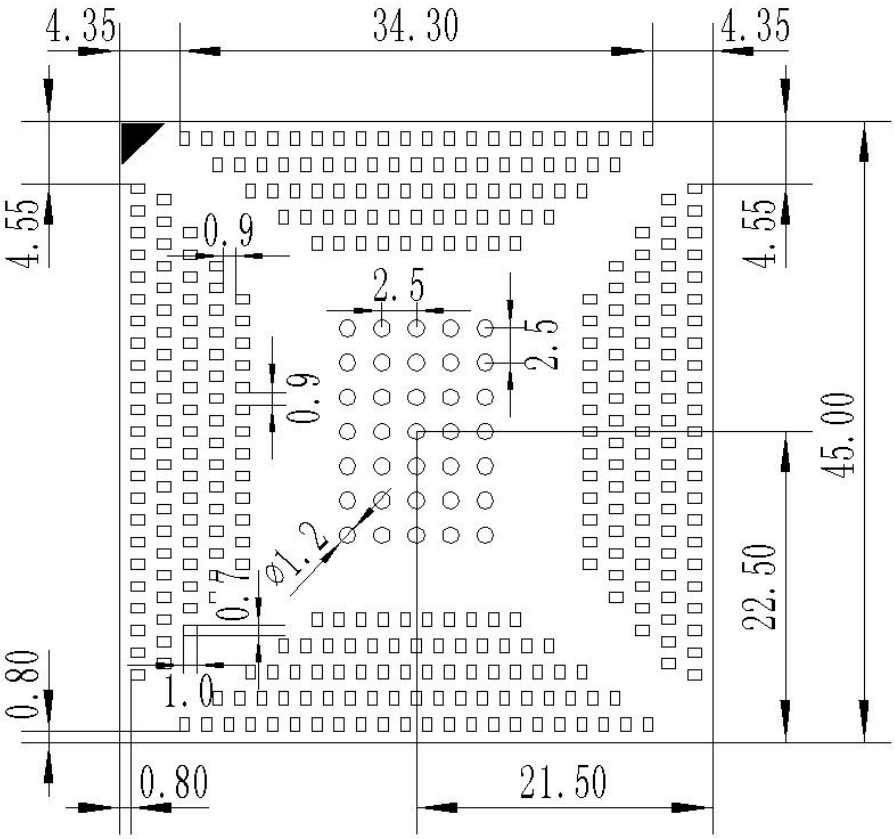
	GPIO	GPIO Driver	bsp /pinctrl/ *
	drm	Display screen related drivers	bsp/drm/panel/*
	LRADC	Button module driver	bsp/lradc/*
	MMC	MMC Driver	bsp/mmc/*
	SPI	SPI Driver	bsp/spi/*
	TWI	I2C Driver	bsp/twi/*
	UART	Serial port driver	bsp/uart/*
	VIN	Specific camera drivers	bsp/vin/modules/sensor/*
	Pcie	PCI Driver	bsp/pci/*
	IR	Infrared driver	bsp/ir-rx/* bsp/ir-tx/*
operating system	Buildroot 202205	Buildroot 202205	<SDK>/buildroot/buildroot-202205
	Debian	Debian 11	<SDK> /debian/compressed_files/
Development Tools	PhoenixSuit	USB burning tool	/tools/ PhoenixSuit
	PhoenixCard	SD card burning tool	/tools/PhoenixCard

8. Structural dimensions

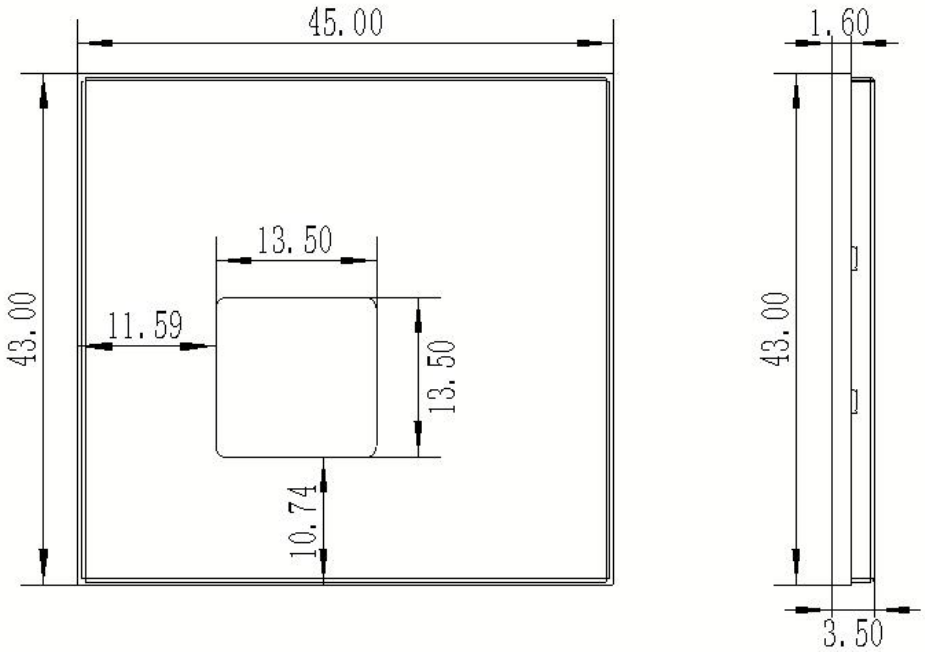
The ECK32-T527B series core board adopts 381 PIN, LGA interface, and can be SMT soldered. There are no components on the bottom of the core board, no exposed wiring, and the bottom board design is simple.

The ECK32-T527B series core board is 45.0mm long and 43.0mm wide, with 346 rectangular pads (1.0 × 0.7mm) and 35 round pads (1.2mm in diameter). The structural dimensions are shown in the figure below. The following dimensions are in millimeters (mm), the structural dimension tolerance is ±0.1mm, and the PCB thickness tolerance is 10%.

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LGA core board structure dimensions (top view)



LGA core board shielding cover structure size drawing

9. Welding Instructions

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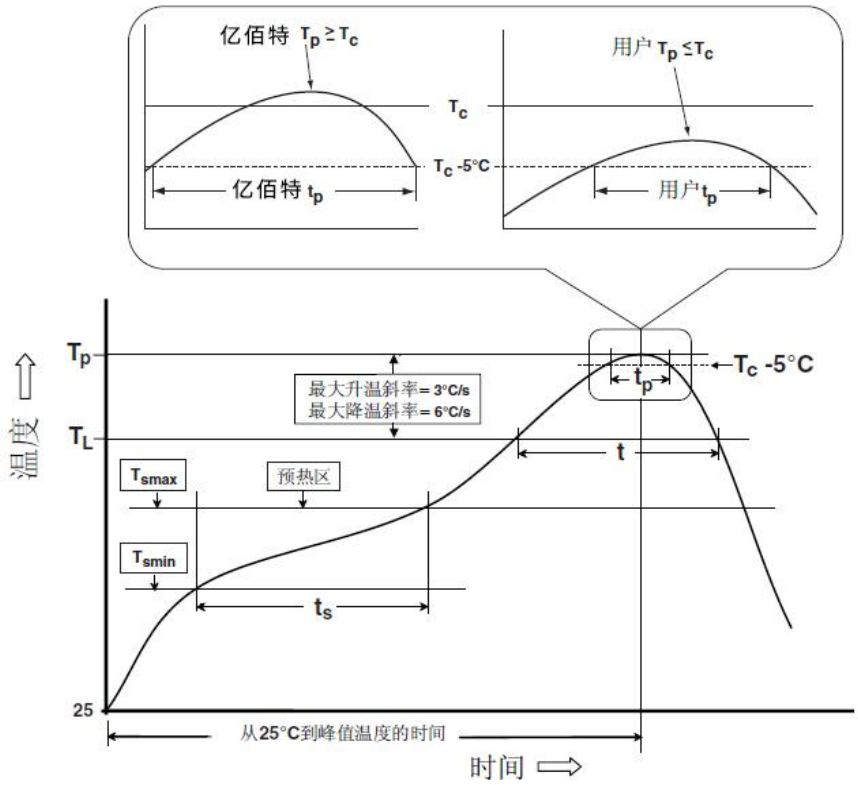
9.1.Reflow temperature

Reflow Temperature Table

Reflow profile characteristics		Leaded process assembly	Lead-free assembly
Preheating/keeping	Minimum temperature (Tsmin)	100℃	150℃
	Maximum temperature (Tsmax)	150℃	200℃
	Time (Tsmin~Tsmin)	60-120 seconds	60-120 seconds
Heating slope (TL~Tp)		3℃/sec, max.	3℃/sec, max.
Liquidus temperature (TL)		183℃	217℃
Keep time above TL		60~ 90 seconds	60~ 90 seconds
Package peak temperature Tp		Users must not exceed the temperature stated on the product's "Moisture Sensitivity" label.	Users must not exceed the temperature stated on the product's "Moisture Sensitivity" label.
The time (Tp) within 5℃ of the specified classification temperature (Tc) is shown in the figure below.		20 seconds	30 seconds
Cooling slope (Tp~TL)		6℃/sec, max.	6℃/sec, max.
Time from room temperature to peak temperature		6 minutes, longest	8 minutes, longest
※The peak temperature (Tp) tolerance of the temperature curve is defined as the upper limit of the user			

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9.2.Reflow Oven Profile



Reflow Oven Profile

10. Revision Notes

Revision Notes Table

Version	Modifications	Modification time	prepared by	Proofreading	Approval
V1.0	First Draft	25-03-28	WFX	Wlq	WFX

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