Product Manual
ECK30-T13IC Core Board



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1.Introduction

1.1. Brief Introduction

ECK30-T13IC series core board is based on Allwinner's T113-i processor carefully designed, using the BTB connector to connect the low-cost, low-power, cost-effective, highly reliable, fully localized industrial-grade embedded core board. It can be widely used in in dustrial control, HMI, IoT and other fields.

Allwinner's T113-i processor is composed of three heterogeneous processors: dual-core ARM Cortex-A7, RISC-V and HiFi4 DSP, which can provide users with efficient computing power. It also provides rich digital I/O functions such as 1-channel display, 1-channel digital camera, 1-channel Gigabit Ethernet, 3-channel SDIO, 2-channel USB, 6-channel UART, and 2-channel CAN, as well as rich analog I/O functions such as analog video, analog audio, and ADC.

ECK30-T13IC series core boards contain 3 specific product models, all of which are designed with fully localized industrial-grade devices. They mainly have some differences in memory capacity, storage configuration, etc. Customers can choose the appropriate model according to their needs. For details of product selection, please refer to the Product Selection section.

The physical diagram of ECK30-T13IC series core board is as follows:



physical diagram

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1.2. Features

1、Processor: Allwinner T113-i processor:

- Dual-core ARM Cortex-A7, up to 1.2GHz;
- RISC-V;
- HiFi4 DSP;

2、On-board mounted DDR3 SDRAM, 256MB/512MB/1GB capacity optional;

3、on-board storage: 8GB eMMC or 256MB SPI NAND FLASH optional;

4、Video output:

- 2 Road LVDS output, support 1920×1080@60fps;
- 1 road digital RGB output, support 1920×1080@60fps;
- 1 Road MIPI DSI, support 4Lane, support 1920×1200@60fps;
- 1 channel CVBS output, supporting NTSC and PAL;
- 1 road serial RGB (DBI) output, support 240×32060fps;
- Note: LVDS0 and LVDS1 are multiplexed with digital RGB pins, LVDS0 is mult iplexed with MIPI DSI pins, and DBI is multiplexed with SPI1 pins;

5、video input:

- 1 road CSI, 8-bit parallel interface, support 1920×1080@30fps;
- 2 way CVBS input, support NTSC and PAL;

6、audio interface:

- integrated Audio Codec;
- 3 road mono MIC input;
- 1 road dual-channel LINE IN;
- 1 road dual-channel FM IN;
- 1 channel differential LINE OUT;
- 1 road dual-channel Headphone output;

7、network: integrated 1 10/100/1000 adaptive Ethernet MAC, support RMII/RGMII interfa ce;

8、USB: 1-way USB2.0 DRD, 1-way USB2.0 HOST;

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9、SMHC: integrated 3 SMHC controller, lead 2-way to BTB connector;

10、4-way TWI, compatible with I2C bus standard, support standard mode (100Kbps) and high-speed mode (400Kbps);

11、2-channel SPI, lead 1 way to BTB connector;

12、6-way UART, maximum baud rate 4Mbps;

13、8-way PWM, the maximum output frequency of 24/100MHz, support for PWM output, input capture;

14、2-way GPADC, 12-bit resolution, maximum sampling rate of 1MHz;

15、4-way TPADC, 12-bit resolution, maximum sampling rate of 1MHz, support for 4-wire resistive touch screen;

16、1-channel LRADC, 6-bit resolution, maximum sampling rate 2KHz;

17、1-channel LEDC, support 1024 LEDs in series, maximum data transfer rate of 800Kbps;

18、3-way I2S/PCM, support full-duplex, sampling rate 8KHz~48KHz;

19、1-channel DMIC, support up to 8 channels, sampling rate 8KHz~48KHz;

20、1-way OWA, compatible with S/PDIF protocol;

21、2-way CIR, 1x CIR TX interface, 1x CIR RX interface;

22、2-way CAN (CAN0, CAN1), support CAN 2.0A and CAN 2.0B protocol;

23、3-way JTAG, including ARM, RISC-V and HiFi4 DSP JTAG;

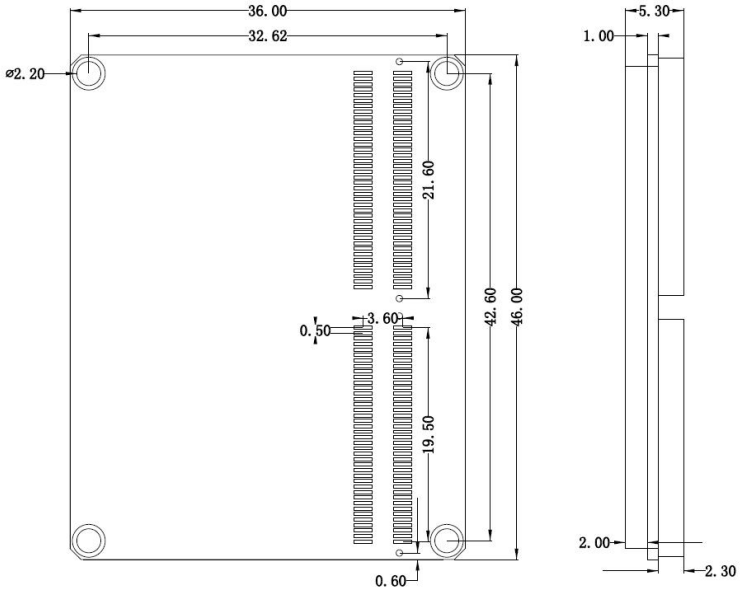
24、interface form: 160-pin BTB connector, pitch 0.5mm;

25、power supply: single DC +5V±10%@0.5A Power Input;

26、Dimensions: 46×36×5.3mm, dimensions as shown below:

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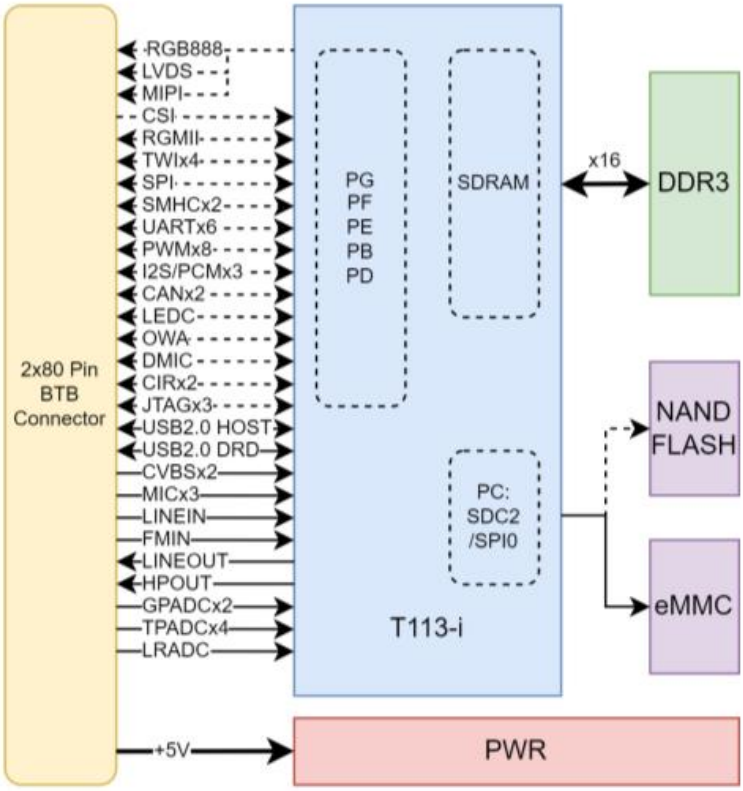
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27、Operating temperature: industrial grade: -40℃-85℃;

28、PCB process: 8-layer board design, immersion gold, lead-free process;

1.3. Functional block diagram of the core board



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1.4. Typical applications

- Smart Homes;
- Smart toys;
- Smart cities;
- Tablets;
- IoT gateways;
- Advertising all-in-one machines;
- Industrial all-in-one machines;
- Industrial control motherboards;
- Robots, drones.

2. Product Selection

2.1. Model Configuration

The ECK30-T13IC series core board selection and configuration table is listed below:

Product Selection and Configuration Chart

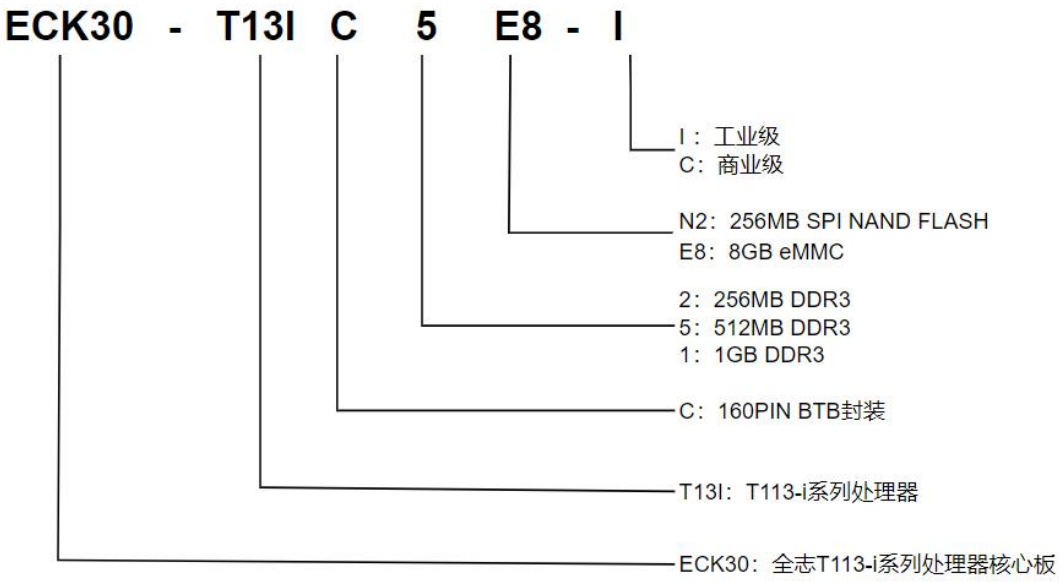
No	Product Model	Processor Model	RAM	Storage	operating temperature
1	ECK30-T13IC2N2-I	T113-i	256MB DDR3	256MB NAND	Industrial Grade -40℃ ~ 85℃
2	ECK30-T13IC5E8-I	T113-i	512MB DDR3	8GB eMMC	Industrial Grade -40℃ ~ 85℃
3	ECK30-T13IC1E8-I	T113-i	1GB DDR3	8GB eMMC	Industrial Grade -40℃ ~ 85℃

2.2. Model code

The description of the product model code is shown below:

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Model Code Description

3. Quick experience

By choosing Ebyte's single board products, you can quickly experience the typical application functions of ECK30-T13IC core board products, backplane design, software development and so on.

4. Functions and parameters

4.1. Product Functions

ECK30-T13IC series core board mainly integrates the processor, memory, storage and power system, and leads to all I/O pins on the processor. Users can design the base board to apply the I/O resources on the core board according to their needs and multiplex the I/O into their desired functions.

The following table lists the main functional parameters of the ECK30-T13IC series core board integrated on-board, and the functional parameters of the reusable I/O resources. The description of each I/O function is the maximum indicator that the core board can use the I/O function without using other I/O functions (e.g., after using the 24-bit color RGB interface function and the network interface function, the full UART function cannot b

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e realized).

Product Functions

Function	quantities	Functional Description
CPU	1	T113-i； Dual-core ARM Cortex-A7@1.2GHz； RISC-V CPU； HiFi4 DSP；
MEM	1	On-board DDR3 SDRAM, 16-bit wide, 256MB/512MB/1GB optional;
FLASH	1	On-board 8GB eMMC / On-board 256MB SPI NAND FLASH optional;
DISPLAY	1	Parallel RGB 24-bit color output, supporting up to 1920×1080@60fps; Dual-channel LVDS output, supporting up to 1920×1080@60fps; 4-lane MIPI DSI, supports up to 1920×1200@60fps Note: The above display interface part of I/O is multiplexed relationship can not be used at the same time; Serial RGB output, supports up to 800×480@60fps;
CSI	1	8-bit parallel digital camera interface, support 1080P@30fps, maximum 148.5MHz pixel clock;
CVBS IN	2	1 CVBS decoder, support NTSC and PAL, 10-bit video ADC;
CVBS OUT	1	Supports NTSC and PAL, 10-bit video DAC;
Audio Codec	1	2-channel DAC, sampling rate 8KHz~192KHz; 3-channel ADC, sampling rate 8KHz~48KHz; 3-channel MIC IN, 1-channel LINE IN, 1-channel FM IN; 1 channel differential LINE OUT, 1 channel Headphone OUT;
EMAC	1	Support RMII/RGMII interface (10/100/1000Mbps);
SMHC	2	Support SD3.0, SDIO3.0, MMC5.0 protocols; SDC0: 4-bit data bus (recommended for baseboard Micro SD function); SDC1: 4-bit data bus; Note: SDC2 is not led to the BTB connector for on-board connection of eMMC or FLASH memory chips;
USB DRD	1	Compliant with USB2.0 standard, supporting USB HOST and USB Device functions;
USB HOST	1	Complies with USB2.0 standard, supports USB HOS function;
TWI(I2C)	4	Support standard mode (100Kbps) and high speed mode (400Kb

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		ps);
SPI	1	Support SPI mode and DBI (Display Bus Interface) mode; Support Master Mode, Slave Mode, 1 chip select signal; Supports up to 100MHz operating frequency;
UART	6	Maximum 4Mbps baud rate (64MHz APB clock), supports hard ware or software flow control;
PWM	8	0~100% adjustable duty cycle, support output and input capture, output frequency 0~24MHz or 100MHz;
GPADC	2	12-bit SAR type A/D converter, sampling frequency up to 1MH z;
TPADC	4	12-bit SAR type A/D converter, sampling frequency up to 1MH z, support 4-wire resistive touch screen;
LRADC	1	6-bit A/D converter with sampling frequency up to 2KHz, suppo rts hold key and universal key;
LEDC	1	Support 1024 LEDs serial connection, LED data transmission rat e up to 800Kbps;
PCM/I2S	3	Support full duplex, sampling rate 8KHz~384KHz;
DMIC	1	Support up to 8 channels, sampling rate 8KHz~48KHz;
OWA	1	One Wire Audio, compatible with S/PDIF protocol;
CIR	2	Including CIR TX, CIR RX, can be remotely controlled by infra red;
CAN	2	Support CAN 2.0A and CAN 2.0B protocols;
JTAG	3	Includes ARM, RISC-V and HiFi4 DSP JTAG;
GPIO	79	Software-configurable GPIO function with support for interrupt i nputs;

4.2. Environmental Characteristics

Environmental Characteristics Table

Workin	Industrial Grade	-40℃ ~ 85℃;

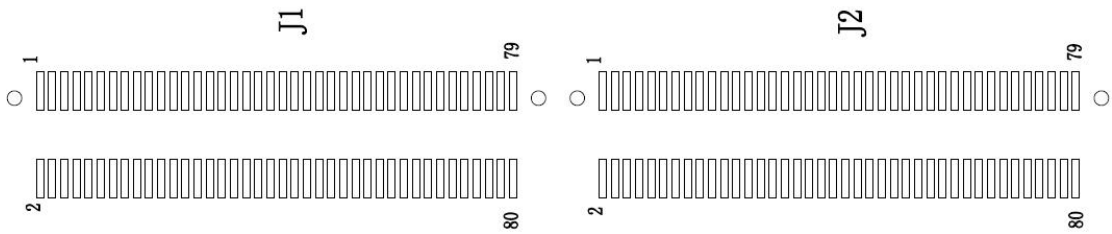
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g Temperature		
Storage temperature	-40℃ ~ 85℃；	
Operating humidity	5 to 95% humidity, non-condensing;	
Storage humidity	60℃ @ 95% humidity, non-condensing;	

4.3. Characteristics

4.3.1. Pin Definitions



Pin Numbering Diagram

Pin Definition Table

Pin	Pin Name	MPU Pin	Level/Rail	Type	Length(mil)	Comment
J1-1	DGND	-	GND	PWR	-	
J1-3	PB0_J16	J16	3.3V/VCC-IO	I/O	2675.29	
J1-5	PB1_J17	J17	3.3V/VCC-IO	I/O	2350.59	
J1-7	PB2_M16	M16	3.3V/VCC-IO	I/O	2466.60	
J1-9	PB3_M15	M15	3.3V/VCC-IO	I/O	2462.52	
J1-11	PB4_K16	K16	3.3V/VCC-IO	I/O	2471.63	
J1-13	PB5_K15	K15	3.3V/VCC-IO	I/O	2456.12	
J1-15	PB6_K17	K17	3.3V/VCC-IO	I/O	2463.43	
J1-17	DGND	-	GND	PWR	-	
J1-19	PB7_J15	J15	3.3V/VCC-IO	I/O	2467.88	
J1-21	PB8_G15	G15	3.3V/VCC-IO	I/O	1930.68	
J1-23	PB9_G16	G16	3.3V/VCC-IO	I/O	1882.61	

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J1-25	PB10_F17	F17	3.3V/VCC-IO	I/O	1888.70	
J1-27	PB11_F15	F15	3.3V/VCC-IO	I/O	1902.53	
J1-29	PB12_F16	F16	3.3V/VCC-IO	I/O	1895.53	
J1-31	DGND	-	GND	PWR	-	
J1-33	FMINR_C17	C17	1.8V/AVCC	AI	1568.88	
J1-35	FMINL_B17	B17	1.8V/AVCC	AI	1416.71	
J1-37	LINEINR_C16	C16	1.8V/AVCC	AI	1401.68	
J1-39	LINEINL_B16	B16	1.8V/AVCC	AI	1329.10	
J1-41	AUD_AGND	-	AGND_AU_DIO	PWR	-	
J1-43	MBIAS_E16	E16	3.3V/VCC-IO	AO	1528.15	
J1-45	MIC_DET_A17	A17	1.8V/AVCC	AI	1425.14	
J1-47	MICIN1P_D20	D20	1.8V/AVCC	AI	1439.29	
J1-49	MICIN1N_D19	D19	1.8V/AVCC	AI	1414.33	
J1-51	MICIN3P_D17	D17	1.8V/AVCC	AI	1462.32	
J1-53	MICIN3N_D16	D16	1.8V/AVCC	AI	1454.19	
J1-55	MICIN2P_E15	E15	1.8V/AVCC	AI	1417.92	
J1-57	MICIN2N_D15	D15	1.8V/AVCC	AI	1388.68	
J1-59	AUD_AGND	-	AGND_AU_DIO	PWR	-	
J1-61	LINEOUTLP_B15	B15	1.8V/AVCC	AO	1312.25	
J1-63	LINEOUTLN_C15	C15	1.8V/AVCC	AO	1318.73	
J1-65	LINEOUTRP_B14	B14	1.8V/AVCC	AO	1366.59	
J1-67	LINEOUTRN_C14	C14	1.8V/AVCC	AO	1385.99	
J1-69	AUD_AGND	-	AGND_AU_DIO	PWR	-	
J1-71	HP_DET_A13	A13	1.8V/AVCC	AI	1185.57	
J1-73	HBIAS_E17	E17	3.3V/VCC-IO	AO	1330.01	
J1-75	HPOUTR_D13	D13	1.8V/HPVCC	AO	947.99	
J1-77	HPOUTFB_E13	E13	1.8V/HPVCC	AI	992.55	
J1-79	HPOUTL_F13	F13	1.8V/HPVCC	AO	974.13	

J1-2	DGND	-	GND	PWR	-	
J1-4	PD0_W19	W19	3.3V/1.8V/VCC-PD	I/O	2479.68	
J1-6	PD1_V20	V20	3.3V/1.8V/VCC-PD	I/O	2479.06	
J1-8	PD2_V19	V19	3.3V/1.8V/VCC-PD	I/O	2480.08	
J1-10	PD3_U20	U20	3.3V/1.8V/VCC-PD	I/O	2477.17	
J1-12	PD4_U19	U19	3.3V/1.8V/VCC-PD	I/O	2475.70	
J1-14	PD5_U18	U18	3.3V/1.8V/VCC-PD	I/O	2471.10	
J1-16	DGND	-	GND	PWR	-	
J1-18	PD6_T19	T19	3.3V/1.8V/VCC-PD	I/O	2471.53	
J1-20	PD7_T18	T18	3.3V/1.8V/VCC-PD	I/O	2473.90	
J1-22	PD8_R20	R20	3.3V/1.8V/VCC-PD	I/O	2480.29	
J1-24	PD9_R19	R19	3.3V/1.8V/VCC-PD	I/O	2477.63	

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J1-26	PD10_T17	T17	3.3V/1.8V/VCC-PD	I/O	2476.84	
J1-28	PD11_R17	R17	3.3V/1.8V/VCC-PD	I/O	2473.99	
J1-30	DGND	-	GND	PWR	-	
J1-32	PD12_P19	P19	3.3V/1.8V/VCC-PD	I/O	2465.41	
J1-34	PD13_P18	P18	3.3V/1.8V/VCC-PD	I/O	2465.87	
J1-36	PD14_N17	N17	3.3V/1.8V/VCC-PD	I/O	2477.64	
J1-38	PD15_N16	N16	3.3V/1.8V/VCC-PD	I/O	2481.07	
J1-40	PD16_N20	N20	3.3V/1.8V/VCC-PD	I/O	2465.31	
J1-42	PD17_N19	N19	3.3V/1.8V/VCC-PD	I/O	2461.80	
J1-44	DGND	-	GND	PWR	-	
J1-46	PD18_M19	M19	3.3V/1.8V/VCC-PD	I/O	2466.16	
J1-48	PD19_M18	M18	3.3V/1.8V/VCC-PD	I/O	2470.49	
J1-50	PD20_W18	W18	3.3V/1.8V/VCC-PD	I/O	2466.39	
J1-52	PD21_V18	V18	3.3V/1.8V/VCC-PD	I/O	2411.73	
J1-54	DGND	-	GND	PWR	-	
J1-56	DGND	-	GND	PWR	-	
J1-58	LRADC_B12	B12	1.8V/AVCC	AI	1318.08	51KΩpullup
J1-60	GPADC0_C13	C13	1.8V/AVCC	AI	984.16	
J1-62	GPADC1_B13	B13	1.8V/AVCC	AI	908.89	
J1-64	DGND	-	GND	PWR	-	
J1-66	TP_X1_C12	C12	1.8V/AVCC	AI	1027.47	1nFpulldown
J1-68	TP_X2_A11	A11	1.8V/AVCC	AI	881.54	1nFpulldown
J1-70	TP_Y1_B11	B11	1.8V/AVCC	AI	944.49	1nFpulldown
J1-72	TP_Y2_C11	C11	1.8V/AVCC	AI	1001.70	1nFpulldown
J1-74	DGND	-	GND	PWR	-	
J1-76	TVIN0_B9	B9	1.8V/VCC-TVIN	AI	879.31	
J1-78	TVIN1_C9	C9	1.8V/VCC-TVIN	AI	881.58	
J1-80	TVOUT0_E19	E19	1.8V/VCC-TVOUT	AO	1201.98	

J2-1	DGND	-	GND	PWR	-	
J2-3	REFCLK_OUT_J2	J2	1.8V/VCC-DCXO	AO	706.68	
J2-5	FEL_A18	A18	3.3V/VCC-IO	DI	2676.60	1KΩinseries
J2-7	NMI_N3	N3	1.8V/VCC-RTC	I/O, OD	598.38	
J2-9	RESET_M2	M2	1.8V/VCC-RTC	I, OD	1649.92	10KΩpullup
J2-11	DGND	-	GND	PWR	-	
J2-13	PG0_B2	B2	3.3V/1.8V/VCC-PG	I/O	1629.81	
J2-15	PG1_B3	B3	3.3V/1.8V/VCC-PG	I/O	1627.95	
J2-17	PG2_A3	A3	3.3V/1.8V/VCC-PG	I/O	1643.19	
J2-19	PG3_C3	C3	3.3V/1.8V/VCC-PG	I/O	1614.27	
J2-21	PG4_A4	A4	3.3V/1.8V/VCC-PG	I/O	1616.79	
J2-23	PG5_B4	B4	3.3V/1.8V/VCC-PG	I/O	1613.06	

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J2-25	DGND	-	GND	PWR	-	
J2-27	PG6_B5	B5	3.3V/1.8V/VCC-PG	I/O	1614.76	
J2-29	PG7_C5	C5	3.3V/1.8V/VCC-PG	I/O	1612.58	
J2-31	PG8_A6	A6	3.3V/1.8V/VCC-PG	I/O	1637.74	
J2-33	PG9_B6	B6	3.3V/1.8V/VCC-PG	I/O	1611.97	
J2-35	PG10_C6	C6	3.3V/1.8V/VCC-PG	I/O	1626.49	
J2-37	PG11_D4	D4	3.3V/1.8V/VCC-PG	I/O	1104.04	
J2-39	DGND	-	GND	PWR	-	
J2-41	PG12_D5	D5	3.3V/1.8V/VCC-PG	I/O	1611.28	
J2-43	PG13_D6	D6	3.3V/1.8V/VCC-PG	I/O	1037.57	
J2-45	PG14_E6	E6	3.3V/1.8V/VCC-PG	I/O	1012.96	
J2-47	PG15_F6	F6	3.3V/1.8V/VCC-PG	I/O	1069.79	
J2-49	PG16_F7	F7	3.3V/1.8V/VCC-PG	I/O	1145.86	
J2-51	PG17_E7	E7	3.3V/1.8V/VCC-PG	I/O	1014.18	
J2-53	PG18_D7	D7	3.3V/1.8V/VCC-PG	I/O	1270.70	
J2-55	DGND	-	GND	PWR	-	
J2-57	DGND	-	GND	PWR	-	
J2-59	VDD_3V3_SOM	-	3.3V/VIO	PWR	-	
J2-61	DGND	-	GND	PWR	-	
J2-63	VDD_1V8_SOM	-	1.8V/VIO	PWR	-	
J2-65	DGND	-	GND	PWR	-	
J2-67	DGND	-	GND	PWR	-	
J2-69	V5_IN	-	5V/VIN	PWR	-	
J2-71	V5_IN	-	5V/VIN	PWR	-	
J2-73	V5_IN	-	5V/VIN	PWR	-	
J2-75	V5_IN	-	5V/VIN	PWR	-	
J2-77	V5_IN	-	5V/VIN	PWR	-	
J2-79	V5_IN	-	5V/VIN	PWR	-	

J2-2	DGND	-	GND	PWR	-	
J2-4	USB1_DP_A8	A8	3.3V/VCC-IO	A I/O	662.06	
J2-6	USB1_DM_B8	B8	3.3V/VCC-IO	A I/O	665.84	
J2-8	DGND	-	GND	PWR	-	
J2-10	DGND	-	GND	PWR	-	
J2-12	USB0_DP_B7	B7	3.3V/VCC-IO	A I/O	747.38	
J2-14	USB0_DM_C7	C7	3.3V/VCC-IO	A I/O	750.80	
J2-16	DGND	-	GND	PWR	-	
J2-18	DGND	-	GND	PWR	-	
J2-20	PF0_C2	C2	3.3V/1.8V/VCC-PF	I/O	786.62	
J2-22	PF1_C1	C1	3.3V/1.8V/VCC-PF	I/O	756.27	
J2-24	PF2_D2	D2	3.3V/1.8V/VCC-PF	I/O	770.05	33 Ω inseries

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J2-26	PF3_D1	D1	3.3V/1.8V/VCC-PF	I/O	767.31	
J2-28	PF6_D3	D3	3.3V/1.8V/VCC-PF	I/O	750.93	
J2-30	PF5_E2	E2	3.3V/1.8V/VCC-PF	I/O	754.76	
J2-32	PF4_E3	E3	3.3V/1.8V/VCC-PF	I/O	770.77	
J2-34	DGND	-	GND	PWR	-	
J2-36	DGND	-	GND	PWR	-	
J2-38	PE17_M6	M6	3.3V/1.8V/VCC-PE	I/O	674.78	
J2-40	PE12_R5	R5	3.3V/1.8V/VCC-PE	I/O	847.87	
J2-42	PE14_N4	N4	3.3V/1.8V/VCC-PE	I/O	851.84	
J2-44	PE15_N5	N5	3.3V/1.8V/VCC-PE	I/O	838.51	
J2-46	PE16_N6	N6	3.3V/1.8V/VCC-PE	I/O	691.00	
J2-48	PE11_N1	N1	3.3V/1.8V/VCC-PE	I/O	858.70	
J2-50	DGND	-	GND	PWR	-	
J2-52	PE10_P3	P3	3.3V/1.8V/VCC-PE	I/O	849.43	
J2-54	PE9_P2	P2	3.3V/1.8V/VCC-PE	I/O	841.70	
J2-56	PE8_R3	R3	3.3V/1.8V/VCC-PE	I/O	841.12	
J2-58	PE6_R1	R1	3.3V/1.8V/VCC-PE	I/O	838.60	
J2-60	PE7_R2	R2	3.3V/1.8V/VCC-PE	I/O	856.49	
J2-62	PE13_R4	R4	3.3V/1.8V/VCC-PE	I/O	854.81	
J2-64	DGND	-	GND	PWR	-	
J2-66	PE4_T2	T2	3.3V/1.8V/VCC-PE	I/O	870.30	
J2-68	PE5_T3	T3	3.3V/1.8V/VCC-PE	I/O	837.22	
J2-70	PE1_U1	U1	3.3V/1.8V/VCC-PE	I/O	875.94	
J2-72	PE2_U2	U2	3.3V/1.8V/VCC-PE	I/O	838.40	
J2-74	PE0_V1	V1	3.3V/1.8V/VCC-PE	I/O	857.64	
J2-76	PE3_U3	U3	3.3V/1.8V/VCC-PE	I/O	873.56	
J2-78	DGND	-	GND	PWR	-	
J2-80	DGND	-	GND	PWR	-	

Notes:

- AI: analog input;
- AO: analog output;
- DI: digital input;
- DO: digital output;
- I/O: digital input and output;
- PWR: power supply;
- alignment length in mil;

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- Detailed BTB connector pin multiplexing functions can be viewed in the “ECK30-T13IC Pin List” document.

4.3.2. I/O impedance control

ECK30-T13IC series core board all high-speed signals in the PCB design have done impedance control and length control, core board alignment impedance control parameters are shown in the table below.

Alignment Impedance Control Table

No	Impedance Control Alignment Classification	Impedance Controls	Typical Model Network Name
1	USB differential signaling	90±10%Ω	USB1_DP_A8/USB1_DM_B8
2	LVDS, MIPI differential signals	100±10%Ω	PD0_W19/PD1_V20
3	Analog video input and output signals	37.5±10%Ω	TVOUT0_E19、TVIN1_C9、TVIN0_B9
4	General Single-Ended Alignment	50±10%Ω	

4.4. Electrical characteristics

4.4.1. Power consumption

Note: The following parameters are measured on the ECK30-T13IC5E8-I core board in a room temperature environment, and the measured power consumption does not include the backplane power consumption, and the measurement of the heavy load power consumption runs the memory and eMMC test program, no display, no backplane SDIO access, and no network access. The following power consumption data is for reference only, as test methods, usage functions, ambient temperature and other factors may affect power consumption.

Power Consumption Table

Power status	Test environments	Supply Voltage	Voltages	Electric consumption
BOOT	During UBOOT operation	5.0V	0.169A	0.845W
PWRUP	Entering the system without run	5.0V	0.104A	0.52W

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	ning the application			
PWRUP	Software reload test	5.0V	0.203A	1.015W
SLEEP	Freeze mode hibernation	5.0V	0.087A	0.435W
SLEEP	Mem mode hibernation	5.0V	0.056A	0.28W

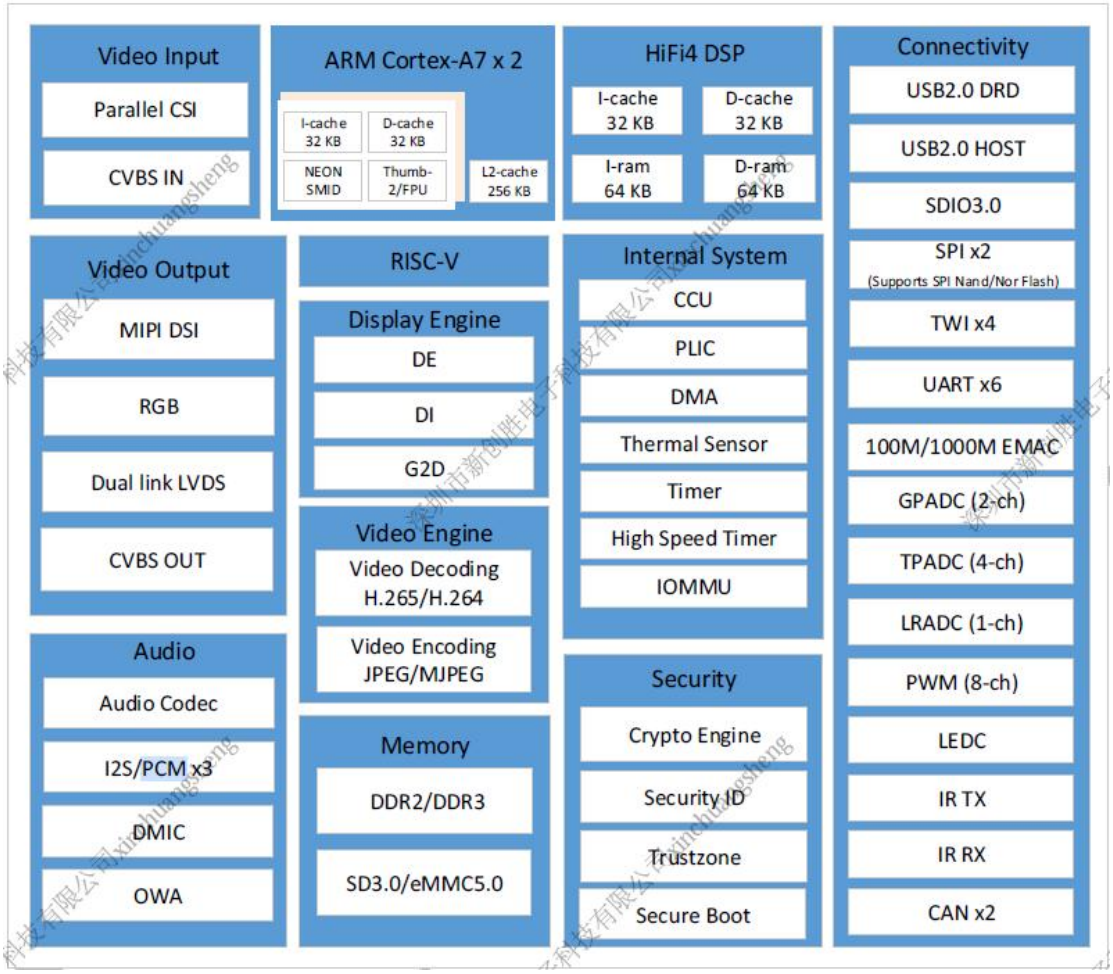
5. Core board hardware design

5.1. Processor

The core board of ECK30-T13IC series uses the T113-i processor from Allwinner Tec hnology's T113 series as the core.The T113-i processor is an advanced application process or designed for RISC-V multimedia decoding platforms.It integrates three heterogeneous pr ocessors, RISC-V, dual-core ARM Cortex-A7 and HiFi4 DSP, to provide efficient computin g power. It integrates three kinds of heterogeneous processors, namely RISC-V, dual-core ARM Cortex-A7 and HiFi4 DSP, which can provide highly efficient computational power. T113-i supports full-format decoding such as H.265, H.264, MPEG-1/2/4, JPEG, VC1, etc. The independent encoder can encode JPEG and VC1. The standalone encoder can encode JPEG or MJPEG.The integrated ADC/DAC and I2S/PCM/DMIC/OWA audio interfaces wo rk seamlessly with the CPU to accelerate the application of multimedia algorithms and im prove the user experience.The T113-i supports a wide range of display output interfaces su ch as RGB/LVDS/MIPI DSI/CVBS OUT to meet the needs of different screens and displa y connections. The T113-i has rich expansion interfaces such as CAN, USB, SDIO, EMA C, TWI, UART, SPI, PWM, GPADC, LRADC, TPADC, IR TX&RX, etc. The T113-i can also be used as an interface to connect to a variety of display outputs, such as RGB/LV DS/MIPI DSI/CVBS OUT, to meet different screen and display connectivity requirements. In addition, the T113-i can be connected to other different peripherals such as WiFi and Bluetooth via SDIO and UART.The functional block diagram of the T113-i processor is sh own below.

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T113-i System Function Block Diagram

5.1.1. Processor Architecture

T113-i processor adopts multi-core heterogeneous design, integrating three kinds of heterog eneous processors: RISC-V, dual-core ARM Cortex-A7 and HiFi4 DSP. The relevant parameters are shown in the table below.

T113-i Processor Architecture Parameter Table

Function	Functional parameters
ARM	Dual-core ARM CortexTM-A7, 1.2GHz; 32 KB I-cache + 32 KB D-cache + NEON SIMD + Thumb 2/FPU + 256 KB L2 cache;
RISC-V	RISC-V CPU, 1008MHz; 32 KB I-cache + 32 KB D-cache;
DSP	HiFi4 DSP, 600MHz; 32 KB L1 I-cache and 32 KB L1 D-cache; 64 KB I-ram and 64 KB D-ram;

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5.2. Memory

ECK30-T13IC series core boards have one DDR3 SDRAM memory chip mounted on board. Designed for 16-bit memory data bit width, 256MB/512MB/1GB three kinds of capacity options. Designed memory are used domestic industrial grade devices. The memory chip models are listed in the table below.

Memory Chip Selection Chart

Factory	Model number	Monolithic capacity	Operating temperature
Longsys	F60C1A0002-M69W	2Gbit	-40℃ ~ 95℃
GigaDevice	GDP1BFLA-WB	2Gbit	-40℃ ~ 95℃
Longsys	F60C1A0004-M79W	4Gbit	-40℃ ~ 95℃
GigaDevice	GDP2BFLM-WB	4Gbit	-40℃ ~ 95℃
GigaDevice	GDP3BELM-WB	8Gbit	-40℃ ~ 95℃

Note: The specific mounted memory chip model is subject to the physical object.

5.3. Clock

ECK30-T13IC series core boards provide one 32.768KHz crystal (passive) oscillator circuit and one 24MHz crystal (passive) oscillator circuit on-board as the processor system clock source.

5.4. Storage

ECK30-T13IC series core boards are designed with two storage schemes on board, one is SPI FLASH storage scheme. One is SPI FLASH storage scheme. This storage scheme selects SLC NAND FLASH chip as the storage medium, which is characterized by low cost and high reliability. The other is eMMC storage scheme. This storage scheme uses eMMC chip as the storage medium, which is characterized by large storage capacity, low unit storage cost and easy to use. Since the two storage solutions reuse the same I/O resources, one model of core board only supports one storage solution. Users need to choose the corresponding model of core board according to the storage requirements of specific projects.

SPI NAND FLASH is connected to the processor via SPI0 bus. The device adopts GD5F2GM7UEYIGR (256MB) industrial grade SPI NAND FLASH from GigaDevice.

The eMMC memory is connected to the processor via the SMHC (SDC2) bus. The devic

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e adopts domestic industrial-grade eMMC memory chip, and the chip model is shown in the f ollowing table.

Emmc Chip Selection Table

Factory	Model number	Capacity	Operating temperature
Longsys	FEMDRW008G-88A39	8GB	-40℃ ~ 85℃
YEESTOR	SGM8000I-S27B8G	8GB	-40℃ ~ 85℃

Note: The specific mounted memory chip model is subject to the physical object.

5.5. LED

Two LEDs are mounted on the back of the core board and can be used for status an d operation indication. 2 LEDs are programmable indication LEDs corresponding to the F2 /PC0 and F1/PC1 pins, which are illuminated at high level respectively.

5.6. Power supply

The ECK30-T13IC series core boards use a split power supply scheme and are desig ned in strict accordance with the voltage, power and timing requirements in the T113-i m anual.The ECK30-T13IC series core boards are powered by a single DC +5V power suppl y, and the external power supply needs to be supplied with only one power input of V5_ IN, while the other power supplies are generated internally by the core boards without the need for additional power supply.

ECK30-T13IC series core boards also provide two power outputs, VDD_3V3_SOM an d VDD_1V8_SOM, which can be used for power supply of low-power devices and power -up timing control of I/O interfaces on the base board. The parameters of the two output power supplies are shown in the following table.

Output power supply parameter table

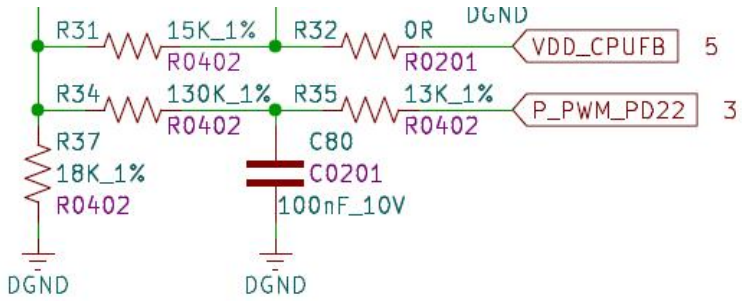
Power Network Name	Power supply type	power domain	Typical Voltage	max. current
VDD_3V3_SOM	BUCK	VIO	3.3V	500mA
VDD_1V8_SOM	LDO	VIO	1.8V	100mA

ECK30-T13IC series core board VDD-CPU power supply design supports the DVFS

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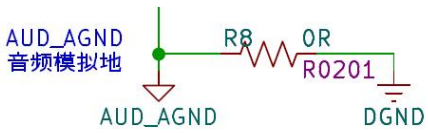
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dynamic FM voltage regulation function. The hardware design uses the PWM function of the processor PD22 pin as the control pin for DVFS dynamic FM voltage regulation. The software should pay attention to the configuration of the PD22 pin and the DVFS function during I/O hardware configuration and function configuration. The related hardware schematic diagram is as follows.



ECK30-T13IC series core boards are not designed with a battery backup RTC function on board, so there is no RTC power interface on the core board. If battery-powered RTC function is required, it can be realized by expanding the RTC chip on the backplane via a I2C bus.

ECK30-T13IC series core board provides two kinds of power ground pins, respectively, the digital signal ground DGND and audio analog signal ground AUGND. the power supply power ground and digital signals are referenced to DGND, and audio analog signals are referenced to AUGND. the two kinds of ground in the core board adopts a single point of connection, the principle of which is shown in the following figure.

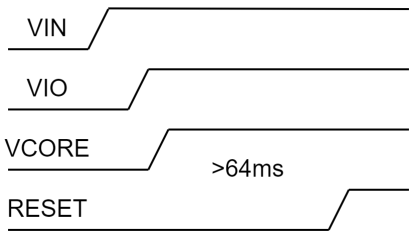


Schematic diagram of AUGND single point grounding

ECK30-T13IC series core board power domain and power-on timing is very simple, the main power domain is only VIN, VIO and VCORE three parts, of which VCORE is only related to the processor, and the user I/O interface has nothing to do with the application. The VCORE is only related to the processor, but not to the user I/O interface, so it is not a concern for the application.The ECK30-T13IC series core board power-on timing is shown in the following figure.

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Core board power-up timing diagram

All external I/O interfaces of the ECK30-T13IC series core board belong to the VIO power domain, and the base board can use the VDD_3V3_SOM or VDD_1V8_SOM power supply output from the core board to be used as a control signal for the power domain of the I/O interfaces of the base board.

5.7. On-Board I/O Assignment

Some of the functions on the ECK30-T13IC series core board occupy the I/O functions of the T113-i processor, which are not led to the BTB connector, and the user should pay attention to the function configuration of these I/Os during the software configuration. The specific occupied I/Os are shown in the following table.

Core Board On-Board Multiplexing I/O Allocation Table

MPU I/O pinout	network name	Core Board Functional Description
Y18	P_PWM_PD22	DVFS PWM
F2	LED1	On-Board User LED1
F1	LED2	On-board user LED2
G3	PC2_eCLK_SCLK	eMMC CLK / SPI0 CLK
G2	PC3_eCMD_SCS	eMMC CMD / SPI0 CS
H3	PC4_eD2_SMOSI	eMMC DATA2 / SPI0 MOSI
F5	PC5_eD1_SMISO	eMMC DATA1 / SPI0 MISO
G6	PC6_eD0_SWP	eMMC DATA0 / SPI0 WP
G5	PC7_eD3_SHOLD	eMMC DATA3 / SPI0 HOLD

6. Baseboard hardware design

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6.1. Power Interface

For embedded product design, the design of the power supply system is crucial, not only need to consider the basic electrical parameters of the power supply itself, but also consider the stability design of the power supply, timing design and many other factors. ECK30-T13IC series core board adopts a single power supply scheme and provides power timing management signals to simplify the user's baseboard power supply design as much as possible.

6.1.1. Power input

The ECK30-T13IC series core boards are powered by a single DC +5V power supply, corresponding to the J2-69, J2-71, J2-73, J2-75, J2-77, J2-79 pins of the BTB connector, and the power supply pin is named V5_IN. the power supply voltage range is 5.0V ±10%. the ECK30-T13IC series core boards' normal power consumption is 1W. The normal power consumption of the ECK30-T13IC series core board is about 1W. When designing the power supply for the core board, it is necessary to consider the power consumption of the I/O output and the increase in power consumption when more functions are running at the same time, as well as the increase in power consumption of components at high temperatures, so it is recommended that the core board power supply current design should not be less than 0.5A.

If the DC-DC power supply to the core board power supply, power supply power margin should not be too large in the power supply design. If the power supply design power is too large, many power supplies to ensure conversion efficiency, will work in discontinuous PWM mode, the output power ripple will increase significantly, not conducive to the stability of the digital signal system. If the LDO is used to supply power to the core board, the design should take into account the LDO's own power loss and operating temperature rise, to prevent the LDO power supply over-temperature to stop working or burned when working in a high-temperature environment or poor heat dissipation.

6.1.2. Power output

ECK30-T13IC series core boards also provide two power outputs, VDD_3V3_SOM an

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d VDD_1V8_SOM, which can be used for power supply of low-power devices on the baseboard and power-up timing control of the baseboard I/O interfaces.

6.1.3. Power control

All external I/O interfaces of the ECK30-T13IC series core board belong to the VIO power domain, and the base board can use the VDD_3V3_SOM or VDD_1V8_SOM power supply output from the core board to be used as a control signal for the power domain of the I/O interfaces of the base board.

6.1.4. Pin Definitions

Power Supply Pin Definition Table

Pin	Network name	MPU	Level/Power Rails	Typology	Alignment length（mil）	Description
J1-41	AUGND		-	PWR		
J1-59	AUGND		-	PWR		
J1-69	AUGND		-	PWR		
J2-59	VDD_3V3_SOM		3.3V / VIO	PWR		Maximum supply current 500 mA
J2-63	VDD_1V8_SOM		1.8V / VIO	PWR		Maximum supply current 100 mA
J2-69	V5_IN		5V / VIN	PWR		
J2-71	V5_IN		5V / VIN	PWR		
J2-73	V5_IN		5V / VIN	PWR		
J2-75	V5_IN		5V / VIN	PWR		
J2-77	V5_IN		5V / VIN	PWR		
J2-79	V5_IN		5V / VIN	PWR		

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6.2. Startup Configuration

6.2.1. Startup Sequence Configuration

When the ECK30-T13IC series core board boots up, the processor reads the status of BOOT_Select and selects the order in which to enumerate the media.The T113 processor has 2 BOOT_Select pins multiplexed with the PC pins, with a default internal pull-up, and the boot configuration relationships are shown in the following table.

T113 Boot Select configuration table

ECK30-T13IC Storage Configuration	PC5 BOOT-SEL1	PC4 BOOT-SEL0	Boot Media
--	0	0	SPI NOR => SPI NAND
--	0	1	SMHC0 => SPI NOR => Other media
SPI NAND memory	1	0	SMHC0 => SPI NAND => Other media
eMMC memory	1	1	SMHC0 => eMMC2 => Other media

ECK30-T13IC series core boards PC5 and PC4 do not lead out to the BTB connector, the core boards already have the boot sequence configured and do not require user backplane configuration. All ECK30-T13IC series core boards are configured to prioritize booting from SMHC0, and the subsequent enumeration order varies depending on the on-board storage method, as shown in the table above.

6.2.2. FEL Pin

ECK30-T13IC series core boards support firmware forced burn-in pin FEL. Ground the FEL signal when the ECK30-T13IC series core boards are not powered on, and release FEL after powering on the ECK30-T13IC series core boards, the ECK30-T13IC series core boards will enter the firmware upgrade mode. Users can design keys or jumpers on the backplane to ground the FEL signal to force the processor into firmware upgrade mode. Since the signal has been designed with pull-up resistors on the core board, the backplane design only needs to consider grounding and proper TVS protection, do not design arbitrary pull-up resistors on the backplane for the FEL signal. If the FEL signal is not used, the signal can be handled in suspension and the firmware can be upgraded via the SD card.

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6.2.3. Pin Definitions

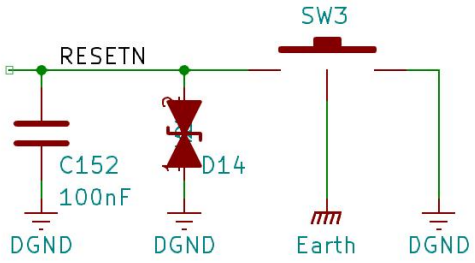
Startup Configuration Pin Definition Table

Pin	network name	MPU	Level/Power Rails	typology	Alignment length（mil）	Description
2	FEL_A18	A18	3.3V/VCC-IO	DI		Series 1KΩ resistor

6.3. Reset button

The RESET_M2 signal from the ECK30-T13IC series core board can be connected to an external keypad for reset control of the processor.The RESET_M2 signal is a bi-directional input/output signal that can be used as an external reset input to reset the processor, and is also the processor's memory power supply reset signal output.The RESET_M2 signal is supplied with a 10K ohm The RESET_M2 signal is provided with a 10K ohm pull-up resistor in the core board. Therefore, when applying the RESET_M2 signal as a manual reset input on the base board, do not connect the pull-up resistor again, connect the key directly, or drive it through the OD gate. Also do not drive the RESET_M2 signal through the push-pull output connector. When connecting a manual input keypad, small capacitors and TVS can be placed to minimize interference and improve ESD performance. The keypad reference schematic is shown below.

6.3.1. 6.3.1 Reference Circuit



Note: Do not arbitrarily pull up the reset and power button signals through resistors. An incorrect pull-up of the power rail can cause indeterminate signals to be input to the key signal interface when the system is in standby or shutdown.

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6.3.2. Pin Definition

Key Pin Definition Table

Pin	network name	MPU	Level/Power Rails	typology	Alignment length（mil）	clarification
4	RESET_M2	M2	1.8V/VCC-RTC	I, OD		10KΩ pull up

6.3.3. LAYOUT recommendations

- The reset signals are sensitive signals and can be handled in packet land or away from signals with high interference;
- The reset signal TVS tube is placed as close as possible to the keys.

6.4. Reference Clock and NMI

6.4.1. REFCLK_OUT

The processor DCXO clock module can fan out a clock signal at the same frequency as the master clock through the REFCLK_OUT_J2 pin. This clock signal can be provided to devices on the backplane for clock input, such as a WiFi module. When using this clock reference output consider whether the clock level, accuracy, and power-up sequence are suitable for the baseboard device. If not satisfied, it is recommended not to use this clock signal.

6.4.2. NMI

Processor non-maskable interrupt signal, mainly used for PMIC management. This pin function is not recommended for user use. It can be left dangling for processing when not in use.

6.4.3. Pin Definition

Key Pin Definition Table

Pin	network name	MPU	Level/Power Rails	typology	Alignment length（mil）	clarification

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1	REFCLK_OUT_J2	J2	1.8V/VCC-DCXO	AO		
3	NMI_N3	N3	1.8V/VCC-RTC	I/O, OD		

6.5. Display Output Interface

ECK30-T13IC series core board supports RGB888 (RGB666), dual-channel LVDS (multiple xed pins with RGB interface), MIPI DSI (multiplexed pins with RGB interface), and SPI (DBI) display interfaces.If only one set of LVDS is used on the PD I/O, the other PD's I/O can be used as normal I/O.

The dual-channel LVDS interface supports up to 1920×1080@60fps;

Single-channel LVDS interface supports up to 1366×768@60fps;

Parallel RGB interface supports up to 1920×1080@60fps;

SPI interface supports up to 240×320@60fps;

4-lane MIPI DSI interface supports up to 1920×1200@60fps.

The multiplexing relationship between the DBI interface and SPI1 is shown in the table b elow.

DBI and SPI1 Multiplexing Table

DBI function	SPI1 function
DBI-CSX	SPI1-CS
DBI-SCLK	SPI1-CLK
DBI-SDO/SDA	SPI1-MOSI
DBI-SDI(WRX)/TE/DCX	SPI1-MISO
DBI-DCX/WRX	SPI1-HOLD
DBI-TE	SPI1-WP

Customers can configure the display resolution and display data format according to their needs. The screen application can use GPIO to control the screen power and backlight power. Backlight brightness can be controlled using PWM output. You can also use I2C and GPIO ex ternal interrupt function to connect the touch screen. You can use the LCD touch screen modu le of EVERBUILT with it, and the related module information can be found in the official we bsite https://www.ebyte.com/.

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6.6. Interface Definition

Display Interface Definition Table

Pin	Network name	MPU	Level/Power Rails	Typology	Alignment length（mil）	Description
58	PB2_M16	M16	3.3V/VCC-IO	I/O	2466.60	LCD0_D0
59	PB3_M15	M15	3.3V/VCC-IO	I/O	2462.52	LCD0_D1
67	PD0_W19	W19	3.3V/VCC-PD	I/O	2479.68	LCD0_D2/LVDS0_V0P/DSI_D0P
68	PD1_V20	V20	3.3V/VCC-PD	I/O	2479.06	LCD0_D3/LVDS0_V0N/DSI_D0N
69	PD2_V19	V19	3.3V/VCC-PD	I/O	2480.08	LCD0_D4/LVDS0_V1P/DSI_D1P
70	PD3_U20	U20	3.3V/VCC-PD	I/O	2477.17	LCD0_D5/LVDS0_V1N/DSI_D1N
72	PD4_U19	U19	3.3V/VCC-PD	I/O	2475.70	LCD0_D6/LVDS0_V2P/DSI_CKP
73	PD5_U18	U18	3.3V/VCC-PD	I/O	2471.10	LCD0_D7/LVDS0_V2N/DSI_CKN
60	PB4_K16	K16	3.3V/VCC-PD	I/O	2471.63	LCD0_D8
61	PB5_K15	K15	3.3V/VCC-PD	I/O	2456.12	LCD0_D9
74	PD6_T19	T19	3.3V/VCC-PD	I/O	2471.53	LCD0_D10/LVDS0_CKP/DSI_D2P
75	PD7_T18	T18	3.3V/VCC-PD	I/O	2473.90	LCD0_D11/LVDS0_CKN/DSI_D2N
76	PD8_R20	R20	3.3V/VCC-PD	I/O	2480.29	LCD0_D12/LVDS0_V3P/DSI_D3P
77	PD9_R19	R19	3.3V/VCC-PD	I/O	2477.63	LCD0_D13/LVDS0_V3N/DSI_D3N
79	PD10_T17	T17	3.3V/VCC-PD	I/O	2476.84	LCD0_D14/LVDS1_V0P
80	PD11_R17	R17	3.3V/VCC-PD	I/O	2473.99	LCD0_D15/LVDS1_V0N
62	PB6_K17	K17	3.3V/VCC-PD	I/O	2463.43	LCD0_D16
63	PB7_J15	J15	3.3V/VCC-PD	I/O	2467.88	LCD0_D17

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81	PD12_P19	P19	3.3V/VCC-PD	I/O	2465.41	LCD0_D18/LVDS1_V1P
82	PD13_P18	P18	3.3V/VCC-PD	I/O	2465.87	LCD0_D19/LVDS1_V1N
83	PD14_N17	N17	3.3V/VCC-PD	I/O	2477.64	LCD0_D20/LVDS1_V2P
84	PD15_N16	N16	3.3V/VCC-PD	I/O	2481.07	LCD0_D21/LVDS1_V2N
86	PD16_N20	N20	3.3V/VCC-PD	I/O	2465.31	LCD0_D22/LVDS1_CKP
87	PD17_N19	N19	3.3V/VCC-PD	I/O	2461.8	LCD0_D23/LVDS1_CKN
88	PD18_M19	M19	3.3V/VCC-PD	I/O	2466.16	LCD0_CLK/LVDS1_V3P
89	PD19_M18	M18	3.3V/VCC-PD	I/O	2470.49	LCD0_DE/LVDS1_V3N
90	PD21_V18	V18	3.3V/VCC-PD	I/O	2411.73	LCD0_VSYNC
91	PD20_W18	W18	3.3V/VCC-PD	I/O	2466.39	LCD0_HSYNC

6.7. LAYOUT recommendations

- Data and time clock differential pairs need to follow the rule of equal length and distance, differential pair error control +-5 mil, differential impedance 100 ohms;
- Differential alignments should be less perforated to ensure that differential pairs are perforated at the same time, and ground holes should be placed next to the differential pair perforations;
- Data differential pairs need to be equalized between groups using the clock differential pairs as a reference, with +-50 mil equalization;
- The differential alignment reference plane should be complete and the alignment should not be split across;
- If the backplane RGB signals are designed with series matching resistors, it is recommended to place them close to the core board BTB connector;
- RGB signals in the core board has been done in equal length processing, core board alignment length see pin definition table;

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- RGB signals in the core board in accordance with the single-ended 50Ω ± 10% imped ance control, impedance control of the base plate is recommended to maintain the sa me;
- It is recommended that the base plate RGB signal alignment to do isometric control, er ror range ± 25mil, signal line spacing at least 2W.

6.8. Digital camera interface

ECK30-T13IC series core board CSI interface supports 8bit DVP interface, BT656 int erface and BT601 interface inputs, parallel CSI interface can support a maximum pixel clo ck of 148.5MHz, and the BT656 interface supports 2*1080p@30fps inputs in clock double -edge sampling mode.ECK30-T13IC series core boards The CSI interface only supports 3.3 V I/O level.

In the actual baseboard application, parallel CSI interface will occupy a large number of I/O pins, reducing other multiplexing functions, you can consider using the USB interf ace camera to realize the camera function.

6.9. Interface Definitions

Digital Camera Interface Definition Table

Pin	Network name	MPU	Level/Power Rails	Typology	Alignment length（mil）	Description
48	PE0_V1	V1	3.3V/VCC-PE	I/O	857.64	CSI Horizontal Sync Signal
49	PE1_U1	U1	3.3V/VCC-PE	I/O	875.94	CSI Vertical Synchron ization Signal
50	PE2_U2	U2	3.3V/VCC-PE	I/O	838.40	CSI Pixel Clock
51	PE3_U3	U3	3.3V/VCC-PE	I/O	873.56	CSI Master Clock
36	PE4_T2	T2	3.3V/VCC-PE	I/O	870.30	CSI Data Bit0
37	PE5_T3	T3	3.3V/VCC-PE	I/O	837.22	CSI Data Bit1
38	PE6_R1	R1	3.3V/VCC-PE	I/O	838.60	CSI Data Bit2
39	PE7_R2	R2	3.3V/VCC-PE	I/O	856.49	CSI Data Bit3
40	PE8_R3	R3	3.3V/VCC-PE	I/O	841.12	CSI Data Bit4
41	PE9_P2	P2	3.3V/VCC-PE	I/O	841.70	CSI Data Bit5
42	PE10_P3	P3	3.3V/VCC-PE	I/O	849.43	CSI Data Bit6

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43	PE11_N1	N1	3.3V/VCC-PE	I/O	858.70	CSI Data Bit7

6.10. LAYOUT recommendations

- CSI signals in the core board has been done equal length processing, core board alignment length see pin definition table;
- CSI signals in the core board in accordance with the single-ended 50Ω ± 10% impedance control, the impedance control of the base plate is recommended to maintain the same;
- It is recommended that the bottom plate CSI signal alignment to do isometric control, error range ± 25mil, signal line spacing of at least 2W.

6.11. SD/MMC card interface

ECK30-T13IC series core boards are equipped with 3-way SMHC (SD/MM host controller) controllers, including SMHC0, SMHC1, and SMHC2. SMHC0 is compliant with Secure Digital Memory v3.0 protocol and is usually used to connect to an SD card. SMHC1 is compliant with Secure Digital I/O v3.0 protocol and is usually used to connect to an expansion function such as a WiFi module. SMHC1 is compliant with Secure Digital I/O v3.0 protocol and is typically used for connecting extended functions such as WiFi modules. SMHC2 is compliant with Multimedia Card v5.0 protocol and is typically used for connecting eMMC memory chips. the ECK30-T13IC series cores use SMHC2 to extend the on-board eMMC memory chips. It is recommended that the backplane use SMHC0 to connect to the SD card. SMHC1 is recommended to extend other devices or not to be used.

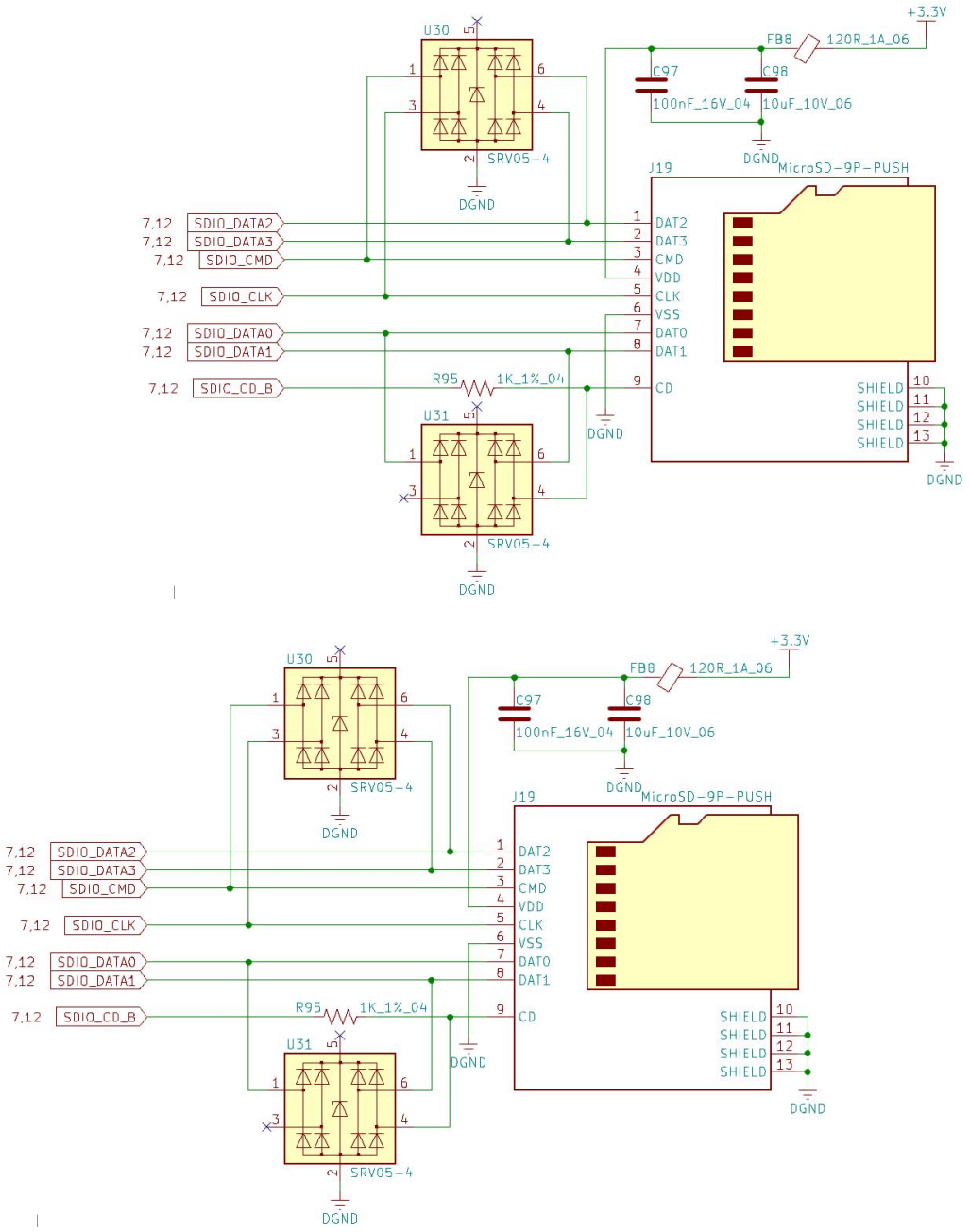
The processor's I/O can be configured with on-chip pull-up resistors. These pull-up resistors can meet the pull-up requirements for SD card interface expansion, and no external pull-up resistors are required for user design. The core board has a 33 ohm matching resistor in series on the clock signal of PF2_D2, so user designs do not need an external series resistor either. To expand Micro SD card through SMHC0 interface, please refer to th

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e following schematic design.

6.12. Reference Circuit



6.13. Pin Definitions

SMHC0 Interface Signal Pin Definitions

Pin	Network name	MPU	Level/Power Rails	Typology	Alignment length（mil）	Description
28	PF1_C1	C1	3.3V/VCC-PF	I/O	756.27	SDC0_D0

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27	PF0_C2	C2	3.3V/VCC-PF	I/O	786.62	SDC0_D1
30	PF5_E2	E2	3.3V/VCC-PF	I/O	754.76	SDC0_D2
32	PF4_E3	E3	3.3V/VCC-PF	I/O	770.77	SDC0_D3
31	PF3_D1	D1	3.3V/VCC-PF	I/O	767.31	SDC0_CMD
29	PF2_D2	D2	3.3V/VCC-PF	I/O	770.05	SDC0_CLK

6.14. LAYOUT recommendations

- SMHC signals in the core board in accordance with the single-ended 50Ω ± 10% impedance control, the impedance control of the base board is recommended to maintain the same;
- SMHC signals in the core board has been done equal length processing, core board alignment length see pin definition table;
- It is recommended that the bottom plate SMHC signal (excluding the insertion detection signal) alignment to do isometric control, error range ± 50mil, signal line spacing of at least 2W;
- Insertion detection signals in series with a 1K ohm resistor to improve ESD performance;
- The distance between the clock signal and other signals follow the 3W rule.

6.15. USB interface

ECK30-T13IC series core board supports 2 USB2.0 interfaces. USB0 supports HOST and Device modes, while USB1 only supports HOST mode.

If users use the OTG function of USB, the USB interface is recommended to use MICRO USB interface because it is a 5-wire interface with USB_ID (can be realized by multiplexing the GPIO function) signal, which can be used to identify HOST and DEVICE to realize the OTG function. If the user does not use the OTG function of USB, but only use it as USB HOST, then the 4-wire or 5-wire interface of USB interface can be selected.

Since the USB interface signal of T113 series processor does not provide a separate VBUS power supply, the USB interface signal belongs to the VIO power domain.

belongs to the VIO power domain. When the USB interface is used as DEVICE, the

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external HOST device should not be powered up first. If the external HOST device pow ers up first, a leakage may form on the USB OTG signals, which risks affecting the proc essor startup or damaging the interface functionality.

6.16. Pin Definitions

USB Interface Signal Pin Definition

Pin	network name	MPU	Level/Power Rails	Typology	Alignment length（mil）	Description
129	USB1_DP_A8	A8	3.3V/VCC-IO	I/O	662.06	
130	USB1_DM_B8	B8	3.3V/VCC-IO	I/O	665.84	
132	USB0_DP_B7	B7	3.3V/VCC-IO	I/O	747.38	
133	USB0_DM_C7	C7	3.3V/VCC-IO	I/O	750.80	

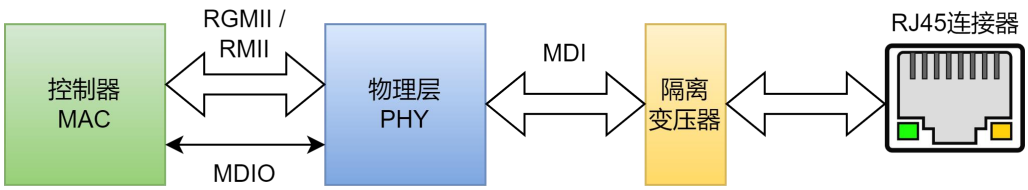
6.17. LAYOUT recommendations

- USB signal alignment do equal length control, differential pair internal error ±5mil, adj acent differential pair spacing 3W or more;
- The differential impedance of USB signal is controlled according to 90Ω;
- USB signal line as short as possible.

6.18. Ethernet Interface

ECK30-T13IC series core board supports 1 channel 10M/100M/1000M adaptive Ethern et controller. The Ethernet controller supports RGMII and RMII interfaces.ECK30-T13IC s eries core board MII interface multiplexing PE/PG pins, only support 3.3V level.

Usually an RJ45 Ethernet interface is mainly composed of Ethernet controller MAC (Media Access Control), Ethernet physical layer interface PHY (Physical Layer), Ethernet t ransformer, RJ45 connector several parts, as shown in the following figure.



RJ45 Ethernet Components

There is no Ethernet PHY circuit on ECK30-T13IC series core board, users need to

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design the PHY interface chip circuit on the backplane to use the Ethernet function. You can refer to the drawing of ECK30-T13IC series single board for the design of PHY inter face circuit.

6.19. Pin Definitions

Ethernet Interface Signal Pin Definitions

Pin	network name	MPU	Level/Power Rails	Typology	Alignment length（mil）	Description
36	PE4_T2	T2	3.3V/VCC-PE	I/O	870.30	RGMII_TXD0
37	PE5_T3	T3	3.3V/VCC-PE	I/O	837.22	RGMII_TXD1
43	PE11_N1	N1	3.3V/VCC-PE	I/O	858.70	RGMII_TXD2
34	PE12_R5	R5	3.3V/VCC-PE	I/O	847.87	RGMII_TXD3
38	PE6_R1	R1	3.3V/VCC-PE	I/O	838.60	RGMII_TXCTRL
51	PE3_U3	U3	3.3V/VCC-PE	I/O	873.56	RGMII_TXCK
49	PE1_U1	U1	3.3V/VCC-PE	I/O	875.94	RGMII_RXD0
50	PE2_U2	U2	3.3V/VCC-PE	I/O	838.40	RGMII_RXD1
35	PE13_R4	R4	3.3V/VCC-PE	I/O	854.81	RGMII_RXD2
44	PE14_N4	N4	3.3V/VCC-PE	I/O	851.84	RGMII_RXD3
48	PE0_V1	V1	3.3V/VCC-PE	I/O	857.64	RGMII_RXCTRL
45	PE15_N5	N5	3.3V/VCC-PE	I/O	838.51	RGMII_RXCK
40	PE8_R3	R3	3.3V/VCC-PE	I/O	841.12	MDC
41	PE9_P2	P2	3.3V/VCC-PE	I/O	841.70	MDIO

6.20. LAYOUT recommendations

- RGMII signal transmit and receive packets do equal length control, error ±25mil, line s pacing 2W or more;
- Network differential signals do equal length control, error ±10mil within the differential pair, adjacent differential pair spacing more than 3W;
- The network interface transformer is placed close to the PHY chip, and the distance is recommended to be no more than 20mm;
- The power pin decoupling capacitor of PHY chip is placed close to PHY chip;

6.21. CVBS interface

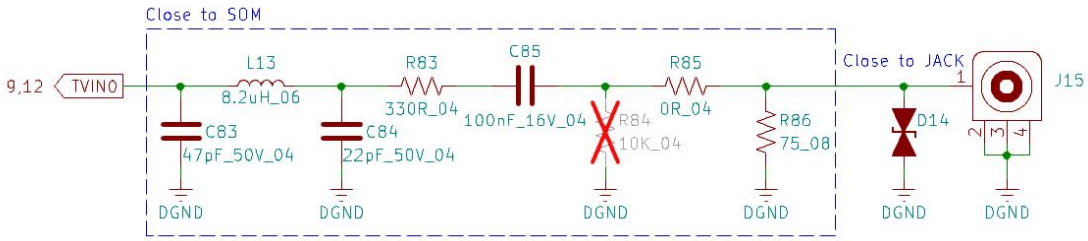
ECK30-T13IC core board provides 2 CVBS analog video inputs and 1 CVBS analog

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video output. Only a small amount of filtering, matching and protection circuits need to be placed on the bottom board to realize the analog video input and output interface func tions.

6.22. Reference Circuit



6.23. Pin Definitions

Analog Video Signal Pin Definitions

Pin	network name	MPU	Level/Power Rails	Typology	Alignment length (mil)	Description
117	TVOUT0_E19	E19	1.8V/VCC-TVOUT	AO		
118	TVIN1_C9	C9	1.8V/VCC-TVIN	AI		
119	TVIN0_B9	B9	1.8V/VCC-TVIN	AI		

6.24. LAYOUT recommendations

- Place the TVS close to the interface;
- Matching 75 ohm resistor has power requirement, 0805 or above size package is recom mended;
- The alignment impedance control is 37.5 ohms;
- Analog signal alignment, should be away from the interference, can be packaged groun d processing.

6.25. Analog Audio Interface

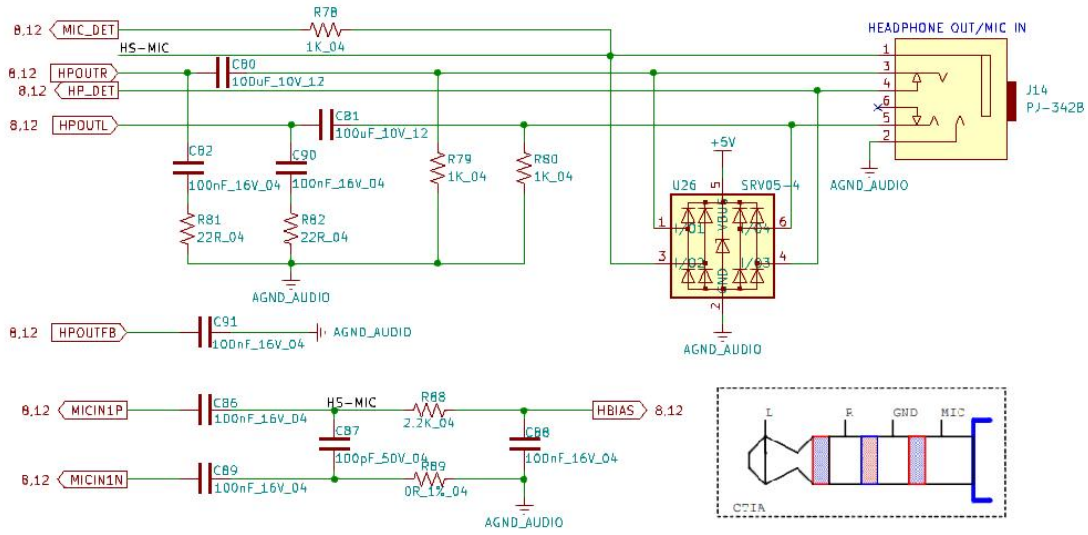
T113-i chip has an integrated audio codec function that provides analog audio interfac es. 2 analog audio outputs (LINEOUT, HPOUT) and 5 analog audio inputs (MICIN*3, F

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MIN, LINEIN) are available from the ECK30-T13IC core board.

6.26. Reference Circuit



Analog Audio Headset Interface Schematic

6.27. Pin Definitions

Analog Audio Signal Pin Definitions

Pin	network name	MPU	Level/Power Rails	Typology	Alignment length（mil）	Description
93	FMINR_C17	C17	1.8V/AVCC	AI		
94	FMINL_B17	B17	1.8V/AVCC	AI		
95	LINEINR_C16	C16	1.8V/AVCC	AI		
96	LINEINL_B16	B16	1.8V/AVCC	AI		
97	AUGND	-	AGND	PWR		Audio Analog Signal Ground
98	MBIAS_E16	E16	3.3V/VCC-IO	AO		Microphone Bias Voltage
99	MIC_DET_A17	A17	1.8V/AVCC	AI		Microphone insertion detection
100	MICIN1P_D20	D20	1.8V/AVCC	AI		
101	MICIN1N_D19	D19	1.8V/AVCC	AI		
102	MICIN2P_E15	E15	1.8V/AVCC	AI		
103	MICIN2N_D15	D15	1.8V/AVCC	AI		
104	MICIN3P_D17	D17	1.8V/AVCC	AI		
105	MICIN3N_D16	D16	1.8V/AVCC	AI		

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106	AUGND	-	AGND	PWR		Audio Analog Signal Ground
107	LINEOUTRP_B14	B14	1.8V/AVCC	AO		
108	LINEOUTRN_C14	C14	1.8V/AVCC	AO		
109	LINEOUTLP_B15	B15	1.8V/AVCC	AO		
110	LINEOUTLN_C15	C15	1.8V/AVCC	AO		
111	HBIAS_E17	E17	3.3V/VCC-IO	AO		Headphone Bias Voltage
112	HP_DET_A13	A13	1.8V/AVCC	AI		Headphone Insertion Detection
113	HPOUTR_D13	D13	1.8V/HPVCC	AO		
114	HPOUTFB_E13	E13	1.8V/HPVCC	AO		
115	HPOUTL_F13	F13	1.8V/HPVCC	AO		

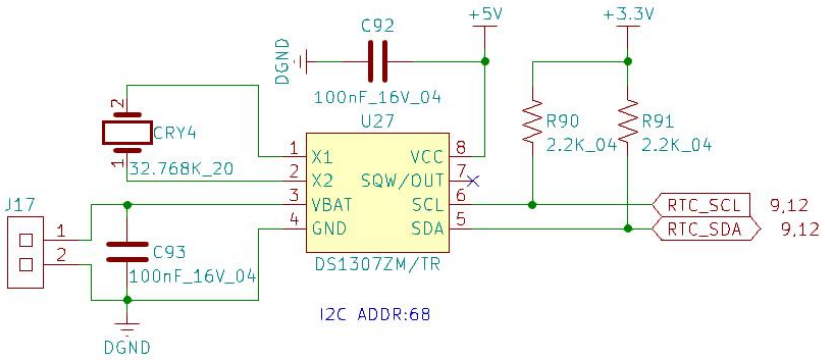
6.28. LAYOUT recommendations

- Place TVS close to the interface;
- Analog signal alignment, which should be kept away from interference, can be ground-wrapped.

6.29. RTC

ECK30-T13IC core board does not have an RTC that uses a backup battery power supply; if the user needs this RTC function, the function can be extended on the base board via the I2C bus.

6.30. Reference Circuit



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RTC Reference Circuit Diagram

6.31. Digital Audio Interface

ECK30-T13IC core board supports a maximum of 2 digital audio interfaces (PCM/I2S). In the circuit design of the base board, the digital audio interface signals need to be connected to the audio codec chip, through which the audio codec chip realizes the audio interface functions such as headphone, microphone and speaker.

6.32. UART Interface

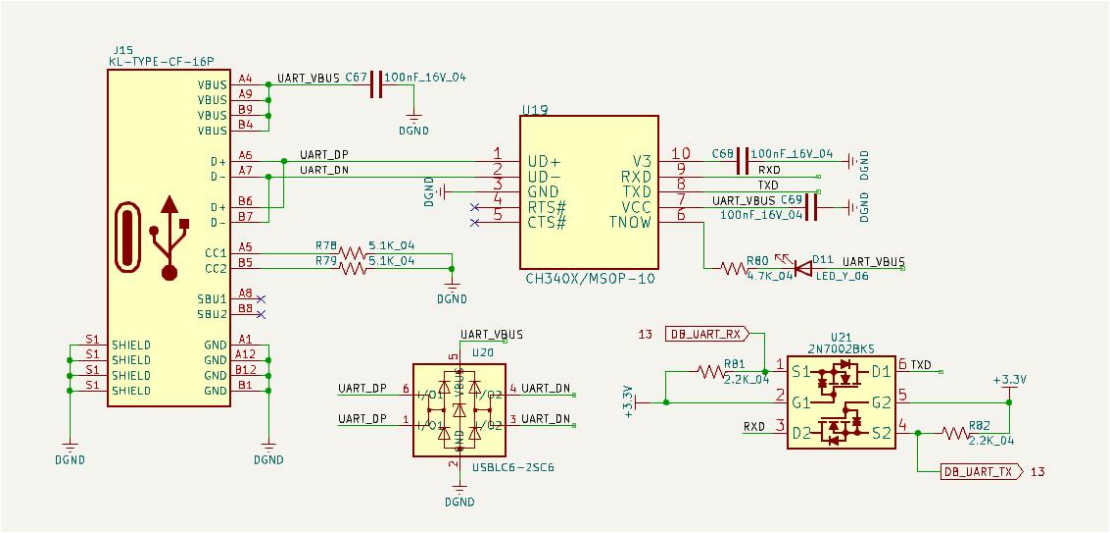
ECK30-T13IC core board supports a maximum of 6 asynchronous serial ports with a maximum baud rate of 4Mbps. By default, the core board uses UART 0 as the debugging serial port.

6.33. Reference Circuit

For the convenience of debugging, the backplane can be debugged through the USB to serial chip will debug the serial port lead out for the USB interface, USB to serial circuit schematic diagram can be referred to in the following figure. CH343X chip I/O to provide automatic anti-pair inverting function, add a 2N7002BKS dual NMOS tube constitute a preventive direction to the MCU inverting circuit, and at the same time pull-up resistor connected to the MCU output VDD_3V3_SOM or VDD_3V3_SOM control under the 3.3V power supply can effectively solve the serial port I/O level compatibility and power domain power-up timing problems. SOM or VDD_3V3_SOM control of the 3.3V power supply, you can effectively solve the serial port I/O level compatibility and power domain power-up timing issues.

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6.34. SPI Interface

ECK30-T13IC series core board leads to 1 SPI interface, which supports master/slave mode. the SPI signals include SPI_CLK, SPI_SS, SPI_MOSI, and SPI_MISO, and the design should confirm the relationship between the master and slave devices, and then confirm the direction of the MOSI and MISO signals. the 1 SPI only provides 1 chip select signal.

6.35. I2C Interface

ECK30-T13IC series core board supports 4-way I2C controller and 2 clock frequency modes, 100Kbit/s in standard mode and 400Kbit/s in fast mode.

Several devices can be mounted under the same I2C bus, and the following points need to be noted in the schematic design:

a) Check whether the addresses of the devices under the same bus are in conflict;

b) Ensure that there is a pair of pull-up resistors on each I2C bus, the resistance value is recommended to be 2.2K~10K, but do not add repeatedly;

c) I2C bus pull-up resistors are not provided in the core board, users need to pull them up when applying in the base board;

d) Check whether the I2C interface level of the device is 3.3V, if not, you need to add a level conversion circuit;

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e) Check whether the I2C interface power rails are consistent, the bus switching circu it needs to be considered when interconnecting I2C interfaces in different time domains;

f) Don't have too many devices under the same bus, otherwise it may exceed the 40 0pF load capacitance limit required by the I2C specification and affect the signal wavefor m.

6.36. CAN interface

ECK30-T13IC series core boards support 2-channel CAN controllers, support CAN 2. 0A and CAN 2.0B protocols, and only require external CAN transceivers for CAN comm unication.

6.37. ADC Interface

ECK30-T13IC series core boards provide three types of ADC interfaces, namely, one LRADC (Low Rate ADC), two GPADCs (General Purpose ADC), and four TPADCs (Tou ch Panel ADC).

LRADC:

- 6bit resolution, used for key voltage recognition, maximum sampling rate 2KHz, sampli ng voltage range: 0~1.266V;
- When LRADC is used for key recognition, it is recommended to use 1% precision resi stor if the key is used in voltage divider resistor mode;
- If LRADC is not used, the core board pins can be suspended, the board has provided 51K pull-up to AVCC.

GPADC:

- 12bit resolution, maximum sampling rate 1MHz, sampling voltage range: 0~1.8V;
- GPADC is not recommended to be applied to external surge or high voltage I/O interfa ce end voltage recognition to avoid causing damage to the chip interface.

TPADC:

- 4-channel TPADC interface, 12bit resolution, 8bit sampling accuracy, maximum samplin g rate 1MHz, can be used to connect 4-wire RTP screen or used as AD_KEY functio n.

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6.38. GPIO Interface

ECK30-T13IC series core boards can provide a maximum of 79 GPIO interfaces, but most of them have multiplexing functions. Users can flexibly configure GPIOs according to their needs.

6.39. Hardware design check items

- Power rails: Check the I/O interface application for inconsistent power rails, such as a 1.8V signal connected to a 3.3V signal. If there is a need to connect signals from different power rails, it should be handled by a level shifting circuit.
- Power-up timing: Check whether the signals connected to the bottom board and the core board are powered up first by the bottom board signals, or the power-up time of the signals of the two boards is very different.
- Pull-up and pull-down resistors: The multiplexed I/O interfaces have an uncertain output state before powering up the software configuration. If the signals need to maintain a certain level when powering up, pull-up and pull-down resistors should be designed on the bottom board. Some function signals also need to design pull-up or pull-down resistors on the backplane, such as I2C signals. Attention should be paid to the design of pull-up power rails when designing pull-up resistors.
- ESD protection: external interface signals should be considered for the corresponding ESD protection design, the choice of ESD program should take into account the signal rate, communication protocols and application environment requirements.
- High-speed signal isometric: High-speed signals should be considered PCB isometric design, including USB, Ethernet, SDIO, display and so on.
- Impedance control: High-speed signals should be considered PCB impedance control, the key to impedance control is to maintain the continuity of the impedance, the base plate should be designed with reference to the impedance of the core board signals.

7. Software resources

ECK30-T13IC series core boards are equipped with an operating system based on Linux 5.4.61 kernel. The boards are shipped with a cross-compilation toolchain required for e

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mbedded Linux system development, U-boot source code, Linux kernel and the source code of each driver module, as well as various development and debugging tools for Windows desktop environments and Linux desktop environments. Development and debugging tools for Windows desktop environment and Linux desktop environment.

Operating System:

Ubuntu 18.04 system

System source code:

u-boot 2018.07

Kernel 5.4.61

Buildroot 201902

Buildroot 202205

openwrt

Development environment and tools:

USB burning tool: PhoenixSuit

SD card burning tool: PhoenixCard

7.1. System resources

System Software Resource Sheet

Categories	Name	Description	Source code
SPL	spl-pub	Boot0, boot uboot	<SDK>/brandy/brandy-2.0/spl-pub/
BOOT	u-boot 2018.07	Boot Programs	<SDK>/brandy/brandy-2.0/u-boot-2018/
Kernel	Kernel 5.4.61	Linux kernel	<SDK>/kernel/linux-5.4/
Device Driver	Audio	Built-in audio driver	sound/soc/sunxi_v2/*
	AWlink	CAN driver	drivers/net/can/sunxi_awlink.c
	GMAC	Built-in MAC driver	drivers/net/ethernet/allwinner/sunxi-gmac.c
	GPADC	GPADC Driver	drivers/input/sensor/sunxi_gpadc.c
	GPIO	GPIO Driver	drivers/pinctrl/sunxi
	LCD	Disp2 Display Driver	drivers/video/fbdev/sunxi/disp2/disp/lcd/
	LRADC	Key Module Driver	drivers/input/keyboard/sunxi-keyboard.c

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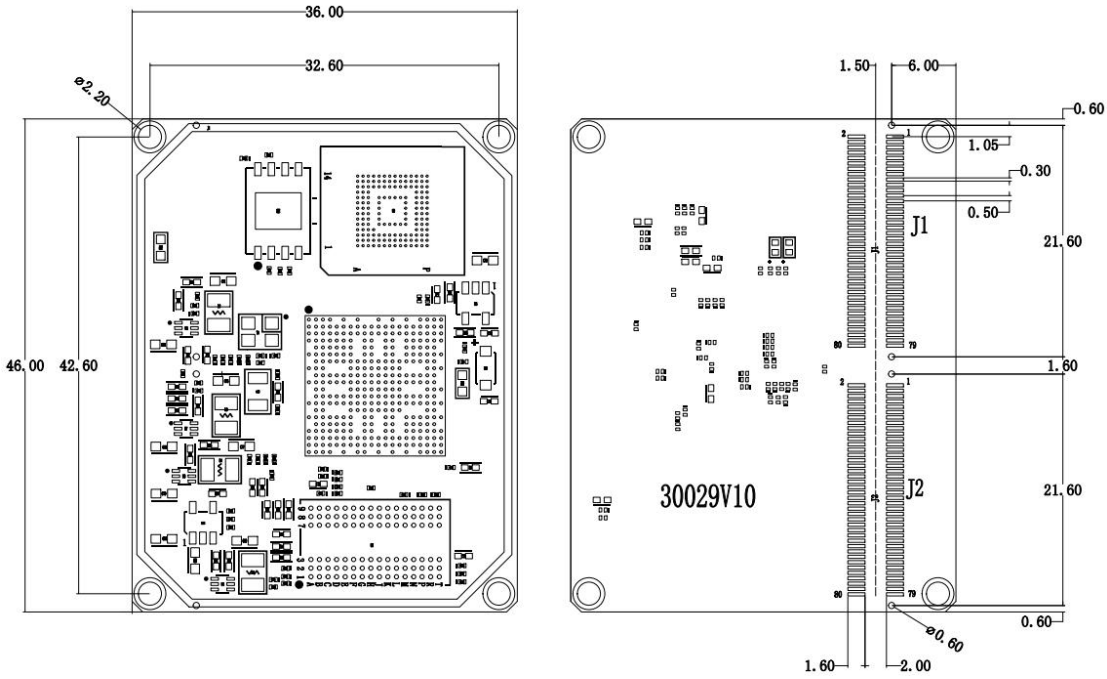
	SMHC	MMC Driver	drivers/mmc/host/sunxi-mmc.c
	SPI	SPI Driver	drivers/spi/spi-sunxi.c
	SPI-NAND	SPI-NAND Driver	drivers/mtd/awnand/spinand
	TVD	CVBS Input	drivers/media/platform/sunxi-tvd/
	TVE	CVBS Output	drivers/video/fbdev/sunxi/disp2/tv/
	TWI	I2C Driver	drivers/i2c/busses/i2c-sunxi.c
	UART	Serial Driver	drivers/tty/serial/sunxi-uart.c
	VIN	CSI Driver	drivers/media/platform/sunxi-vin/
Operating Systems	Buildroot 201902	Version 201902 Buildroot	<SDK>/buildroot/buildroot-201902
	Buildroot 202205	Buildroot version 2022 05	<SDK>/buildroot/buildroot-202205
	openwrt	openwrt	<SDK>openwrt/openwrt
Development Tools	PhoenixSuit	USB Burning Tool	/tools/PhoenixSuit
	PhoenixCard	SD Card Burning Tool	/tools/PhoenixCard

8. Structural dimensions

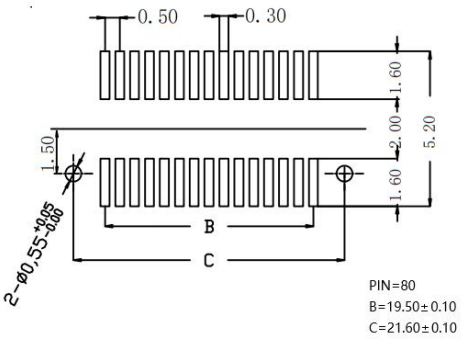
ECK30-T13IC series core board adopts 160 PIN, 0.5mm pitch BTB connector interface form, which is convenient for users to install and remove, and the core board comes with four 2.2mm mounting holes for fixing the core board. The core board structure dimensions are shown in the figure below.

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BTB Core Board Structure Dimension Drawing



BTB Connector Dimension Drawing

9. Reference documents

T113-i_V1.9.pdf

10. Revised notes

Revised Explanatory Notes

Version	Revisions	Revision time	Preparation	Proofreading	Approval
V1.0	first draft	25-04-21	WJ	LJQ	WFX

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