User Manual
ECK30-T13IA Core Board



Chengdu Ebyte Electronic Technology Co.,Ltd.

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1. Product Overview

1.1.Product Introduction

Ebyte ECK30-T13IA series core board is carefully designed based on Allwinner's T113-i processor. It is a low-cost, low-power, cost-effective, and highly reliable domestically produced industrial embedded core board with stamp hole connection. It can be widely used in industrial control, HMI, IoT and other fields.

Allwinner's T113-i processor is composed of three heterogeneous processors: dual-core ARM Cortex-A7 , RISC-V and HiFi4 DSP, which can provide users with efficient computing capabilities. It also provides rich digital I/O functions such as 1 display, 1 digital camera, 1 Gigabit Ethernet, 3 SDIO, 2 USB, 6 UART, 2 CAN, etc., and also provides rich analog I/O functions such as analog video, analog audio, ADC, etc.

The ECK30-T13IA series core board includes 3 specific product models, all of which are designed with domestically produced industrial-grade devices. They mainly differ in memory capacity, storage configuration, etc. Customers can choose the appropriate model according to their needs. For product selection, please refer to the product selection section.

The physical picture of the ECK30-T13IA series core board (without components on the bottom of the product) is as follows:



Physical picture

1.2.Features

1、Processor: Allwinner T113-i Processor:

- Dual-core ARM Cortex-A7, up to 1.2GHz;
- RISC-V;

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- HiFi4 DSP ;

2、On-board DDR3 SDRAM, 256MB/512MB/1GB capacity optional;

3、On-board storage: 8GB eMMC or 256MB SPI NAND FLASH optional;

4、Video Output:

- 2-channel LVDS output, supporting 1920×1080@60fps;
- 1 digital RGB output, supporting 1920×1080@60fps;
- 1 MIPI DSI, supports 4Lane, supports 1920×1200@60fps;
- 1 CVBS output, supporting NTSC and PAL formats;
- 1 serial RGB (DBI) output, supporting 240×32060fps;

Note: LVDS0, LVDS1 and digital RGB pins are multiplexed, LVDS0 and MIPI DSI pins are mu ltiplexed, and DBI and SPI1 pins are multiplexed;

5、Video Input:

- 1 CSI, 8-bit parallel interface, supports 1920×1080@30fps;
- 2-way CVBS input, supporting NTSC and PAL formats;

6、Audio Interface:

- Integrated Audio Codec;
- 3-way mono MIC input;
- 1 dual-channel LINE IN;
- 1 dual-channel FM IN;
- 1 differential LINE OUT;
- 1-channel dual-channel Headphone output;

7、Network: integrated with 1 10/100/1000 adaptive Ethernet MAC, supporting RMII/RGMII interface;

8、USB: 1 USB2.0 DRD, 1 USB2.0 HOST;

9、SMHC: Integrates 3 SMHC controllers, and leads 2 routes to stamp holes;

10、4-channel TWI, compatible with I2C bus standard, supporting standard mode (100Kbps) and high -speed mode (400Kbps);

11、2-way SPI, 1 way is led out to the stamp hole ;

12、6-channel UART, maximum baud rate 4Mbps;

13、8-channel PWM, maximum output frequency 24/100MHz, support PWM output and input captur e;

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14、2-channel GPADC, 12-bit resolution, maximum sampling rate 1MHz;

15、4-channel TPADC, 12-bit resolution, maximum sampling rate 1MHz, support 4-wire resistive touch screen;

16、1 LRADC, 6-bit resolution, maximum sampling rate 2KHz;

17、1 LEDC, supports 1024 LEDs in series, with a maximum data transmission rate of 800Kbps;

18、3-channel I2S/PCM, support full-duplex, sampling rate 8KHz~48KHz;

19、1-way DMIC, supports up to 8 channels, sampling rate 8KHz~48KHz;

20、1-channel OWA, compatible with S/PDIF protocol;

21、2 CIRs, 1x CIR TX interface, 1x CIR RX interface;

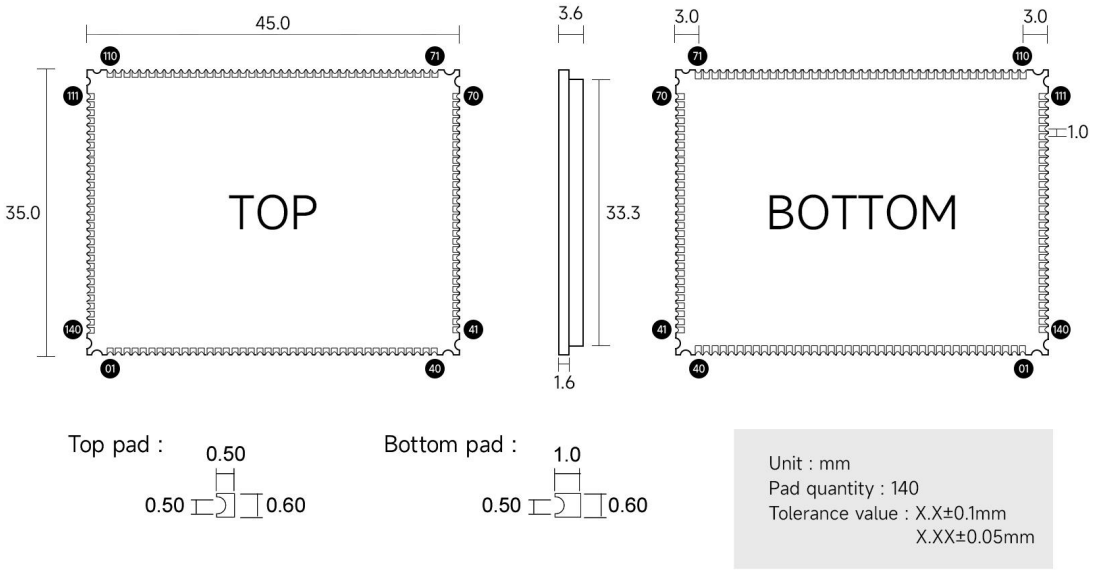
22、2-way CAN (CAN0, CAN1), supporting CAN 2.0A and CAN 2.0B protocols;

23、3-way JTAG, including ARM, RISC-V and HiFi4 DSP JTAG;

24、Interface form: 140-pin stamp hole, spacing 1.0mm;

25、Power supply: single-channel DC +5V±10%@0.5A power input;

26、Size: 45×35×3.6mm, as shown in the figure below:



Dimensions

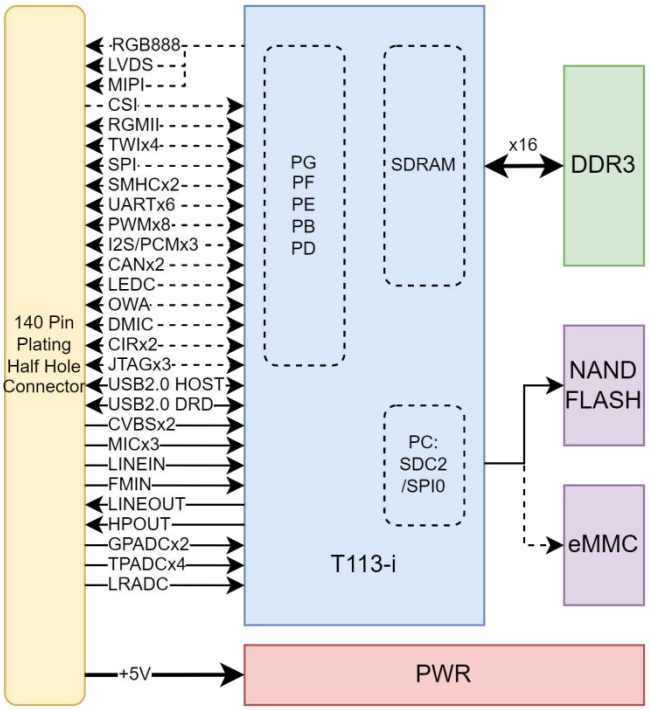
27、Working temperature: Industrial grade: -40℃-85℃;

28、PCB technology: 8-layer board design, immersion gold, lead-free technology;

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1.3.Core board functional block diagram



Functional Block Diagram

1.4.Typical Applications

- Smart home;
- Smart toys;
- Smart cities;
- Tablet computer ;
- IoT Gateway ;
- Advertising all-in-one machine ;
- Industrial all-in-one machine ;
- Industrial control motherboard;
- Robots and drones.

2. Product Selection

2.1.Model configuration

The ECK30-T13IA series core board selection and configuration table is as follows:

Product Selection and Configuration Table

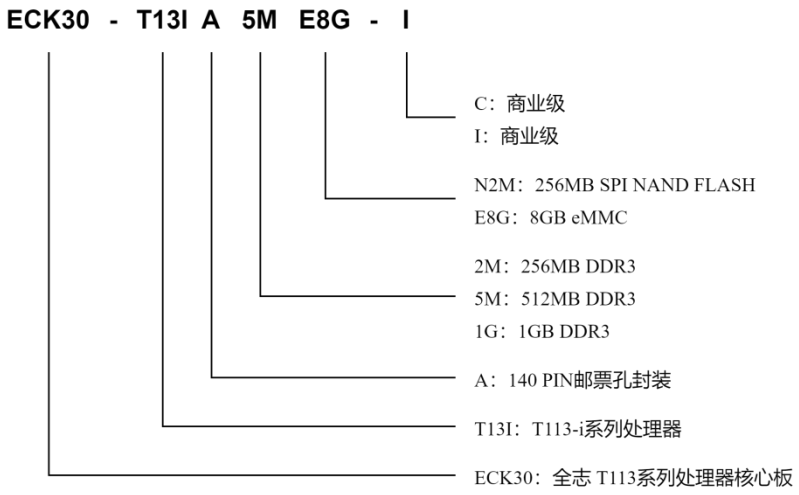
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Serial number	Product Model	Processor model	Memory	storage	Operating temperature
1	ECK30-T13IA2MN2M-I	T113-i	256MB DDR3	256MB NAND	Domestic industrial grade -40℃ ~ 85℃
2	ECK30-T13IA5ME8G-I	T113-i	512MB DDR3	8GB eMMC	Domestic industrial grade -40℃ ~ 85℃
3	ECK30-T13IA1GE8G-I	T113-i	1GB DDR3	8GB eMMC	Domestic industrial grade -40℃ ~ 85℃

2.2.Model code

The product model coding is shown in the figure below:



Model code description

3. Quick Experience

Choosing Ebyte single-board computer products, you can quickly experience the typical application fu nctions, baseboard design, software development, etc. of the ECK30-T13IA core board products.

4. Features and parameters

4.1.Product Features

The ECK30-T13IA series core board mainly integrates the processor, memory, storage and power syst em, and leads out all the I/O pins on the processor. Users can design the baseboard to apply the I/O res ources on the core board according to their needs and reuse the I/O into the functions they need.

The following table lists the main function parameters of the ECK30-T13IA series core board integrat ed on the board, and the function parameters of the reusable I/O resources. The description of each I/O f

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unction is the maximum indicator that the core board can use the I/O function without using other I/O fu nctions (for example, after using the 24-bit color RGB interface function and the network interface functio n, all UART functions cannot be realized).

Product Features

Function	quantity	Functional Description
CPU	1	T113-i; Dual-core ARM Cortex-A7@1.2GHz; RISC-V CPU; HiFi4 DSP;
MEM	1	On-board DDR3 SDRAM, 16-bit width, 256MB/512MB/1GB optional;
FLASH	1	On-board 8GB eMMC / on-board 256MB SPI NAND FLASH optional;
DISPLAY	1	Parallel RGB 24-bit color output, up to 1920× 1080@60fps ; Dual-channel LVDS output , supporting up to 1920× 1080@60fps ; 4-lane MIPI DSI, supports up to 1920× 1 200 @60fps ; Note: The I/Os of the above display interfaces are multiplexed and cannot be used at the same time; Serial RGB output, up to 800×480 @60fps ;
CSI	1	8- bit parallel digital camera interface , supports 1080P@30fps, maximum 148.5MHz pixel clock ;
CVBS IN	2	1 CVBS decoder, supporting NTSC and PAL formats , 10-bit video ADC;
CVBS OUT	1	Support NTSC and PAL formats , 10-bit video DAC;
Audio Codec	1	2- channel DAC , sampling rate 8KHz~192KHz ; 3- channel ADC , sampling rate 8KHz~48KHz ; 3 MIC IN , 1 LINE IN , 1 FM IN ; 1 differential LINE OUT , 1 headphone OUT ;
E- MAC	1	Support RMII/RGMII interface (10/100/1000Mbps) ;
SMHC	2	Support SD3.0 , SDIO3.0 , MMC5.0 protocols; SDC0 : 4- bit data bus (recommended as baseboard Micro SD function); SDC1 : 4 -bit data bus; Note: SDC2 is not brought out to the stamp hole, and is used to connect the eMMC or FLASH storage chip on the board;
USB DRD	1	Comply with USB2.0 standard, support USB HOST and USB Device functions;
USB HOST	1	Comply with USB2.0 standard and support USB HOS function;
TWI(I2C)	4	Support standard mode (100Kbps) and high-speed mode (400Kbps) ;
SPI	1	Support SPI mode and DBI (Display Bus Interface) mode; Support Master Mode , Slave Mode , 1 chip select signal; Supports up to 100MHz operating frequency;
UART	6	Maximum baud rate of 4Mbps (64MHz APB clock) , support hardware or software flow control;
PWM	8	0~100% adjustable duty cycle, supports output and input capture , output frequency is 0~24MHz or 100MHz ;
GPADC	2	12 -bit SAR type A/D converter, sampling frequency up to 1MHz ;
TPADC	4	12 -bit SAR A/D converter , sampling frequency up to 1MHz , supports 4- wire resistive touch screen;
LRADC	1	6- bit A/D converter, sampling frequency up to 2KHz , supports hold key and general key;
LEDC	1	Supports 1024 LED serial connections, LED data transmission rate up to 800Kbps ;

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PCM/I2S	3	Support full duplex, sampling rate 8KHz~384KHz ;
DMIC	1	Supports up to 8 channels, sampling rate 8KHz~48KHz ;
OWA	1	One Wire Audio , compatible with S/PDIF protocol;
CIR	2	Contains CIR TX and CIR RX , which can be remotely controlled via infrared;
CAN	2	Support CAN 2.0A and CAN 2.0B protocols;
JTAG	3	Includes ARM , RISC-V and HiFi4 DSP JTAG ;
GPIO	79	Software configures GPIO function and supports interrupt input;

4.2.Environmental characteristics

Environmental characteristics table

Operating temperature	Commercial Grade	0℃ ~ 70℃;
	Industrial Grade	-40℃ ~ 85℃;
Storage temperature	-40℃ ~ 85℃;	
Operating humidity	5~95% humidity, non-condensing;	
Storage humidity	60℃@95% humidity, non-condensing;	

4.3.I/O Features

4.3.1. I/O Pin Definition



Pin numbering diagram

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Pin Definition Table

Pin	Pin Name	MPU Pin	Level/Rail	Type	Length (mil)	Comment
1	REFCLK_OUT_J2	J2	1.8V	AO		
2	FEL_A18	A18	3.3V	DI		1KΩ in series
3	NMI_N3	N3	1.8V	I/O		
4	RESET_M2	M2	3.3V	I/O		10KΩ pull up
5	DGND	-	GND	PWR		
6	PG17_E7	E7	3.3V	I/O	1075.42	
7	PG18_D7	D7	3.3V	I/O	1007.06	
8	PG13_D6	D6	3.3V	I/O	891.26	
9	PG9_B6	B6	3.3V	I/O	914.82	
10	PG8_A6	A6	3.3V	I/O	919.43	
11	PG2_A3	A3	3.3V	I/O	902.69	
12	PG1_B3	B3	3.3V	I/O	907.56	
13	PG0_B2	B2	3.3V	I/O	916.6	
14	PG10_C6	C6	3.3V	I/O	904.65	
15	PG12_D5	D5	3.3V	I/O	895.1	
16	PG7_C5	C5	3.3V	I/O	902.43	
17	PG6_B5	B5	3.3V	I/O	904.28	
18	PG5_B4	B4	3.3V	I/O	901.95	
19	PG4_A4	A4	3.3V	I/O	901.03	
20	PG3_C3	C3	3.3V	I/O	898.23	
twenty one	PG16_F7	F7	3.3V	I/O	899.31	
twenty two	PG11_D4	D4	3.3V	I/O	782.01	
twenty three	PG14_E6	E6	3.3V	I/O	753.47	
twenty four	PG15_F6	F6	3.3V	I/O	752.68	
25	DGND	-	GND	PWR		
26	PF6_D3	D3	3.3V	I/O	1126.85	
27	PF0_C2	C2	3.3V	I/O	1122.36	
28	PF1_C1	C1	3.3V	I/O	1129.58	
29	PF2_D2	D2	3.3V	I/O	1129.74	33Ω in series
30	PF5_E2	E2	3.3V	I/O	1131.95	
31	PF3_D1	D1	3.3V	I/O	1130.76	
32	PF4_E3	E3	3.3V	I/O	1124.16	
33	DGND	-	GND	PWR		
34	PE12_R5	R5	3.3V	I/O	1117.23	
35	PE13_R4	R4	3.3V	I/O	1011.36	
36	PE4_T2	T2	3.3V	I/O	1010.35	
37	PE5_T3	T3	3.3V	I/O	1012.91	
38	PE6_R1	R1	3.3V	I/O	1010.38	
39	PE7_R2	R2	3.3V	I/O	1011.52	

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40	PE8_R3	R3	3.3V	I/O	1010.62	
41	PE9_P2	P2	3.3V	I/O	1009.88	
42	PE10_P3	P3	3.3V	I/O	1007.44	
43	PE11_N1	N1	3.3V	I/O	1011.75	
44	PE14_N4	N4	3.3V	I/O	1009.9	
45	PE15_N5	N5	3.3V	I/O	1012.78	
46	PE16_N6	N6	3.3V	I/O	971.43	
47	PE17_M6	M6	3.3V	I/O	1002.44	
48	PE0_V1	V1	3.3V	I/O	1012.2	
49	PE1_U1	U1	3.3V	I/O	1012.06	
50	PE2_U2	U2	3.3V	I/O	1011.86	
51	PE3_U3	U3	3.3V	I/O	1010.43	
52	DGND	-	GND	PWR		
53	PB8_G15	G15	3.3V	I/O	1535.4	
54	PB9_G16	G16	3.3V	I/O	1593.27	
55	PB10_F17	F17	3.3V	I/O	1592.89	
56	PB11_F15	F15	3.3V	I/O	1593.85	
57	PB12_F16	F16	3.3V	I/O	1511.52	
58	PB2_M16	M16	3.3V	I/O	1126.85	
59	PB3_M15	M15	3.3V	I/O	1082.91	
60	PB4_K16	K16	3.3V	I/O	1097.01	
61	PB5_K15	K15	3.3V	I/O	1125.02	
62	PB6_K17	K17	3.3V	I/O	1113.72	
63	PB7_J15	J15	3.3V	I/O	1038.85	
64	PB0_J16	J16	3.3V	I/O	1038.54	
65	PB1_J17	J17	3.3V	I/O	1032.1	
66	DGND	-	GND	PWR		
67	PD0_W19	W19	3.3V	I/O	1017.36	
68	PD1_V20	V20	3.3V	I/O	1016.69	
69	PD2_V19	V19	3.3V	I/O	1016.5	
70	PD3_U20	U20	3.3V	I/O	1016.65	
71	DGND	-	GND	PWR		
72	PD4_U19	U19	3.3V	I/O	1034.18	
73	PD5_U18	U18	3.3V	I/O	1037.15	
74	PD6_T19	T19	3.3V	I/O	1031.65	
75	PD7_T18	T18	3.3V	I/O	1031.69	
76	PD8_R20	R20	3.3V	I/O	1017.22	
77	PD9_R19	R19	3.3V	I/O	1019.47	
78	DGND	-	GND	PWR		
79	PD10_T17	T17	3.3V	I/O	1018.78	
80	PD11_R17	R17	3.3V	I/O	1018.77	
81	PD12_P19	P19	3.3V	I/O	1017.67	
82	PD13_P18	P18	3.3V	I/O	1018.78	

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83	PD14_N17	N17	3.3V	I/O	1016.2	
84	PD15_N16	N16	3.3V	I/O	1019.47	
85	DGND	-	GND	PWR		
86	PD16_N20	N20	3.3V	I/O	1031.7	
87	PD17_N19	N19	3.3V	I/O	1034.48	
88	PD18_M19	M19	3.3V	I/O	1032.43	
89	PD19_M18	M18	3.3V	I/O	1034.74	
90	PD21_V18	V18	3.3V	I/O	1095.57	
91	PD20_W18	W18	3.3V	I/O	1126.38	
92	DGND	-	GND	PWR		
93	FMINR_C17	C17	-	AI		
94	FMINL_B17	B17	-	AI		
95	LINEINR_C16	C16	-	AI		
96	LINEINL_B16	B16	-	AI		
97	AUGND	-	AGND	PWR		
98	MBIAS_E16	E16	-	AO		
99	MIC_DET_A17	A17	-	AI		
100	MICIN1P_D20	D20	-	AI		
101	MICIN1N_D19	D19	-	AI		
102	MICIN2P_E15	E15	-	AI		
103	MICIN2N_D15	D15	-	AI		
104	MICIN3P_D17	D17	-	AI		
105	MICIN3N_D16	D16	-	AI		
106	AUGND	-	AGND	PWR		
107	LINEOUTRP_B14	B14	-	AO		
108	LINEOUTRN_C14	C14	-	AO		
109	LINEOUTLP_B15	B15	-	AO		
110	LINEOUTLN_C15	C15	-	AO		
111	HBIAS_E17	E17	-	AO		
112	HP_DET_A13	A13	-	AI		
113	HPOUTR_D13	D13	-	AO		
114	HPOUTFB_E13	E13	-	AO		
115	HPOUTL_F13	F13	-	AO		
116	DGND	-	GND	PWR		
117	TVOUT0_E19	E19	-	AO		
118	TVIN1_C9	C9	-	AI		
119	TVIN0_B9	B9	-	AI		
120	DGND	-	GND	PWR		
121	LRADC_B12	B12	-	AI		51KΩ pull up
122	GPADC0_C13	C13	-	AI		
123	GPADC1_B13	B13	-	AI		
124	TP_X1_C12	C12	-	AI		1nF pull down
125	TP_X2_A11	A11	-	AI		1nF pull down

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126	TP_Y1_B11	B11	-	AI		1nF pull down
127	TP_Y2_C11	C11	-	AI		1nF pull down
128	DGND	-	GND	PWR		
129	USB1_DP_A8	A8	-	I/O	960.34	
130	USB1_DM_B8	B8	-	I/O	962.55	
131	DGND	-	GND	PWR		
132	USB0_DP_B7	B7	-	I/O	957.89	
133	USB0_DM_C7	C7	-	I/O	959.18	
134	DGND	-	GND	PWR		
135	VDD_3V3_SOM	-	3.3V	PWR		
136	VDD_1V8_SOM	-	1.8V	PWR		
137	DGND	-	GND	PWR		
138	DGND	-	GND	PWR		
139	VDD_5V_SOM	-	5V	PWR		
140	VDD_5V_SOM	-	5V	PWR		

Note:

- AI: analog input;
- AO: analog output;
- DI: digital input;
- DO: digital output;
- I/O: digital input and output;
- PWR: power supply;
- The unit of trace length is mil;
- For detailed stamp hole pin multiplexing functions, please refer to the "ECK30-T13IA Pin List" file.

4.3.2. I/O Impedance Control

All high-speed signals of the ECK30-T13IA series core board have impedance control and length control during PCB design. The impedance control parameters of the core board traces are shown in the table below.

Trace impedance control table

Serial number	Impedance Controlled Routing Classification	Impedance Control	Typical Model Network Name
1	USB differential signaling	90±10%Ω	USB1_DP_A8 / USB1_DM_B8
2	LVDS, MIPI differential signal	100±10%Ω	PD0_W19/PD1_V20
3	Analog video input and output signals	37.5±10%Ω	TVOUT0_E19 , TVIN1_C9 , TVIN0_B9

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4	General single-ended routing	50±10%Ω	

4.4.Electrical characteristics

4.4.1. Power consumption

Note: The following parameters are measured on the ECK30-T13IA5ME8G-I core board at room temperature. The measured power consumption does not include the baseboard power consumption. When measuring the heavy-load power consumption, the memory and eMMC test programs are run, without display, baseboard SDIO access, and network access. Factors such as test methods, usage functions, and ambient temperature will affect power consumption. The following power consumption data is for reference only.

Power Consumption Table

Power Status	Test environment	Supply voltage	Current	Power consumption
BOOT	UBOOT is running	5.0V	0.169A	0.845W
PWRUP	Entering the system without running the application	5.0V	0.104A	0.52W
PWRUP	Software reload testing	5.0V	0.203 A	1.015W
SLEEP	Freeze mode hibernation	5.0V	0.0 87 A	0.435W
SLEEP	mem mode sleep state	5.0V	0.0 56 A	0.28W

5. Core board hardware design

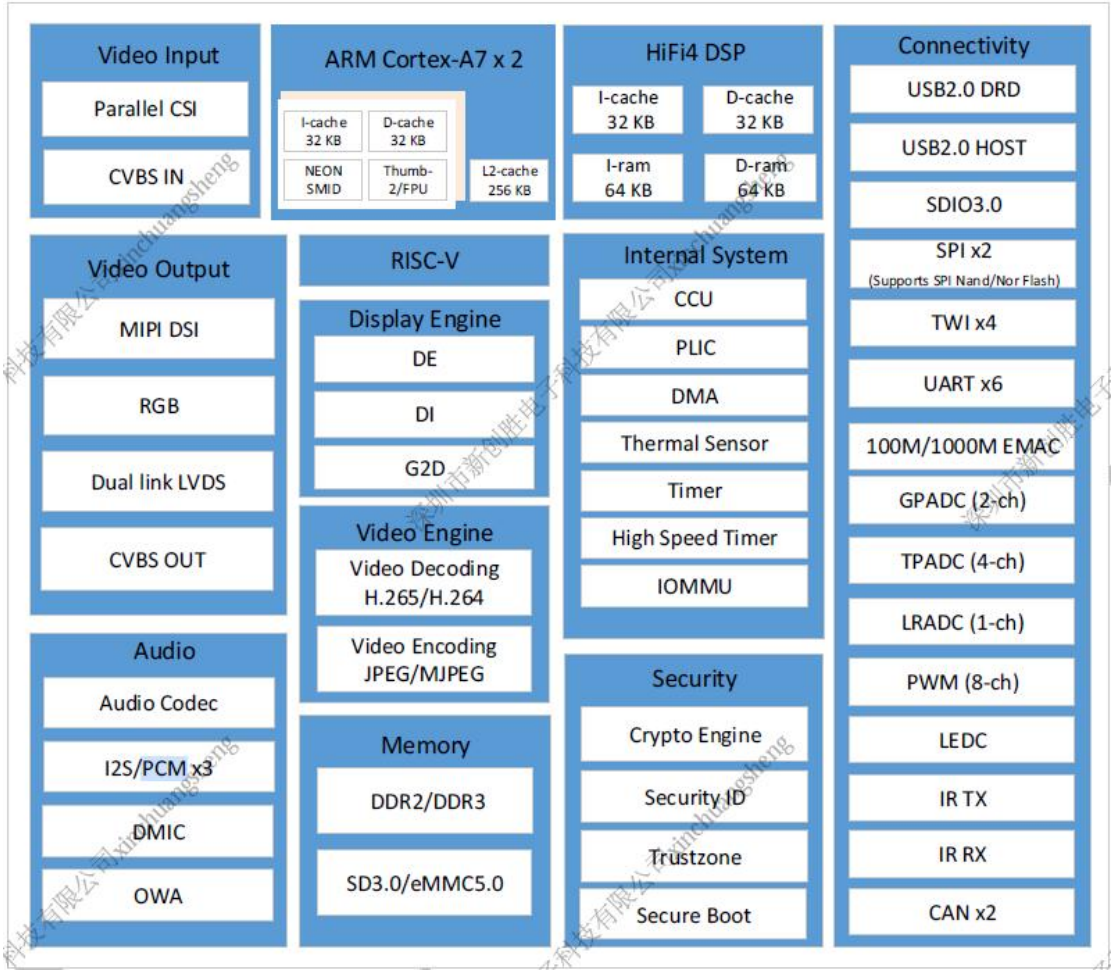
5.1.processor

the T113-i processor in the T113 series of Allwinner Technology as the core. The T113-i processor is an advanced application processor designed for the RISC-V multimedia decoding platform. It integrates three heterogeneous processors: RISC-V, dual-core ARM Cortex - A7 and HiFi4 DSP, which can provide efficient computing power. T113-i supports full-format decoding such as H.265, H.264, MPEG-1/2/4, JPEG, VC1, etc. The independent encoder can encode JPEG or MJPEG. The integrated ADC/DAC and I2S/PCM/DMIC/OWA audio interfaces can work seamlessly with the CPU to accelerate multimedia algorithm applications and improve user experience. T113-i supports multiple display output interfaces of RGB/LVDS/MIPI DSI/CVBS OUT to meet the needs of connecting to different screens and monitors. T113-i has a rich set of expansion interfaces, such as CAN, USB, SDIO, EMAC, TWI, UART, SPI, PWM, GPADC, LRADC, TPADC, IR TX&RX, etc. In addition, T113-i can be connected to other different peripheral devices such as WiFi and Bluetooth through SDIO and UART. The functional block diagram of T113-i processor is s

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hown in the figure below.



T113-i system functional block diagram

5.1.1. Processor Architecture

The T113-i processor adopts a multi-core heterogeneous design, integrating three heterogeneous proces sors: RISC-V, dual-core ARM Cortex - A7 and HiFi4 DSP. See the table below for related parameters.

T113-i processor architecture parameter table

Function	Function parameters
ARM	Dual-core ARM CortexTM-A7, 1.2GHz; 32 KB I-cache + 32 KB D-cache + NEON SIMD + Thumb 2/FPU + 256 KB L2 cache;
RISC-V	RISC-V CPU, 1008MHz; 32 KB I - cache + 32 KB D - cache ;
DSP	HiFi4 DSP, 600MHz; 32 KB L1 I - cache and 32 KB L1 D - cache ; 64 KB I - ram and 64 KB D - ram ;

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5.2.Memory

The ECK30-T13IA series core board has a DDR3 SDRAM memory chip mounted on the board. It is designed with a 16-bit memory data width and has three optional capacities: 256MB/512MB/1GB. The designed memory uses domestic industrial-grade devices. The memory chip model is shown in Table below.

Memory Chip Selection Table

factory	model	Single chip capacity	Operating temperature
Longsys	F60C1A0002-M69W	2Gbit	-40℃ ~ 95 ℃
GigaDevice	GDP1BFLA-WB	2Gbit	-40℃ ~ 95 ℃
Longsys	F60C1A0004-M79W	4Gbit	-40℃ ~ 95 ℃
GigaDevice	GDP2BFLM-WB	4Gbit	-40℃ ~ 95 ℃
GigaDevice	GDP3BELM-WB	8Gbit	-40℃ ~ 95 ℃

Note: The specific model of the mounted memory chip shall be subject to the actual product.

5.3.clock

ECK30-T13IA series core board provides one 32.768KHz crystal (passive) oscillator circuit and one 24MHz crystal (passive) oscillator circuit on the board as the processor system clock source.

5.4.storage

The ECK30-T13IA series core board has two storage solutions designed on the board. One is the SPI FLASH storage solution. This storage solution uses SLC NAND FLASH chips as storage media, which has the characteristics of low cost and high reliability. The other is the eMMC storage solution. This storage solution uses eMMC chips as storage media, which has the characteristics of large storage capacity, low unit storage cost and easy use. Because the two storage solutions reuse the same I/O resources, a core board product of one model only supports one storage solution. Users need to select the corresponding model of core board products according to the storage requirements of specific projects.

The SPI NAND FLASH is connected to the processor via the SPI0 bus. The device uses GigaDevice's GD5F2GM7UEYIGR (256MB) industrial-grade SPI NAND FLASH.

The eMMC memory is connected to the processor via the SMHC (SDC2) bus. The device uses domestic industrial-grade eMMC memory chips, and the chip models are shown in the table below.

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eMMC chip selection table

factory	model	capacity	Operating temperature
Longsys	FEMDRW008G-88A39	8GB	-40℃ ~ 85 ℃
YEESTOR	SGM8000I-S27B8G	8GB	-40℃ ~ 85 ℃

Note: The specific model of the mounted memory chip shall be subject to the actual product.

5.5.led

LEDs are mounted on the core board , which can be used to indicate the status and operation of the board without a shield cover . Both LEDs are programmable indicator LEDs , corresponding to the two pins F2/PC0 and F1/PC1 respectively, and light up when the high level is on.

5.6.power supply

ECK30-T13IA series core board adopts a separate power supply solution and is designed in strict acc ordance with the voltage, power and timing requirements in the T113-i manual. The ECK30-T13IA series core board is powered by a single DC +5V power supply. Only one VDD_5V_SOM power input is requi red externally. Other power supplies are generated internally by the core board, and no additional power s upply is required.

The ECK30-T13IA series core board also provides two power outputs, namely VDD_3V3_SOM and VDD_1V8_SOM, which can be used to power low-power devices on the baseboard and control the power -on timing of the baseboard I/O interface. The relevant parameters of the two output power supplies are s hown in the table below.

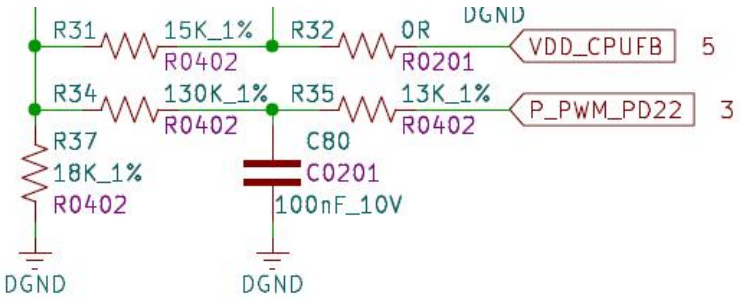
Output power parameter table

Power network name	Power supply type	Power Domain	Typical voltage	Maximum current
VDD_3V3_SOM	BUCK	VIO	3.3V	500mA
VDD_1V8_SOM	LDO	VIO	1.8V	100mA

the ECK30-T13IA series core board supports DVFS dynamic frequency and voltage regulation. The h ardware design uses the PWM function of the processor PD22 pin as the control pin for DVFS dynamic frequency and voltage regulation. The software should pay attention to the configuration of the PD22 pin and the DVFS function when configuring the I/O hardware and functions. The relevant hardware schemati c diagram is as follows.

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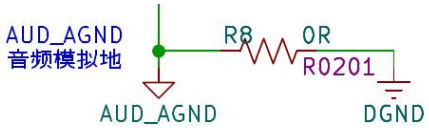
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DVFS functional hardware schematic diagram

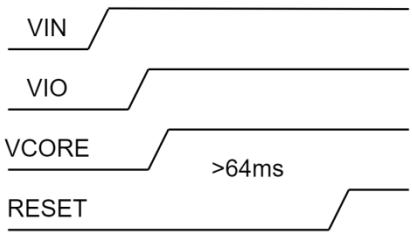
The ECK30-T13IA series core board does not have a backup battery-powered RTC function, so the c ore board does not have an RTC power interface. If a backup battery-powered RTC function is required, the RTC chip can be expanded on the baseboard through the I2C bus.

The ECK30-T13IA series core board provides two power ground pins, namely the digital signal groun d DGND and the audio analog signal ground AUGND. The power ground and digital signal are reference d to DGND, and the audio analog signal is referenced to AUGND. The two grounds are connected at a single point on the core board, and the principle is shown in the figure below.



AUGND single point grounding schematic diagram

the ECK30-T13IA series core board are very simple. The main power domains are only VIN, VIO a nd VCORE. Among them, VCORE is only related to the processor and has nothing to do with the user I /O interface. It can be ignored when applying. The power-on sequence of the ECK30-T13IA series core b oard is shown in the figure below.



Core board power-on timing diagram

All external I/O interfaces of the ECK30-T13IA series core board belong to the VIO power domain. The baseboard can use the VDD_3V3_SOM or VDD_1V8_SOM power output by the core board as the c ontrol signal of the baseboard I/O interface power domain.

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5.7.On-board I/O assignment

ECK30-T13IA series core board occupy the I/O functions of the T113-i processor. These I/O functions are not brought out to the stamp holes. Users should pay attention to the function configuration of these I/Os when configuring the software. The specific occupied I/Os are shown in the following table.

Core board multiplexing I/O allocation table

MPU I/O Pins	Network Name	Core board function description
Y18	P_PWM_PD22	DVFS PWM
F2	LED1	On-board user LED1
F1	LED 2	On-board user LED2
G3	PC2_eCLK_SCLK	eMMC CLK / SPI0 CLK
G2	PC3_eCMD_SCS	eMMC CMD / SPI0 CS
H3	PC4_eD2_SMOSI	eMMC DATA2 / SPI0 MOSI
F5	PC5_eD1_SMISO	eMMC DATA1 / SPI0 MISO
G6	PC6_eD0_SWP	eMMC DATA0 / SPI0 WP
G5	PC7_eD3_SHOLD	eMMC DATA3 / SPI0 HOLD

6. Baseboard hardware design

6.1.Power interface

For embedded product design, the design of the power system is crucial . It not only needs to consider the basic electrical parameters of the power supply itself, but also the stability design , timing design and other factors of the power supply. The ECK30-T13IA series core board adopts a single power supply solution and provides power timing management signals to simplify the user's baseboard power design as much as possible.

6.1.1. Power Input

The ECK30-T13IA series core board is powered by a single DC +5V power supply, corresponding to pins 139 and 140 of the stamp hole connector. The power supply pin is named VDD_5V_SOM. The power supply voltage range is 5.0V±10%. The normal power consumption of the ECK30-T13IA series core board is about 1W. When designing the power supply for the core board, the baseboard should consider the I/O output power consumption and the increased power consumption when more functions are running at the same time, and the increased power consumption of components at high temperature. Therefore, it

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is recommended that the core board power supply current design should not be less than 0.5A.

If a DC-DC power supply is used to power the core board, the power margin should not be too large when designing the power supply. If the power design is too large, many power supplies will work in discontinuous PWM mode to ensure conversion efficiency, and the output power ripple will increase significantly, which is not conducive to the working stability of the digital signal system. If an LDO is used to power the core board, the power loss and operating temperature rise of the LDO itself should be considered during design to prevent the LDO power supply from overheating and stopping working or burning when working in a high temperature environment or an environment with poor heat dissipation.

6.1.2. Power Output

The ECK30-T13IA series core board also provides two power outputs, namely VDD_3V3_SOM and VDD_1V8_SOM, which can be used to power low-power devices on the baseboard and control the power-on timing of the baseboard I/O interface.

6.1.3. Power Control

All external I/O interfaces of the ECK30-T13IA series core board belong to the VIO power domain. The baseboard can use the VDD_3V3_SOM or VDD_1V8_SOM power output by the core board as the control signal of the baseboard I/O interface power domain.

6.1.4. Pin Definition

Power pin definition table

Pinout	Network Name	MPU	Level/power rail	type	Trace length	illustrate
97	AUGND		-	PWR		
106	AUGND		-	PWR		
135	VDD_3V3_SOM		3.3V / VIO	PWR		Maximum supply current 500mA
136	VDD_1V8_SOM		1.8V / VIO	PWR		Maximum supply current 100mA
139	VDD_5V_SOM		5V / VIN	PWR		
140	VDD_5V_SOM		5V / VIN	PWR		

6.2.Launch Configuration

6.2.1. Boot order configuration

When the ECK30-T13IA series core board starts, the processor will read the status of BOOT_Select and select the order of enumeration media. The T113 processor has two BOOT_Select pins that are multi

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plexed with the PC pins. The default internal pull-up is shown in the following table for the startup confi guration relationship.

T113 Boot Select Configuration Table

ECK30-T13IA Storage Configuration	PC5 BOOT-SEL1	PC4 BOOT-SEL0	Boot Media
--	0	0	SPI NOR => SPI NAND
--	0	1	SMHC0 => SPI NOR => Other media
SPI NAND Storage	1	0	SMHC0 => SPI NAND => Other media
eMMC storage	1	1	SMHC0 => eMMC2 => Other media

PC5 and PC4 of ECK30-T13IA series core board are not led out to the stamp hole. The core board has configured the boot sequence, and no user baseboard configuration is required. All ECK30-T13IA seri es core board configurations start from SMHC0 first, and the subsequent enumeration order varies accordi ng to the different storage methods on the board, as shown in the table above.

6.2.2. FEL pin

The ECK30-T13IA series core board supports the firmware forced burning pin FEL. When the ECK3 0-T13IA series core board is not powered on, the FEL signal is grounded. After power-on, FEL is release d, and the ECK30-T13IA series core board will enter the firmware upgrade mode. Users can design butto ns or jumpers on the baseboard to ground the FEL signal to force the processor to enter the firmware up grade mode. Since the signal has been designed with a pull-up resistor on the core board, the baseboard design only needs to consider grounding and appropriate TVS protection. Do not arbitrarily design a pull-up resistor for the FEL signal on the baseboard. If the FEL signal is not used, the signal can be left floa ting and the firmware can be upgraded through the SD card.

6.2.3. Pin Definition

Startup configuration pin definition table

Pinout	Network Name	MPU	Level/power rail	type	Trace length	illustrate
2	FEL_A18	A18	3.3V	DI		Connect a 1KΩ resistor in series

6.3.Reset button

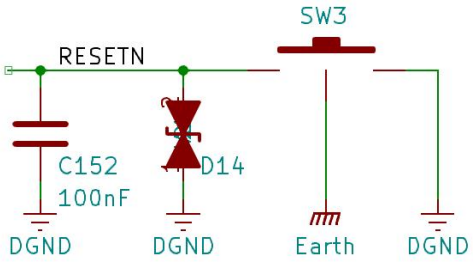
the ECK30-T13IA series core board can be connected to an external button to achieve reset control o f the processor. The RESET_M2 signal is an input-output bidirectional signal. It can be used as an extern

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al reset input to reset the processor. It is also the processor memory power reset signal output. The RES ET_M2 signal provides a 10K ohm pull-up resistor in the core board. Therefore, when the RESET_M2 si gnal is used as a manual reset input on the baseboard, do not connect the pull-up resistor, directly conne ct the button, or drive it through the OD gate. Do not drive the RESET_M2 signal through a push-pull o utput interface. When connecting the manual input button, you can place a small capacitor and TVS to re duce interference and improve ESD performance. The button reference schematic is shown in the figure b elow.

6.3.1. References



Button reference schematic

Note: Do not pull up the reset and power button signals through resistors at will. If the pull-up pow er rail is incorrect, it will cause uncertain signals to be input to the button signal interface when the syst em is in standby or shutdown.

6.3.2. Pin Definition

Button pin definition table

Pinout	Network Name	MPU	Level/power rail	type	Trace length	illustrate
4	RESET_M2	M2	3.3V	I/O		10KΩ pull up

6.3.3. LAYOUT SUGGESTIONS

- The reset signal is a sensitive signal and can be processed in a package or away from signals with greater interference ;
- Place the reset signal TVS tube as close to the button as possible.

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6.4.Reference Clock and NMI

6.4.1. REFCLK_OUT

The processor DCXO clock module can fan out a clock signal with the same frequency as the main clock through the REFCLK_OUT_J2 pin. This clock signal can be provided to the devices on the baseboard as clock input, such as the WiFi module. When using this clock reference output, consider whether the clock level, accuracy, and power-on sequence are suitable for the baseboard device. If not, it is recommended not to use this clock signal.

6.4.2. NMI

Processor non-maskable interrupt signal, mainly used for PMIC management. This pin function is not recommended for users to use. It can be left floating when not in use.

6.4.3. Pin Definition

Button pin definition table

Pinout	Network Name	MPU	Level/power rail	type	Trace length	illustrate
1	REFCLK_OUT_J2	J2	1.8V	AO		
3	NMI_N3	N3	1.8V	I/O		

6.5.Display output interface

The ECK30-T13IA series core board supports RGB888 (RGB666), dual-channel LVDS (multiplexed with RGB interface pins), MIPI DSI (multiplexed with RGB interface pins), and SPI (DBI) display interfaces. If only one set of LVDS is used on the PD I/O, the other PD I/Os can be used as normal I/Os.

- Dual-channel LVDS interface supports up to 1920×1080@60fps;
- Single-channel LVDS interface supports up to 1366×768@60fps;
- The parallel RGB interface supports up to 1920×1080@60fps;
- The SPI interface supports up to 240 × 320 @60fps;
- The 4-lane MIPI DSI interface supports up to 1920×1200@60fps .

The multiplexing relationship between the DBI interface and SPI1 is shown in the following table.

DBI and SPI1 multiplexing table

DBI Function	SPI1 Function
DBI-CSX	SPI1-CS

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DBI-SCLK	SPI1-CLK
DBI-SDO/SDA	SPI1-MOSI
DBI-SDI(WRX)/TE/DCX	SPI1-MISO
DBI-DCX/WRX	SPI1-HOLD
DBI-TE	SPI1-WP

Customers can configure the display resolution and display data format according to their needs . In screen applications, GPIO can be used to control the screen power and backlight power. PWM output can be used to control the backlight brightness. I2C and GPIO external interrupt functions can also be used to connect the touch screen. Ebyte's LCD touch screen module can be used in conjunction with it. For detailed module information, please refer to the official website https://www.ebyte.com/.

6.5.1. Interface Definition

Display interface definition table

Pinout	Network Name	MPU	Level/power rail	type	Trace length	illustrate
58	PB2_M16	M16	3.3V	I/O	1126.85	LCD0_D0
59	PB3_M15	M15	3.3V	I/O	1082.91	LCD0_D1
67	PD0_W19	W19	3.3V	I/O	1017.36	LCD0_D2 / LVDS0_V0P / DSI_D0P
68	PD1_V20	V20	3.3V	I/O	1016.69	LCD0_D3 / LVDS0_V0N / DSI_D0N
69	PD2_V19	V19	3.3V	I/O	1016.5	LCD0_D4 / LVDS0_V1P / DSI_D1P
70	PD3_U20	U20	3.3V	I/O	1016.65	LCD0_D5 / LVDS0_V1N / DSI_D1N
72	PD4_U19	U19	3.3V	I/O	1034.18	LCD0_D6 / LVDS0_V2P / DSI_CKP
73	PD5_U18	U18	3.3V	I/O	1037.15	LCD0_D7 / LVDS0_V2N / DSI_CKN
60	PB4_K16	K16	3.3V	I/O	1097.01	LCD0_D8
61	PB5_K15	K15	3.3V	I/O	1125.02	LCD0_D9
74	PD6_T19	T19	3.3V	I/O	1031.65	LCD0_D10 / LVDS0_CKP / DSI_D2P
75	PD7_T18	T18	3.3V	I/O	1031.69	LCD0_D11 / LVDS0_CKN / DSI_D2N
76	PD8_R20	R20	3.3V	I/O	1017.22	LCD0_D12 / LVDS0_V3P / DSI_D3P
77	PD9_R19	R19	3.3V	I/O	1019.47	LCD0_D13 / LVDS0_V3N / DSI_D3N
79	PD10_T17	T17	3.3V	I/O	1018.78	LCD0_D14 / LVDS1_V0P
80	PD11_R17	R17	3.3V	I/O	1018.77	LCD0_D15 / LVDS1_V0N
62	PB6_K17	K17	3.3V	I/O	1113.72	LCD0_D16
63	PB7_J15	J15	3.3V	I/O	1038.85	LCD0_D17
81	PD12_P19	P19	3.3V	I/O	1017.67	LCD0_D18 / LVDS1_V1P
82	PD13_P18	P18	3.3V	I/O	1018.78	LCD0_D19 / LVDS1_V1N
83	PD14_N17	N17	3.3V	I/O	1016.2	LCD0_D20 / LVDS1_V2P
84	PD15_N16	N16	3.3V	I/O	1019.47	LCD0_D21 / LVDS1_V2N
86	PD16_N20	N20	3.3V	I/O	1031.7	LCD0_D22 / LVDS1_CKP
87	PD17_N19	N19	3.3V	I/O	1034.48	LCD0_D23 / LVDS1_CKN
88	PD18_M19	M19	3.3V	I/O	1032.43	LCD0_CLK / LVDS1_V3P

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89	PD19_M18	M18	3.3V	I/O	1034.74	LCD0_DE / LVDS1_V3N
90	PD21_V18	V18	3.3V	I/O	1095.57	LCD0_VSYNC
91	PD20_W18	W18	3.3V	I/O	1126.38	LCD0_HSYNC

6.5.2. LAYOUT SUGGESTIONS

- The data and clock differential pairs must follow the equal length and equal distance rules, the differential pair error control is +-5mil, and the differential impedance is 100 ohms ;
- Use fewer vias for differential routing , ensure that the differential pairs are drilled at the same time , and place ground vias next to the differential pair vias ;
- The data differential pair needs to be equal in length between groups with reference to the clock differential pair , and the equal length is +-50mil ;
- The reference plane for differential routing should be complete, and the routing should not cross the split ;
- If the baseboard RGB signal is designed with a series matching resistor , it is recommended to place it close to the stamp hole of the core board ;
- The RGB signals have been processed to equal length in the core board. For the wiring length i n the core board, see the pin definition table;
- signal in the core board is controlled according to the single-ended 50Ω ±10% impedance, and the impedance control of the baseboard is recommended to be consistent;
- It is recommended that the RGB signal lines on the baseboard be of equal length, with an error range of ± 25 mil and a signal line spacing of at least 2W.

6.6.Digital camera interface

the ECK30-T13IA series core board supports 8-bit DVP interface, BT656 interface and BT601 interfa ce input. The parallel CSI interface can support a maximum pixel clock of 148.5MHz. The BT656 interfa ce can support 2*1080p@30fps input in clock double-edge sampling mode. The CSI interface of the ECK 30-T13IA series core board only supports 3.3VI/O level.

In actual backplane applications, the parallel CSI interface will occupy a large number of I/O pins, r educing other multiplexing functions. You can consider using a USB interface camera to implement the ca mera function.

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6.6.1. Interface Definition

Digital camera interface definition table

Pinout	Network Name	MPU	Level/power rail	type	Trace length	illustrate
48	PE0_V1	V1	3.3V	I/O	1012.2	CSI horizontal synchronization signal
49	PE1_U1	U1	3.3V	I/O	1012.06	CSI vertical synchronization signal
50	PE2_U2	U2	3.3V	I/O	1011.86	CSI Pixel Clock
51	PE3_U3	U3	3.3V	I/O	1010.43	CSI Master Clock
36	PE4_T2	T2	3.3V	I/O	1010.35	CSI Data Bit0
37	PE5_T3	T3	3.3V	I/O	1012.91	CSI Data Bit1
38	PE6_R1	R1	3.3V	I/O	1010.38	CSI Data Bit2
39	PE7_R2	R2	3.3V	I/O	1011.52	CSI Data Bit3
40	PE8_R3	R3	3.3V	I/O	1010.62	CSI Data Bit4
41	PE9_P2	P2	3.3V	I/O	1009.88	CSI Data Bit5
42	PE10_P3	P3	3.3V	I/O	1007.44	CSI Data Bit6
43	PE11_N1	N1	3.3V	I/O	1011.75	CSI Data Bit7

6.6.2. LAYOUT SUGGESTIONS

- The CSI signal has been processed into equal length in the core board. The length of the trace in the core board can be found in the pin definition table;
- signal in the core board is controlled according to the single-ended 50Ω ±10% impedance. It is recommended that the impedance control of the baseboard remain consistent.
- It is recommended that the CSI signal traces on the baseboard be of equal length with an error range of ± 25 mil and a signal line spacing of at least 2W.

6.7.SD/MMC card interface

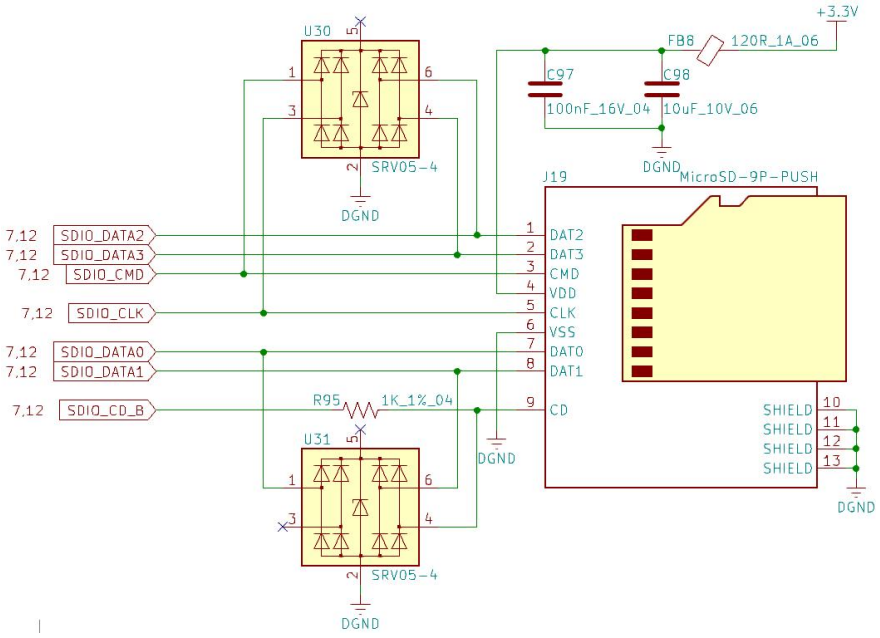
The ECK30-T13IA series core board is equipped with 3 SMHC (SD/MM host controller) controllers, including SMHC0, SMHC1, and SMHC2. SMHC0 complies with the Secure Digital Memory v3.0 protocol and is usually used to connect to SD cards. SMHC1 complies with the Secure Digital I/O v3.0 protocol and is usually used to connect to extended functions, such as WiFi modules. SMHC2 complies with the Multimedia Card v5.0 protocol and is usually used to connect to eMMC storage chips. The ECK30-T13IA series core uses SMHC2 to expand the on-board eMMC storage chip. It is recommended that the baseboard use SMHC0 to connect to the SD card. SMHC1 is recommended to expand other devices or not be used.

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The processor's I/O can be configured with on-chip pull-up resistors. These pull-up resistors can meet the pull-up requirements when the SD card interface is expanded, and the user design does not require external pull-up resistors. The core board has already connected a 33 ohm matching resistor in series with the clock signal of PF2_D2, and the user design does not require external series resistors. To expand the Micro SD card through the SMHC0 interface, you can refer to the following schematic design.

6.7.1. References



SD card reference circuit diagram

6.7.2. Pin Definition

SMHC0 interface signal pin definition

Pinout	Network Name	MPU	Level/power rail	type	Trace length	illustrate
28	PF1_C1	C1	3.3V	I/O	1129.58	SDC0_D0
27	PF0_C2	C2	3.3V	I/O	1122.36	SDC0_D1
30	PF5_E2	E2	3.3V	I/O	1131.95	SDC0_D2
32	PF4_E3	E3	3.3V	I/O	1124.16	SDC0_D3
31	PF3_D1	D1	3.3V	I/O	1130.76	SDC0_CMD
29	PF2_D2	D2	3.3V	I/O	1129.74	SDC0_CLK

6.7.3. LAYOUT SUGGESTIONS

- ❖ signal in the core board is controlled according to the single-ended 50Ω±10% impedance, and the impedance control of the baseboard is recommended to be consistent;

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- The SMHC signal has been processed to equal length in the core board. For the wiring length in the core board, see the pin definition table;
- It is recommended that the SMHC signal (excluding the insertion detection signal) on the bottom board be routed with equal length control, with an error range of ± 50 mil , and the signal line spacing be at least 2W ;
- Insert a 1K ohm resistor in series with the detection signal to improve ESD performance;
- The distance between the clock signal and other signals follows the 3W rule.

6.8.USB interface

The ECK30-T13IA series core board supports 2 USB2.0 interfaces. USB0 supports HOST and Device modes, and USB1 only supports HOST mode.

If the user uses the USB OTG function, the USB interface is recommended to use the MICRO USB interface, because the interface is a 5-wire interface with USB_ID (can be realized through GPIO function multiplexing) signal, which can be used to identify the HOST and DEVICE, thereby realizing the OTG function. If the user does not use the USB OTG function and only uses it as a USB HOST, then the USB interface can be selected as a 4-wire or 5-wire interface.

USB_OTGx_VBUS is the power supply for the USB interface I/O of the processor. To use the USB function, the USB interface I/O needs to be powered through these two pins, with a supply voltage of 5.0V±10% and a maximum supply current of 50mA

The USB interface signal of the T113 series processor does not provide a separate VBUS power supply. The USB interface signal belongs to the VIO power domain. When using the USB interface as a device mode, external HOST should be power on first. If the external HOST is powered on first, there may be a risk of leakage on the USB OTG signal, which could affect processor startup or damage interface functionality.

6.8.1. Pin Definition

USB interface signal pin definition

Pinout	Network Name	MPU	Level/power rail	type	Trace length	illustrate
129	USB1_DP_A8	A8	-	I/O	960.34	
130	USB1_DM_B8	B8	-	I/O	962.55	
132	USB0_DP_B7	B7	-	I/O	957.89	

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133	USB0_DM_C7	C7	-	I/O	959.18	

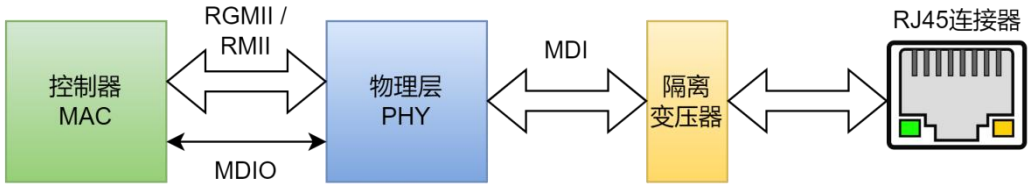
6.8.2. LAYOUT SUGGESTIONS

- The USB signal routing is controlled to be of equal length , the error within the differential pair is ± 5 mil, and the spacing between adjacent differential pairs is more than 3W;
- The differential impedance of the USB signal is controlled at 90Ω;
- Keep the USB signal cable as short as possible .

6.9.Ethernet interface

The ECK30-T13IA series core board supports 1- way 10M/100M /1000M adaptive Ethernet controller . The Ethernet controller supports RG MII and RMII interfaces. The MII interface of the ECK30-T13IA series core board is reused for the PE/PG pins and only supports 3.3V level.

Usually an RJ45 Ethernet interface is mainly composed of an Ethernet controller MAC (Media Acces s Control), an Ethernet physical layer interface PHY (Physical Layer), an Ethernet transformer, and an RJ 45 connector, as shown in the figure below.



RJ45 Ethernet components

The ECK30-T13IA series core board does not have an Ethernet PHY circuit designed in it. If the us er uses the Ethernet function, the PHY interface chip circuit needs to be designed on the baseboard. The baseboard PHY interface chip circuit design can refer to the Ebyte single-board computer product drawing s.

6.9.1. Pin Definition

Ethernet interface signal pin definition

Pinout	Network Name	MPU	Level/power rail	type	Trace length	illustrate
36	PE4_T2	T2	3.3V	I/O	1010.35	RGMII_TXD0
37	PE5_T3	T3	3.3V	I/O	1012.91	RGMII_TXD1
43	PE11_N1	N1	3.3V	I/O	1011.75	RGMII_TXD2

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34	PE12_R5	R5	3.3V	I/O	1117.23	RGMII_TXD3
38	PE6_R1	R1	3.3V	I/O	1010.38	RGMII_TXCTRL
51	PE3_U3	U3	3.3V	I/O	1010.43	RGMII_TXCK
49	PE1_U1	U1	3.3V	I/O	1012.06	RGMII_RXD0
50	PE2_U2	U2	3.3V	I/O	1011.86	RGMII_RXD1
35	PE13_R4	R4	3.3V	I/O	1011.36	RGMII_RXD2
44	PE14_N4	N4	3.3V	I/O	1009.9	RGMII_RXD3
48	PE0_V1	V1	3.3V	I/O	1012.2	RGMII_RXCTRL
45	PE15_N5	N5	3.3V	I/O	1012.78	RGMII_RXCK
40	PE8_R3	R3	3.3V	I/O	1010.62	MDC
41	PE9_P2	P2	3.3V	I/O	1009.88	MDIO

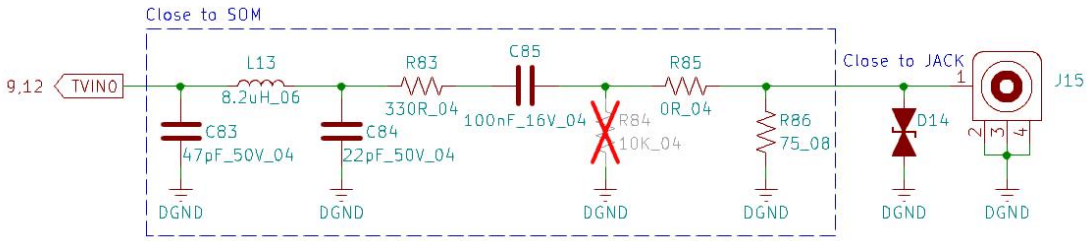
6.9.2. LAYOUT SUGGESTIONS

- ❖ RGMII signal sending and receiving groups are controlled to be equal length, with an error of ± 25mil and a line spacing of more than 2W;
- ❖ The network differential signal is controlled to be equal length, the error within the differential p air is ± 10mil , and the spacing between adjacent differential pairs is more than 3W;
- ❖ The network port transformer should be placed close to the PHY chip, and the recommended dis tance is no more than 20 mm.
- ❖ The decoupling capacitor of the power pin of the PHY chip is placed close to the PHY chip;

6.10.CVBS interface

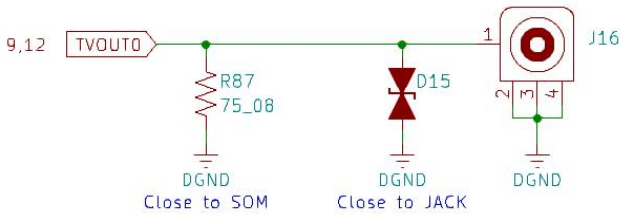
ECK30-T13IA core board provides 2 CVBS analog video inputs and 1 CVBS analog video output. Y ou only need to place a small amount of filtering, matching and protection circuits on the bottom board t o realize the analog video input and output interface functions.

6.10.1. References



CVBS input interface circuit diagram

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CVBS output interface circuit diagram

6.10.2. Pin Definition

Analog video signal pin definition

Pinout	Network Name	MPU	Level/power rail	type	Trace length	illustrate
117	TVOUT0_E19	E19	-	AO		
118	TVIN1_C9	C9	-	AI		
119	TVIN0_B9	B9	-	AI		

6.10.3. LAYOUT SUGGESTIONS

- Place TVS close to the interface;
- Matching 75 ohm resistors has power requirements, and 0805 or larger size packages are recommended;
- The trace impedance is controlled to 37.5 ohms;
- Analog signal routing should be kept away from interference and can be wrapped with ground.

6.11.Analog audio interface

The T113-i chip integrates audio codec functions and provides analog audio interfaces. The ECK30-T13IA core board leads to 2 analog audio output interfaces (LINEOUT, HPOUT) and 5 analog audio input interfaces (MICIN*3, FMIN, LINEIN).

The ECK30-T13iA core board supports headphone and microphone insertion detection. Check the insertion of the earphones through HP_DET signal and whether the earphones have microphone function through MIC_DET signal. Referring to the figure below, the HP_DET signal detects voltage changes to determine if headphones are inserted. When the earphones are not plugged in, pins 3 and 4 of the earphone jack are short circuited, and the HP_DET signal is pulled down to a low level by a 100K resistor. When the earphones are inserted, pins 3 and 4 of the earphone jack are disconnected, and the HP_DET signal is p

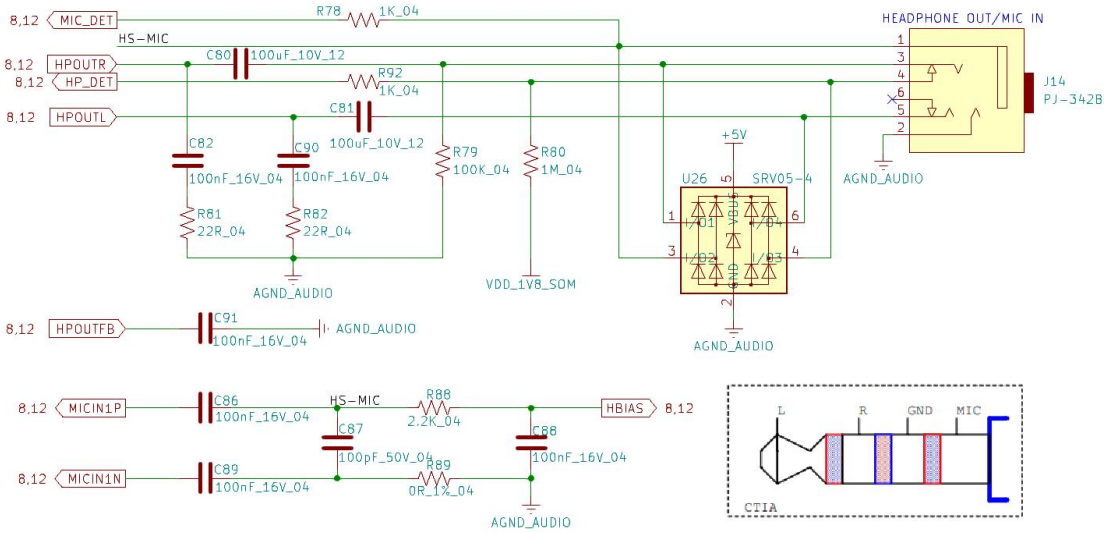
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ulled up to 1.8V by a 1M resistor (The 1.8V output from the core board). The MIC_DET interface is an ADC interface that detects the voltage of the microphone signal, determines whether the microphone is inserted, and the function of the headphone button.

The application of audio interface insertion detection circuit needs to be matched with the driver program. If you encounter driver mismatch issues during use, you can consult our software technical support.

6.11.1. References



Analog Audio Headset Interface Schematic

6.11.2. Pin Definition

Analog audio signal pin definition

Pinout	Network Name	MPU	Level/power rail	type	Trace length	illustrate
93	FMINR_C17	C17	-	AI		
94	FMINL_B17	B17	-	AI		
95	LINEINR_C16	C16	-	AI		
96	LINEINL_B16	B16	-	AI		
97	AUGND	-	AGND	PWR		Audio analog signal ground
98	MBIAS_E16	E16	-	AO		Microphone bias voltage
99	MIC_DET_A17	A17	-	AI		Microphone insertion detection
100	MICIN1P_D20	D20	-	AI		
101	MICIN1N_D19	D19	-	AI		
102	MICIN2P_E15	E15	-	AI		
103	MICIN2N_D15	D15	-	AI		
104	MICIN3P_D17	D17	-	AI		
105	MICIN3N_D16	D16	-	AI		
106	AUGND	-	AGND	PWR		Audio analog signal ground
107	LINEOUTRP_B14	B14	-	AO		

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108	LINEOUTRN_C14	C14	-	AO		
109	LINEOUTLP_B15	B15	-	AO		
110	LINEOUTLN_C15	C15	-	AO		
111	HBIAS_E17	E17	-	AO		Headphone bias voltage
112	HP_DET_A13	A13	-	AI		Headphone insertion detection
113	HPOUTR_D13	D13	-	AO		
114	HPOUTFB_E13	E13	-	AO		
115	HPOUTL_F13	F13	-	AO		

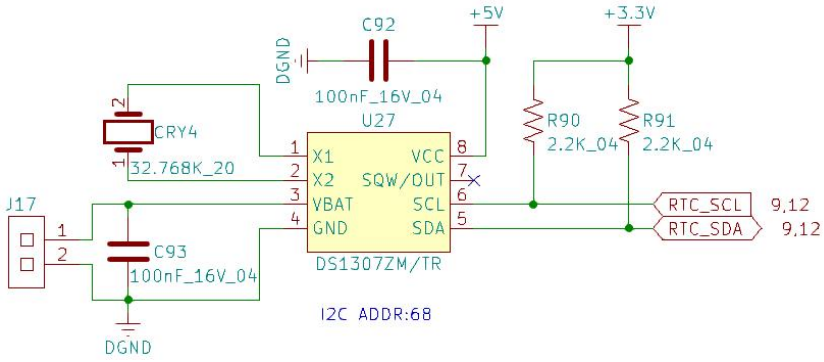
6.11.3. LAYOUT SUGGESTIONS

- ❖ Place TVS close to the interface;
- ❖ Analog signal routing should be kept away from interference and can be wrapped with ground.

6.12.RTC

ECK30-T13IA core board . If the user needs this RTC function, it can be expanded on the baseboar d through the I2C bus.

6.12.1. References



RTC reference circuit diagram

6.13.Digital Audio Interface

ECK30-T13IA core board supports up to 2 digital audio interfaces (PCM/I2S). In the baseboard cir cuit design, the digital audio interface signal needs to be connected to the audio codec chip , and the au dio interface functions such as headphones, microphones, and speakers are realized through the audio code c chip .

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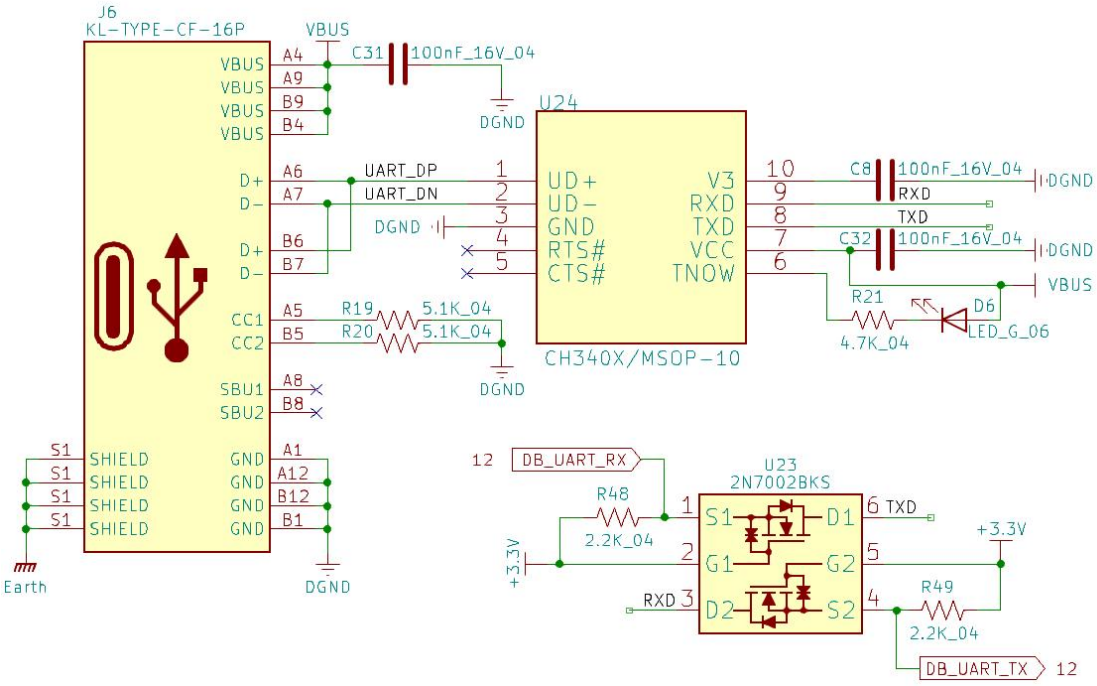
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6.14.UART Interface

The ECK30-T13IA core board supports up to 6 asynchronous serial ports and a baud rate of up to 4 Mbps. The core board uses UART 0 as the debug serial port by default.

6.14.1. References

For debugging convenience, the debug serial port can be brought out as a USB interface through a USB-to-serial port chip on the baseboard. The USB-to-serial port circuit schematic can be found in the fi gure below. The CH340X and MOSFET, which can effectively solve the problems of serial port I/O level compatibility and power domain power-on timing.



USB debug serial port reference schematic

6.15.SPI interface

The ECK30-T13IA series core board leads to 1 SPI interface , supporting master/slave mode. SPI sig nals include SPI_CLK, SPI_SS, SPI_MOSI and SPI_MISO. When designing, you must first confirm the re lationship between the master and slave devices, and then confirm the direction of the MOSI and MISO s ignals. 1 SPI only provides 1 chip select signal .

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6.16.I2C Interface

The ECK30-T13IA series core board supports 4-way I2C controllers and 2 clock frequency modes. The rate in standard mode is 100Kbit/s and the rate in fast mode is 400Kbit/s.

Several devices can be mounted on the same I2C bus. The following points should be noted when designing the schematic:

a) Check whether the device addresses on the same bus conflict;

b) Ensure that each I2C bus has a pair of pull-up resistors. The recommended resistance is 2.2K~10K, but do not add multiple resistors.

c) The core board does not provide an I2C bus pull-up resistor, so the user needs to pull it up when using the baseboard;

d) Check whether the I2C interface level of the device is 3.3V. If not, a level conversion circuit needs to be added;

e) Check whether the I2C interface power rails are consistent. When I2C interfaces in different time domains are interconnected, the bus switch circuit needs to be considered;

f) Do not use too many devices on the same bus, otherwise the load capacitance limit of 400pF required by the I2C specification may be exceeded, affecting the signal waveform.

6.17.CAN interface

ECK30-T13IA series core board supports 2-way CAN controllers and CAN 2.0A and CAN 2.0B protocols. It only needs an external CAN transceiver to perform CAN communication.

6.18.ADC Interface

The ECK30-T13IA series core board provides three types of ADC interfaces, namely 1-way LRADC (Low Rate ADC), 2-way GPADC (General Purpose ADC), and 4-way TPADC (Touch Panel ADC).

LRADC:

- 6-bit resolution, used for key voltage recognition, maximum sampling rate 2KHz, sampling voltage range: 0~1.266V;
- When LRADC is used for key recognition, if the key adopts voltage-dividing resistor mode, it is recommended to use 1% precision resistor;

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- If LRADC is not used, the core board pin can be left floating, and a 51K pull-up to AVCC is provided on the board.

GPADC:

- 12bit resolution, maximum sampling rate 1MHz, sampling voltage range: 0~1.8V;
- GPADC is not recommended for voltage identification of I/O interfaces with external surges or high voltages to avoid damage to the chip interface.

TPADC:

- 4-channel TPADC interface, 12-bit resolution, 8-bit sampling accuracy, maximum sampling rate 1 MHz, can be used to connect 4-wire RTP screen or used as AD_KEY function.

6.19.GPIO interface

The ECK30-T13IA series core board can provide up to 79 GPIO interfaces, but most of them have multiplexing functions. Users can flexibly configure GPIO according to their own needs.

6.20.Hardware Design Checklist

- Power rail: Check whether there is an inconsistency in the power rails of the I/O interface application, such as a 1.8V signal connected to a 3.3V signal. If there is a need to connect signals with different power rails, a level conversion circuit should be used.
- Power-on sequence: Check whether the signals connecting the baseboard and the core board are powered on first, or whether the power-on time of the two board signals is very different.
- Pull-up and pull-down resistors: The output state of the multiplexed I/O interface is uncertain before the power-on software configuration. If the signal needs to maintain a certain level when powered on, pull-up and pull-down resistors should be designed on the baseboard. Some functional signals also need to be designed with pull-up or pull-down resistors on the baseboard, such as I2C signals. When designing pull-up resistors, attention should be paid to the design of the pull-up power rail.
- ESD protection: The corresponding ESD protection design should be considered for the external interface signal. The selection of ESD solution should take into account the requirements of signal rate, communication protocol and application environment.

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- High-speed signals should be of equal length: High-speed signals should consider the equal length design of PCB, including USB, Ethernet, SDIO, display, etc.
- Impedance control: High-speed signals should consider PCB impedance control. The key to impedance control is to maintain impedance continuity. The baseboard should be designed with reference to the impedance of the core board signal.

7. Software Resources

The ECK30-T13IA series core board is equipped with an operating system based on the Linux 5.4.61 kernel. The development board comes with a cross-compilation tool chain required for embedded Linux system development, U-boot source code, Linux kernel and driver module source code, as well as various development and debugging tools suitable for Windows desktop environment and Linux desktop environment.

operating system:

Ubuntu 18.04 system

System source code:

u-boot 2018.07

Kernel 5.4.61

Buildroot 201902

Buildroot 202205

openwrt

Development environment and tools:

USB burning tool: PhoenixSuit

SD card burning tool: PhoenixCard

7.1.System resources

System Software Resource Table

category	name	describe	Source code
SPL	spl-pub	Boot0, boot uboot	<SDK>/ brandy/brandy-2.0/spl-pub /
BOOT	u-boot 2018.07	Bootloader	<SDK>/brandy/brandy-2.0/u-boot-2018/
Kernel	Kernel 5.4.61	Linux Kernel	<SDK>/kernel/linux-5.4/
Device Driver	Audio	Built-in audio driver	sound/soc/sunxi_v2/*
	AWlink	CAN Driver	drivers/net/can/sunxi_awlink.c
	GMAC	Built-in MAC driver	drivers/net/ethernet/allwinner/sunxi-gmac.c

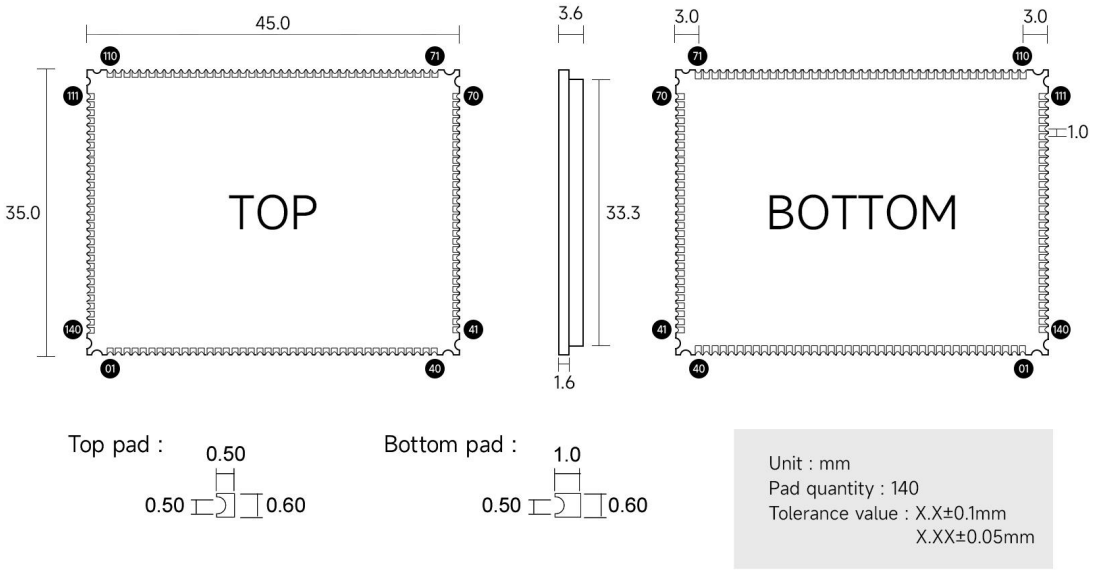
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	GPADC	GPADC Driver	drivers/input/sensor/sunxi_gpadc.c
	GPIO	GPIO Driver	drivers/pinctrl/sunxi
	LCD	Disp2 display driver	drivers/video/fbdev/sunxi/disp2/disp/lcd/
	LRADC	Key module driver	drivers/input/keyboard/sunxi-keyboard.c
	SMHC	MMC Driver	drivers/mmc/host/sunxi-mmc.c
	SPI	SPI Driver	drivers/spi/spi-sunxi.c
	SPI-NAND	SPI-NAND Driver	drivers/mtd/awnand/spinand
	TVD	CVBS Input	drivers/media/platform/sunxi- tvd/
	TVE	CVBS output	drivers/video/fbdev/sunxi/disp2/tv/
	TWI	I2C Driver	drivers/i2c/busses/i2c-sunxi.c
	UART	Serial port driver	drivers/tty/serial/sunxi-uart.c
	VIN	CSI Driver	drivers/media/platform/sunxi-vin/
operating system	Buildroot 201902	Buildroot 201902	<SDK>/buildroot/buildroot-201902
	Buildroot 202205	Buildroot 202205 version	<SDK>/buildroot/buildroot-202205
	openwrt	openwrt	<SDK>openwrt/openwrt
Development Tools	PhoenixSuit	USB burning tool	/tools/ PhoenixSuit
	PhoenixCard	SD card burning tool	/tools/PhoenixCard

8. Structural dimensions

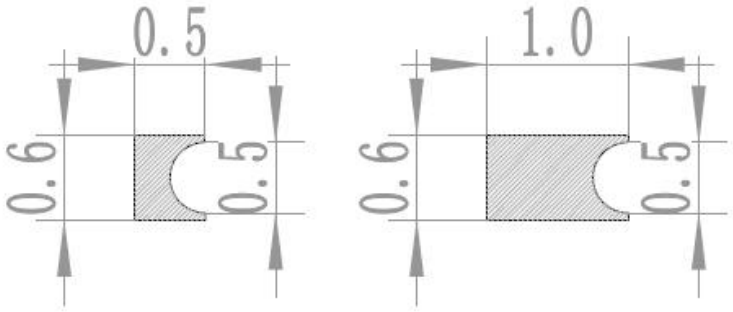
The ECK30-T13IA series core board adopts 140 PIN, 1.0mm pitch stamp hole interface, which can be STM soldered or hand soldered. There are no components and exposed traces on the bottom of the core board, and the bottom board design is simple. The core board structure size is shown in the figure below.



Stamp hole core board structure size drawing

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Stamp hole size chart

9. Welding Instructions

9.1.Reflow temperature

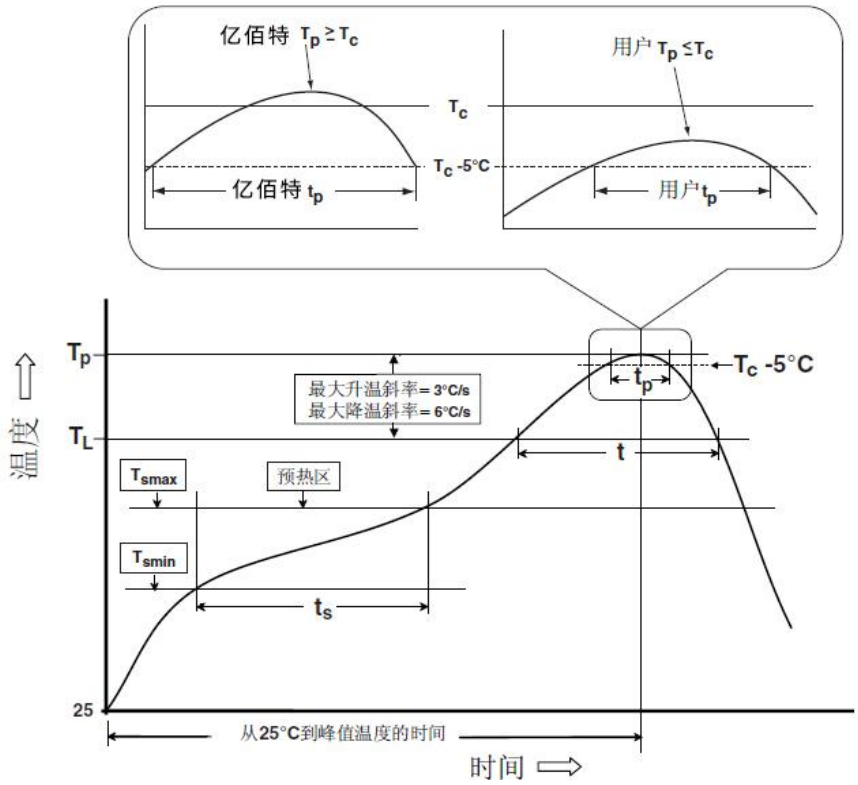
Reflow Temperature Table

Reflow profile characteristics		Leaded process assembly	Lead-free assembly
Preheating/keeping	Minimum temperature (Tsmin)	100℃	150℃
	Maximum temperature (Tsmax)	150℃	200℃
	Time (Tsmin~Tsmin)	60-120 seconds	60-120 seconds
Heating slope (TL~Tp)		3℃/sec, max.	3℃/sec, max.
Liquidus temperature (TL)		183℃	217℃
Keep time above TL		60~ 90 seconds	60~ 90 seconds
Package peak temperature Tp		Users must not exceed the temperature stated on the product's "Moisture Sensitivity" label.	Users must not exceed the temperature stated on the product's "Moisture Sensitivity" label.
The time (Tp) within 5° C of the specified classification temperature (Tc) is shown in the figure below.		20 seconds	30 seconds
Cooling slope (Tp~TL)		6℃/sec, max.	6℃/sec, max.
Time from room temperature to peak temperature		6 minutes, longest	8 minutes, longest
※The peak temperature (Tp) tolerance of the temperature curve is defined as the upper limit of the user			

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9.2.Reflow Oven Profile



Reflow Oven Profile

10. Reference Documentation

T113-i_V1.9.pdf

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11. Revision Notes

Revision Notes Table

Version	Modifications	Modification time	prepared by	Proofreading	Approval
V1.0	First Draft	24-09-25	WFX	Wlq	WFX
V1.1	Modify SMHC1 and USB section description.	24-11-25	WFX	Wlq	WFX
V1.2	1. Update the audio interface reference circuit, change the design of the HP_DET signal pull-down resistor, and add descriptions related to the insertion detection circuit. 2. Update the reference circuit of the debugging serial port.	24-12-18	WFX	Wlq	WFX

12. Contact Us

Technical support: support@cdebyte.com

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