Product Manual

ECK20-6Y28C Core Board



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1. Product Overview

2. Product Introduction

he Ebyte ECK20-6Y28C series core board is a low-cost, low-power, high-performance, and high-reliability embedded core board based on the NXP Cortex-A7 core i.MX6ULL processor, designed with BTB connectors. It can be widely used in industrial control, HMI, IoT, and other fields.

The NXP i.MX6ULL processor features a single ARM Cortex-A7 core with a maximum frequency of 792MHz, providing 1 LCD display, 1 digital camera, 2 100M Ethernet, 2 USB OTG, 8 UART, 2 SDIO, 2 CAN, and multiple GPIOs.

The ECK20-6Y28C series core board includes 3 specific product models. They mainly differ in memory capacity and storage configuration. Customers can choose the appropriate model according to their needs. For product selection, please refer to the product selection chapter.

The physical diagram of the ECK20-6Y28C series core board (no components on the bottom side) is as follows:



Physical picture

2.1.Product Features

1、Processor: i.MX6ULL series industrial-grade processor, 792MHz;

2、Memory: On-board DDR3L SDRAM, 256MB/512GB optional;

3、Storage: 8GB eMMC or 512MB parallel NAND FLASH optional;

4、Display: 1 parallel display interface, maximum resolution support WXGA (1366×768@60fps);

5、Network: 10/100 adaptive Ethernet MII/RMII interface;

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6、USB: 2 USB2.0 OTG interfaces;

7、SDIO: 2 MMC/SD/SDIO card interfaces (eMMC configuration only supports 1 SDIO interface);

8、Multiple expansion I/O interfaces: including UART, CAN, I2C, SPI, SAI, ADC, GPIO, etc;

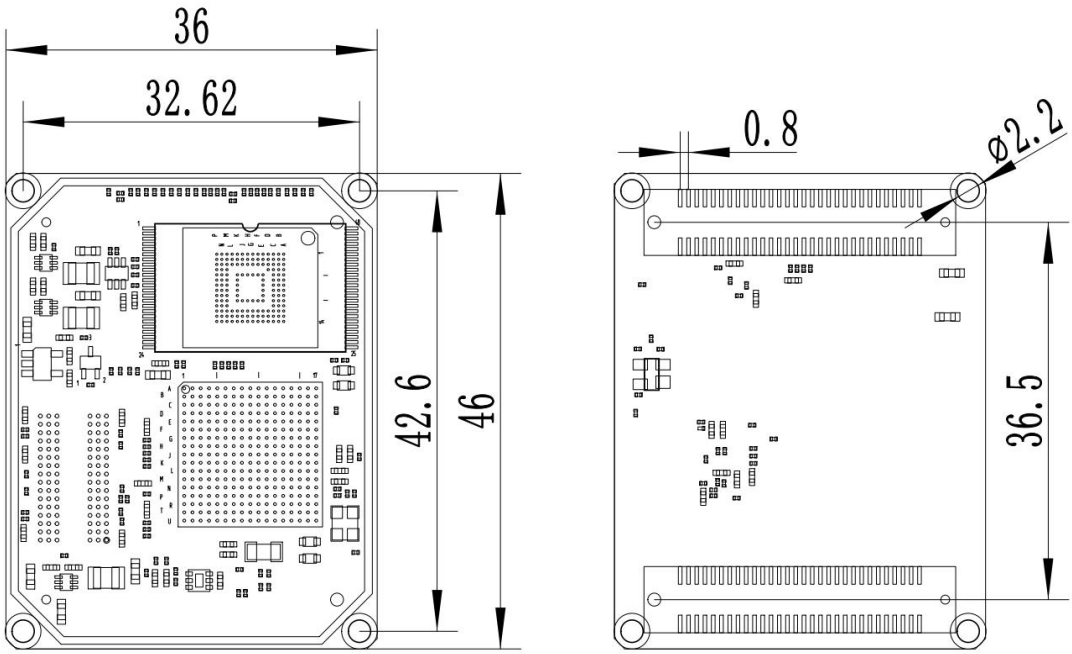
9、Supports on-chip watchdog function (timeout can cause processor reset);

10、Supports on-chip RTC function;

11、Interface form: 120-pin BTB connector;

12、Power supply: Single DC +5V±10%@0.3A power input;

13、Structural dimensions: 46×36×6.8mm, PCB + shield height 3mm, BTB connector height 5mm, di mensions as shown below:



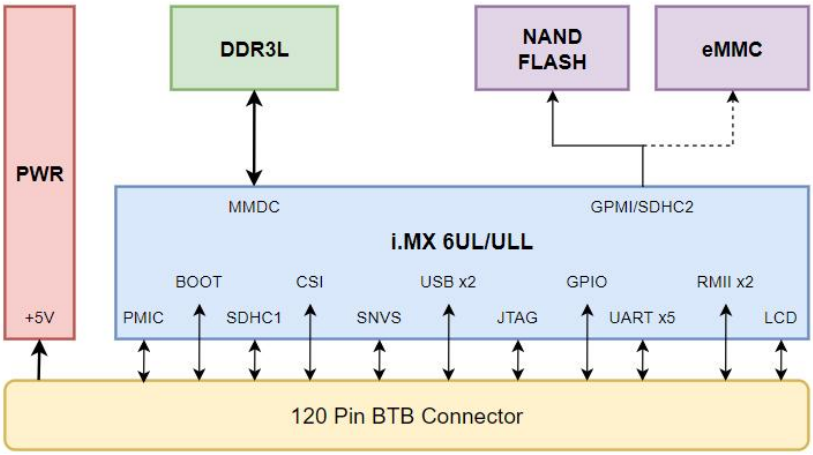
Dimensions

14、Operating temperature: Commercial grade: 0℃-70℃, Industrial grade: -40℃-85℃;

15、PCB process:8-layer board design,immersion gold,lead-free process

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2.2.Core Board Functional Block Diagram



Functional Block Diagram

2.3.Typical Applications

- Smart home;
- Smart toys;
- Smart city;
- Tablet PC;
- IoT gateway;
- Advertising all-in-one machine;
- Industrial all-in-one machine;
- Industrial control motherboard;
- Robots, drones.

3. Product Selection

3.1.Model Configuration

The ECK20-6Y28C series core board selection configuration table is as follows:

Product Selection and Configuration Table

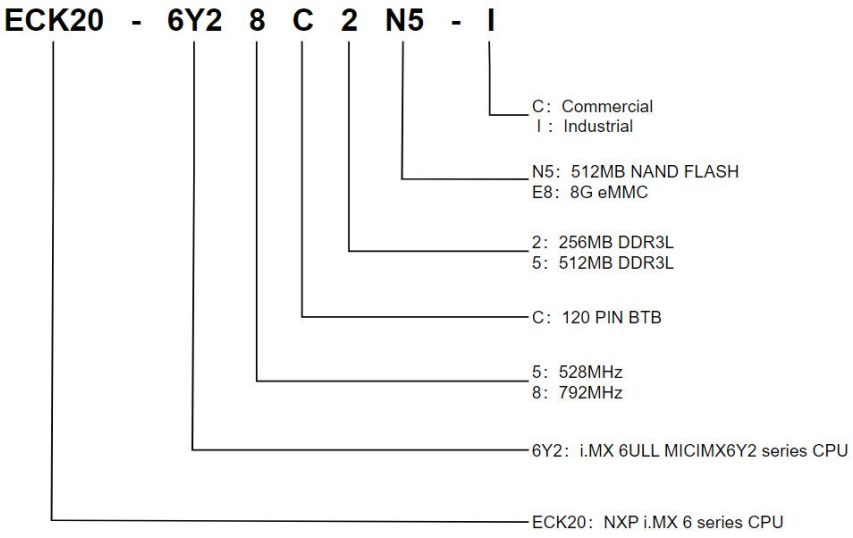
Serial number	Product Model	Processor model	Memory	storage	Operating temperature
1	ECK20-6Y28C2N5-I	MCIMX6Y2CVM08AB	256MB DDR3L	512MB NAND	Industrial Grade -40℃ ~ 85℃
2	ECK20-6Y28C5E8-C	MCIMX6Y2CVM08AB	512MB DDR3L	8GB eMMC	Commercial Grade 0℃ ~ 70℃
3	ECK20-6Y28C5E8-I	MCIMX6Y2CVM08AB	512MB	8GB	Industrial Grade

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			DDR3L	eMMC	-40℃ ~ 85℃

3.2.Model Code

The product model code description is as follows:



Model code illustration

4. Quick Experience

Choose Ebyte's single-board computer products to quickly experience the typical application functions, baseboard design, and software development of the ECK20-6Y28C core board.

5. Functions and Parameters

5.1.Product Functions

The ECK20-6Y28C series core board mainly integrates the processor, memory, storage, and power sys tem, and leads out all I/O pins of the processor. Users can design the baseboard according to their own needs to apply the I/O resources on the core board, and multiplex the I/O into the functions they need.

The following table lists the main functional parameters integrated on the ECK20-6Y28C series core board and the functional parameters of the multiplexed I/O resources. The description of each I/O functio n is the maximum index that the core board can use the I/O function without using other I/O functions (for example, after using 1 24-bit LCD interface function and 2 network interface functions, 8 UART fun ctions cannot be implemented).

Product Features

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product	Functional Description	
processor	MCIMX6Y2CVM08AB; i.MX 6ULL Applications Processors for Industrial; Single Arm Cortex-A7 core, 792MHz;	
storage	Memory	On-board DDR3L SDRAM, 16-bit width, 256MB/512MB optional;
	FLASH	On-board 8GB eMMC / on-board 512MB parallel NAND FLASH optional;
show	1 parallel display interface, maximum resolution supports WXGA (1366×768@60fps); Support 24bit, 18bit, 16bit, 8bit parallel display output;	
Camera	1 parallel camera interface, supporting up to 24-bit data and 85MHz clock; Support 24bit, 16bit, 10bit, 8bit data input; Support BT.656 data format;	
USDHC	2-way MMC/SD/SDIO card interface; 1bit or 4bit mode SD/SDIO card,Maximum support for UHS-I SDR-104 mode; 1bit, 4bit or 8bit mode MMC card, maximum support DDR mode; 4-bit or 8-bit mode eMMC, supporting up to HS200 mode;	
USB	2-way USB 2.0 OTG;	
Audio	3-way I2S/SAI/AC97, maximum 1.4Mbps per way; Support ESAI audio interface; Support SPDIF audio interface;	
Serial Port	8-channel UART, maximum 5Mbps per channel;	
SPI	4-channel eCSPI (Enhanced CSPI), maximum 52Mbps per channel;	
Ethernet	2-way 10/100 Ethernet MAC, support IEEE1588, support RMII;	
I2C	4-way I2C, maximum 400Kbps per channel;	
CAN	2-way CAN interface, supporting CAN 2.0B protocol;	
PWM	8-channel PWM, maximum clock frequency 66MHz;	
ADC	2 12-bit ADCs, supporting up to 10 input channels;	
EIM	Support EIM (External Interface Module), expandable NOR FLASH or PSRAM, etc.;	
JTAG	Support System JTAG Controller;	
TIMER	2 GPT (General Purpose Timer) timer functions;	
WDT	3 Watchdog timer functions;	
keyboard	1 8×8 matrix keyboard function;	
GPIO	105 (maximum) GPIO, supporting interrupt function;	

5.2.Environmental Characteristics

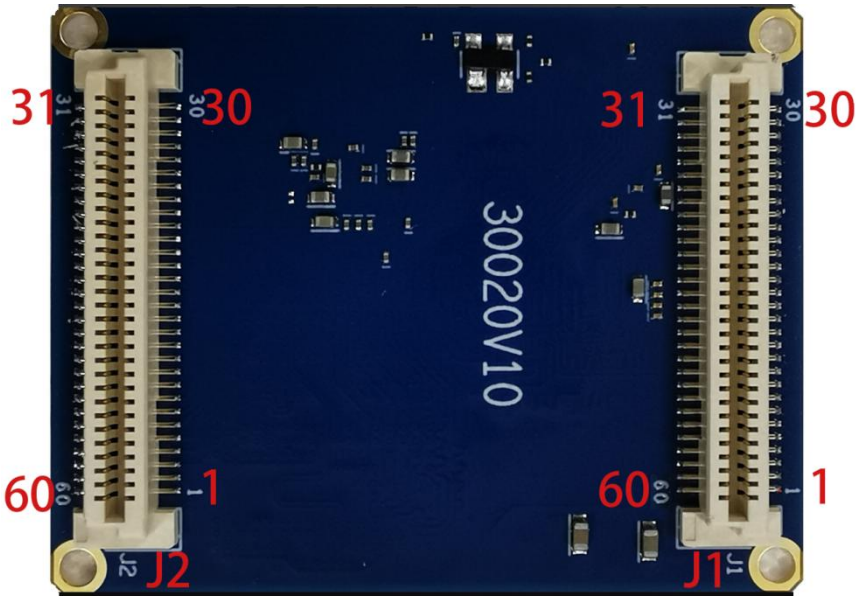
Environmental characteristics table

Operating temperature	Commercial Grade	0℃ ~ 70℃;
	Industrial Grade	-40℃ ~ 85℃;
Storage temperature	-40 ~ 85℃;	
Operating humidity	5~95% humidity, non-condensing;	
Storage humidity	60℃@95% humidity, non-condensing;	

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5.3.I/O Characteristics

5.3.1. I/O Pin Definition



Pin numbering diagram

Pin Definition Table

Pinout	Network Name	MPU	Level/Power Rail	type	Trace length	illustrate
J1-1	CSI_HSYNC	F3	3.3V/NVCC_CSI	I/O	1346.67	
J1-2	CSI_MCLK	F5	3.3V/NVCC_CSI	I/O	1350.47	
J1-3	CSI_DATA2	E2	3.3V/NVCC_CSI	I/O	1349.88	
J1-4	CSI_DATA6	D2	3.3V/NVCC_CSI	I/O	1344.27	
J1-5	CSI_PIXCLK	E5	3.3V/NVCC_CSI	I/O	1348.42	
J1-6	CSI_DATA5	D3	3.3V/NVCC_CSI	I/O	1351.41	
J1-7	LCD_DATA0	B9	3.3V/NVCC_3V3	I/O	1126.87	47K pull down
J1-8	LCD_DATA1	A9	3.3V/NVCC_3V3	I/O	1120.26	47K pull down
J1-9	LCD_DATA2	E10	3.3V/NVCC_3V3	I/O	1120.91	47K pull down
J1-10	LCD_DATA3	D10	3.3V/NVCC_3V3	I/O	1121.35	47K pull down
J1-11	LCD_DATA4	C10	3.3V/NVCC_3V3	I/O	1117.53	47K pull down
J1-12	LCD_DATA5	B10	3.3V/NVCC_3V3	I/O	1118.87	47K pull down
J1-13	LCD_DATA6	A10	3.3V/NVCC_3V3	I/O	1118.25	47K pull down
J1-14	LCD_DATA7	D11	3.3V/NVCC_3V3	I/O	1117.90	47K pull down
J1-15	LCD_DATA8	B11	3.3V/NVCC_3V3	I/O	1116.88	47K pull down
J1-16	LCD_DATA9	A11	3.3V/NVCC_3V3	I/O	1120.64	47K pull down
J1-17	LCD_DATA10	E12	3.3V/NVCC_3V3	I/O	1118.52	47K pull down
J1-18	LCD_DATA11	D12	3.3V/NVCC_3V3	I/O	1116.43	47K pull down
J1-19	LCD_DATA12	C12	3.3V/NVCC_3V3	I/O	1111.73	47K pull down

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J1-20	LCD_DATA13	B12	3.3V/NVCC_3V3	I/O	1111.69	47K pull down
J1-21	LCD_DATA14	A12	3.3V/NVCC_3V3	I/O	1116.77	47K pull down
J1-22	LCD_DATA15	D13	3.3V/NVCC_3V3	I/O	1119.49	47K pull down
J1-23	LCD_DATA16	C13	3.3V/NVCC_3V3	I/O	1115.45	47K pull down
J1-24	LCD_DATA17	B13	3.3V/NVCC_3V3	I/O	1113.94	47K pull down
J1-25	LCD_DATA18	A13	3.3V/NVCC_3V3	I/O	1112.83	47K pull down
J1-26	LCD_DATA19	D14	3.3V/NVCC_3V3	I/O	1112.36	47K pull down
J1-27	LCD_DATA20	C14	3.3V/NVCC_3V3	I/O	1123.00	47K pull down
J1-28	LCD_DATA21	B14	3.3V/NVCC_3V3	I/O	1121.71	47K pull down
J1-29	LCD_DATA22	A14	3.3V/NVCC_3V3	I/O	1121.90	47K pull down
J1-30	LCD_DATA23	B16	3.3V/NVCC_3V3	I/O	1115.26	47K pull down
J1-31	ENET2_TX_CLK	D17	3.3V/NVCC_3V3	I/O	1072.76	10ohm in series
J1-32	ENET2_TX_EN	B15	3.3V/NVCC_3V3	I/O	1070.66	
J1-33	ENET2_RX_EN	B17	3.3V/NVCC_3V3	I/O	1507.52	
J1-34	ENET2_RX_ER	D16	3.3V/NVCC_3V3	I/O	1514.31	
J1-35	ENET2_TX_DATA1	A16	3.3V/NVCC_3V3	I/O	1066.33	
J1-36	ENET2_TX_DATA0	A15	3.3V/NVCC_3V3	I/O	1069.09	
J1-37	ENET2_RX_DATA1	C16	3.3V/NVCC_3V3	I/O	1504.76	
J1-38	ENET2_RX_DATA0	C17	3.3V/NVCC_3V3	I/O	1513.40	
J1-39	SNVS_TAMPER6	N11	3.3V/SNVS_IN	I/O	1021.79	
J1-40	RESETN		3.3V/SNVS_IN	I		50K pull up
J1-41	PWR_ON_EN		3.3V/SNVS_IN	O		
J1-42	VBAT		3.3V/SNVS_IN	PWR		Diode in series
J1-43	LCD_VSYNC	C9	3.3V/NVCC_3V3	I/O	1121.21	
J1-44	LCD_HSYNC	D9	3.3V/NVCC_3V3	I/O	1117.66	
J1-45	LCD_CLK	A8	3.3V/NVCC_3V3	I/O	1119.18	10ohm in series
J1-46	LCD_ENABLE	B8	3.3V/NVCC_3V3	I/O	1114.93	
J1-47	GPIO1_IO05	M17	3.3V/NVCC_3V3	I/O	2700.36	SD1_VSELECT
J1-48	SNVS_TAMPER9	R6	3.3V/SNVS_IN	I/O	1295.30	
J1-49	SD1_DATA0	B3	3.3V/1.8V/NVCC_SD	I/O	1150.61	10K pull up
J1-50	SD1_DATA1	B2	3.3V/1.8V/NVCC_SD	I/O	1149.15	
J1-51	SD1_DATA3	A2	3.3V/1.8V/NVCC_SD	I/O	1152.75	
J1-52	SD1_DATA2	B1	3.3V/1.8V/NVCC_SD	I/O	1151.28	
J1-53	SD1_CMD	C2	3.3V/1.8V/NVCC_SD	I/O	1149.57	10K pull up
J1-54	SD1_CLK	C1	3.3V/1.8V/NVCC_SD	I/O	1155.73	10ohm in series
J1-55	CSI_DATA4	D4	3.3V/NVCC_CSI	I/O	1353.49	
J1-56	CSI_DATA0	E4	3.3V/NVCC_CSI	I/O	1354.05	
J1-57	CSI_DATA1	E3	3.3V/NVCC_CSI	I/O	1356.27	
J1-58	CSI_DATA7	D1	3.3V/NVCC_CSI	I/O	1347.28	
J1-59	CSI_DATA3	E1	3.3V/NVCC_CSI	I/O	1353.75	
J1-60	CSI_VSYNC	F2	3.3V/NVCC_CSI	I/O	1348.21	
J2-1	VIN_5V		5V/VIN_5V	PWR		
J2-2	VIN_5V		5V/VIN_5V	PWR		

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J2-3	SNVS_TAMPER4	P9	3.3V/SNVS_IN	I/O	923.00	
J2-4	PWRBTN	R8	3.3V/SNVS_IN	I		100K pull up in MPU
J2-5	SNVS_TAMPER1	R9	3.3V/SNVS_IN	I/O	785.02	
J2-6	SNVS_TAMPER0	R10	3.3V/SNVS_IN	I/O	752.02	
J2-7	BOOT_MODE0	T10	3.3V/SNVS_IN	I/O	705.37	100K pull down in MPU
J2-8	BOOT_MODE1	U10	3.3V/SNVS_IN	I/O	654.31	100K pull down in MPU
J2-9	SNVS_TAMPER8	N9	3.3V/SNVS_IN	I/O	849.47	
J2-10	SNVS_TAMPER7	N10	3.3V/SNVS_IN	I/O	877.01	
J2-11	SNVS_TAMPER5	N8	3.3V/SNVS_IN	I/O	1037.04	
J2-12	SNVS_TAMPER2	P11	3.3V/SNVS_IN	I/O	910.31	
J2-13	GPIO1_IO02	L14	3.3V/NVCC_3V3	I/O	978.92	
J2-14	GPIO1_IO04	M16	3.3V/NVCC_3V3	I/O	1176.59	
J2-15	GPIO1_IO09	M15	3.3V/NVCC_3V3	I/O	938.84	
J2-16	GPIO1_IO08	N17	3.3V/NVCC_3V3	I/O	960.66	
J2-17	JTAG_TDI	N16	3.3V/NVCC_3V3	I/O	928.65	
J2-18	JTAG_TDO	N15	3.3V/NVCC_3V3	I/O	828.53	
J2-19	JTAG_TCK	M14	3.3V/NVCC_3V3	I/O	770.53	10K pull down
J2-20	JTAG_TMS	P14	3.3V/NVCC_3V3	I/O	695.30	
J2-21	JTAG_TRST_B	N14	3.3V/NVCC_3V3	I/O	668.70	
J2-22	JTAG_MOD	P15	3.3V/NVCC_3V3	I/O	623.76	10K pull down
J2-23	ENET1_TX_DATA0	E15	3.3V/NVCC_3V3	I/O	1342.13	
J2-24	ENET1_RX_DATA1	E17	3.3V/NVCC_3V3	I/O	1018.22	
J2-25	ENET1_RX_EN	E16	3.3V/NVCC_3V3	I/O	1006.93	
J2-26	ENET1_RX_DATA0	F16	3.3V/NVCC_3V3	I/O	1008.26	
J2-27	ENET1_TX_EN	F15	3.3V/NVCC_3V3	I/O	1333.67	
J2-28	ENET1_TX_DATA1	E14	3.3V/NVCC_3V3	I/O	1347.76	
J2-29	ENET1_TX_CLK	F14	3.3V/NVCC_3V3	I/O	1343.51	10ohm in series
J2-30	ENET1_RX_ER	D15	3.3V/NVCC_3V3	I/O	1013.51	
J2-31	UART5_TX_DATA	F17	3.3V/NVCC_3V3	I/O	971.23	
J2-32	UART5_RX_DATA	G13	3.3V/NVCC_3V3	I/O	1085.64	
J2-33	UART4_TX_DATA	G17	3.3V/NVCC_3V3	I/O	908.74	
J2-34	UART4_RX_DATA	G16	3.3V/NVCC_3V3	I/O	952.88	
J2-35	UART3_RTS_B	G14	3.3V/NVCC_3V3	I/O	972.04	
J2-36	UART3_CTS_B	H15	3.3V/NVCC_3V3	I/O	1026.32	
J2-37	UART3_RX_DATA	H16	3.3V/NVCC_3V3	I/O	1245.58	
J2-38	UART3_TX_DATA	H17	3.3V/NVCC_3V3	I/O	1010.03	
J2-39	UART2_CTS_B	J15	3.3V/NVCC_3V3	I/O	1323.24	
J2-40	UART2_RTS_B	H14	3.3V/NVCC_3V3	I/O	1614.01	
J2-41	UART2_RX_DATA	J16	3.3V/NVCC_3V3	I/O	1701.66	
J2-42	UART2_TX_DATA	J17	3.3V/NVCC_3V3	I/O	1007.48	
J2-43	UART1_RTS_B	J14	3.3V/NVCC_3V3	I/O	1835.40	SD1_CD

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J2-44	GPIO1_IO06	K17	3.3V/NVCC_3V3	I/O	926.46	
J2-45	GPIO1_IO07	L16	3.3V/NVCC_3V3	I/O	914.25	
J2-46	UART1_RX_DATA	K16	3.3V/NVCC_3V3	I/O	964.86	
J2-47	GPIO1_IO03	L17	3.3V/NVCC_3V3	I/O	1105.24	
J2-48	UART1_CTS_B	K15	3.3V/NVCC_3V3	I/O	1080.04	
J2-49	GPIO1_IO01	L15	3.3V/NVCC_3V3	I/O	998.61	
J2-50	UART1_TX_DATA	K14	3.3V/NVCC_3V3	I/O	991.95	
J2-51	GPIO1_IO00	K13	3.3V/NVCC_3V3	I/O	916.25	
J2-52	USB_OTG1_CHD_B	U16	3.3V/VBUS_3V	I/O	1069.72	
J2-53	USB_OTG1_DN	T15	3.3V/VBUS_3V	I/O	1209.28	
J2-54	USB_OTG1_DP	U15	3.3V/VBUS_3V	I/O	1208.30	
J2-55	USB_OTG2_DN	T13	3.3V/VBUS_3V	I/O	1243.24	
J2-56	USB_OTG2_DP	U13	3.3V/VBUS_3V	I/O	1243.75	
J2-57	USB_OTG1_VBUS	T12	5V/VBUS_5V	PWR		
J2-58	USB_OTG2_VBUS	U12	5V/VBUS_5V	PWR		
J2-59	DGND		GDN/DGND	PWR		
J2-60	DGND		GDN/DGND	PWR		

Note: The unit of trace length is mil.

5.3.2. I/O Impedance Control

Generally, the impedance of single-ended signals is controlled at 50 ohms, while differential signal impedance control is as shown in the table below.

Differential trace impedance control table

Pin	Pin Name	Trace Length	Impedance Control	Description
J2-53/J2-54	USB_OTG1_DN/USB_OTG1_DP	1209.28/1208.30	90ohms	USB signals
J2-55/J2-56	USB_OTG2_DN/USB_OTG2_DP	1243.24/1243.75	90ohms	USB signals

5.4.Electrical Characteristics

5.4.1. Power Consumption

Note: The following parameters were measured under normal temperature conditions on the ECK20-6Y28C5E8-I core board, excluding power consumption from the baseboard. Heavy load power consumption measurements were taken without display output, SDIO access on the baseboard, and network access

Power Consumption Table

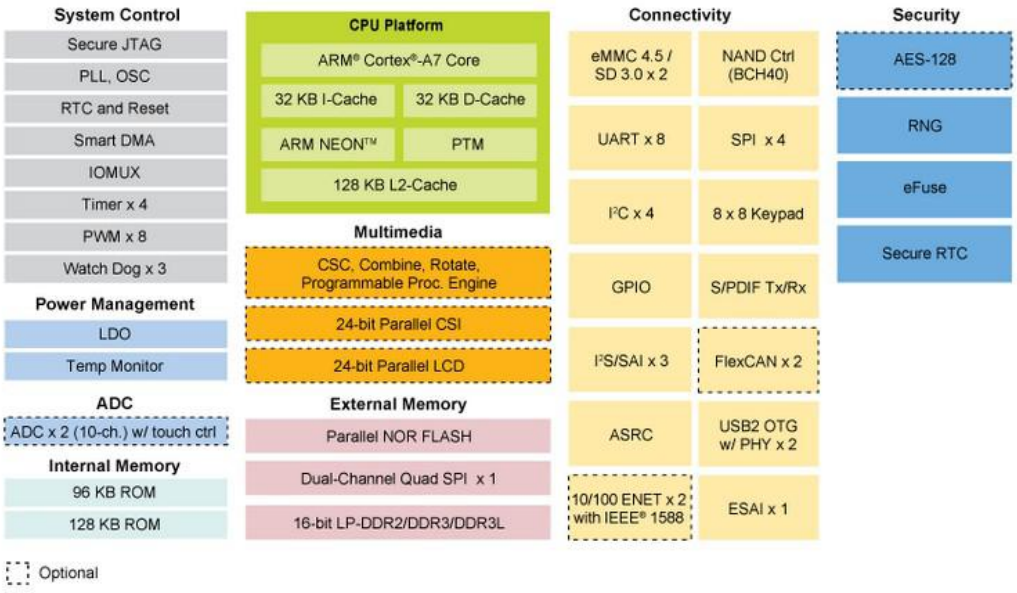
Power State	Test Environment	Supply Voltage	Current	Power Consumption
PWRUP	System startup with no applications running	5.0V	0.085A	0.427W
PWRUP	Software heavy load test	5.0V	0.203A	1.101W
SLEEP	Freezemode sleep state	5.0V	0.045A	0.225W
SLEEP	Standbymode sleep state	5.0V	0.013A	0.055W
SLEEP	Memmode sleep state	5.0V	0.005A	0.0twenty fourW
PWRDN	Poweroffstate power consumption	5.0V	0.0003A	0.001W

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6. Core Board Hardware Design

6.1.Processor

The ECK20-6Y28C series core board uses the MCIMX6Y2CVM08AB processor from the i.MX6ULL series. The i.MX6ULL series is a low-power, high-performance, and cost-effective application processor based on the ARM Cortex-A7 core. Compared to the i.MX6UL series, the i.MX6ULL series has streamlined some encryption functions while maintaining high cost-effectiveness and ultra-low power consumption characteristics. It can be considered an optimized version of the i.MX6UL series for cost efficiency. The functional block diagram of the i.MX6ULL series is shown below.



i.MX6ULLSeries Functional Block Diagram

- MCIMX6Y2CVM08AB processor main features are as follows:
- ARM® Cortex®-A7core, operating frequency up to 792MHz;
- 16-bit LP-DDR2, DDR3/DDR3L memory interface;
- 8-bit parallel NAND FLASH interface;
- 16/8-bit parallel NOR FLASH interface;
- Parallel LCD display, resolution up to WXGA (1366x768);
- twenty four/16/10/8-bit parallel camera sensor interface;
- Two CAN interfaces;

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- One Quad SPI NOR FLASH interface;
- TwoUSB 2.0 OTGinterface;
- Two10/100Ethernet,supportIEEE 1588protocol;
- TwoMMC 4.5/SD 3.0/SDIOports;
- Audio interface including three I2S/SAI, S/PDIF Tx/Rx;
- Eight UART interfaces;
- Two ADC modules supporting up to 10 input channels.

6.2.Memory

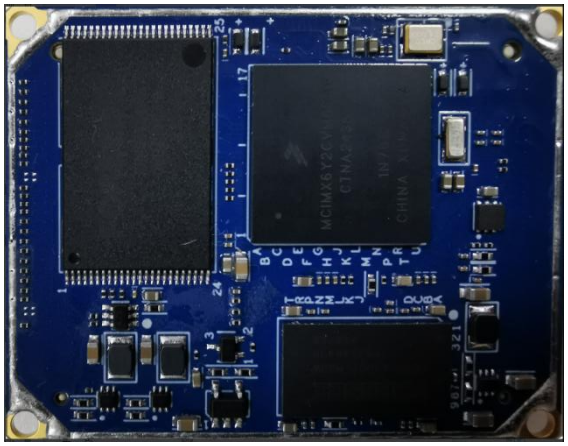
The ECK20-6Y28C series core board is equipped with one DDR3L SDRAM memory chip on-board. The design supports a 16-bit memory data bus width with two capacity options: 256MB and 512MB.

6.3.Clock

The ECK20-6Y28C series core board provides one 32.768KHz crystal (unbuffered) oscillator circuit and one 24 MHz crystal (unbuffered) oscillator circuit on-board as the clock source for the processor system.

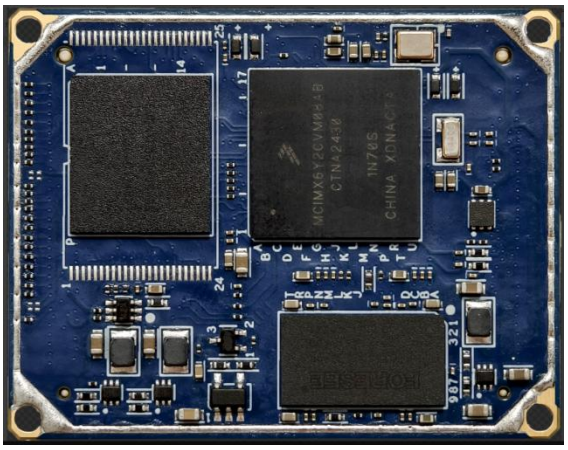
6.4.Storage

The ECK20-6Y28C series core board has two storage solutions on-board: one is a parallel FLASH st orage solution using SLC NAND FLASH chips, which have the advantages of low cost and high reliabili ty; the other is an eMMC storage solution using eMMC chips, which offer large storage capacity, low un it storage cost, and ease of use. Since these two storage solutions share the same I/O resources, only one storage solution is supported by each model of the core board product. Users need to select the correspo nding model of the core board product according to the specific project requirements for storage.



NAND FLASH version without shielding cover

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eMMC version without shielding cover

eMMC memory is connected to the USDHC2 functional interface, sharing I/O pins with the NAND i nterface. The eMMC chip and processor interface signal levels only support 3.3V levels and do not suppo rt 1.8V levels, so the USDHC2 interface supports a maximum clock frequency of 50MHz. Software shoul d pay attention to the parameter configuration of USDHC2.

6.4.1. Multiplexed I/O allocation

Storage I/O Allocation Table

MPU I/O Pins	NAND Features	eMMC Features
D7	NAND_DATA0	eMMC_DATA0
B7	NAND_DATA1	eMMC_DATA1
A7	NAND_DATA2	eMMC_DATA2
D6	NAND_DATA3	eMMC_DATA3
C6	NAND_DATA4	eMMC_DATA4
B6	NAND_DATA5	eMMC_DATA5
A6	NAND_DATA6	eMMC_DATA6
A5	NAND_DATA7	eMMC_DATA7
A3	NAND_nREADY	
D8	NAND_nRE	eMMC_CLK
C5	NAND_nCE0	
B5	NAND_nCE1	
A4	NAND_CLE	
B4	NAND_ALE	eMMC_RST#
C8	NAND_nWE	eMMC_CMD
D5	NAND_nWP	
E6	NAND_DQS	

6.5.Watchdog

The ECK20-6Y28C series core board internally supports one watchdog function. When a watchdog ti

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meout occurs, it generates a low-level pulse (approximately 1.6 milliseconds wide) on the RESETN signal pin, causing a system reset.

6.6.Power Supply

The ECK20-6Y28C series core board adopts a separated power supply scheme, strictly designed according to the voltage, power, and timing requirements specified in the i.MX6ULL manual. The power supply solution of the ECK20-6Y28C series core board supports automatic adjustment of the SD1 I/O interface voltage, automatically selecting either 3.3V or 1.8VI/O supply voltage based on the SDIO speed requirements. ECK20-6Y28C series core board does not support dynamic adjustment of the CPU nuclear power supply voltage.

6.6.1. Power Domain

The ECK20-6Y28C series core board uses a single-channel DC +5V power supply. Only one power input, VIN_5V, needs to be provided externally; other power supplies are generated internally by the core board, requiring no additional power sources. The power domains associated with the power rails and their typical voltages are shown in the table below. Among these, the SNVS power domain is powered up first, followed by the NVCC power domain, while the VBUS power domain can be powered up at any time. When using the core board, attention should be paid to the power domains to which signals belong and the power-up sequence of each power domain.

Power Domain Table

Power supply name	Power Description	Typical voltage	Power Domain
VIN_5V	Core board 5V main power input	5.0V	SNVS
SNVS_IN	SNVS Power Rail	3.3V	SNVS
NVCC_3V3/CSI	I/O interface power rail	3.3V	NVCC
NVCC_SD	SDIO interface power rail	1.8V/3.3V	NVCC
VBUS_5V	USB interface 5V power rail	5.0V	VBUS
VBUS_3V	USB interface 3V power rail	3.3V	VBUS

6.6.2. Multiplexed I/O allocation

Power I/O Assignment Table

MPU I/O Pins	Network Name	Function
T9	SNVS_PMIC_ON_REQ	Processor power management output
M17	GPIO1_IO05	SD1 I/O voltage adjustment

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7. Baseboard hardware design

7.1.Power interface

For embedded product design, the design of the power system is critical. It not only requires consideration of the basic electrical parameters of the power supply itself but also involves factors such as power stability design and timing design. The ECK20-6Y28C series core board adopts a single power supply solution and provides power sequencing management signals to simplify the power design on the user's base board as much as possible.

7.1.1. Power Input

The ECK20-6Y28C series core board uses a single-channel DC +5V power supply, corresponding to pins J2-1 and J2-2 of the BTB connector. The power supply voltage range is 5.0V±10%. The typical power consumption of the ECK20-6Y28C series core board is around 1W. When designing the power supply for the core board on the baseboard, consider the increased power consumption when I/O and more functions are running simultaneously, as well as the increased power consumption at high temperatures. Therefore, it is recommended to design the core board's power supply current to be approximately 0.5A.

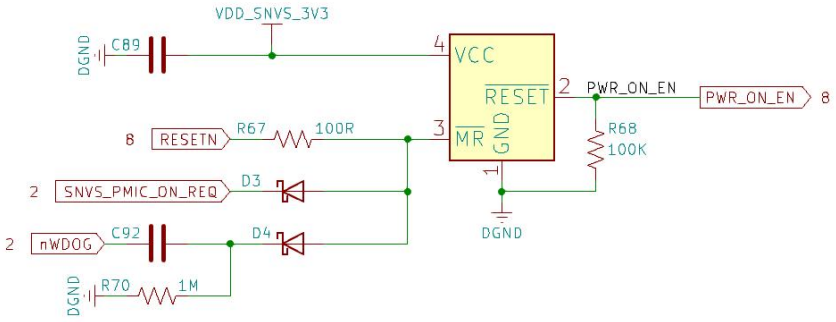
If using a DC-DC power supply for the core board, the power margin in the power design should not be too large. If the designed power is too high, many power supplies operate in discontinuous PWM mode to ensure conversion efficiency, resulting in significantly increased output ripple, which is detrimental to the stability of digital signal systems. If using an LDO to power the core board, consider the power loss and operating temperature rise of the LDO itself during design to prevent the LDO from overheating or burning out when working in high-temperature environments or environments with poor heat dissipation.

7.1.2. Power Control

The ECK20-6Y28C series core board outputs a power management control signal, PWR_ON_EN. When this signal is active (high level), it indicates that the power supply for the NVCC power domain is enabled. The user's baseboard can use this signal to control when the related power domains on the baseboard begin to operate. The PWR_ON_EN signal becomes inactive (low level) when the manual reset is active (low level), or when the SNVS_PMIC_ON_REQ signal is inactive (low level), or when the watchdog

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timeout signal is active (low level). The circuit for generating the PWR_ON_EN signal is shown in the fi gure below.



PWR_ON_EN generation circuit

Note: Since a reset (this product is designed with a cold reset, which will cause some power supplie s to turn off) and power switch operations can lead to partial or complete power loss in the power syste m, some circuits, due to the presence of capacitors or circuit design requirements, cannot rapidly drop to 0V and require some time to discharge. If multiple resets or power switches are performed within a short period, it may result in abnormal power-on states for some I/O interfaces or chips, leading to failure to start up or even more severe faults. It is recommended that the interval time between resets or power on/ off cycles be greater than 2-3 seconds.

When designing the power supply for the baseboard, attention should be paid to the characteristics of I/O sign als such as their power rails, operating levels, and power-up sequencing. The pin definition table in this manual pr ovides detailed descriptions of the voltage levels and power rails for the core board's I/O interfaces. When connecti ng the core board's I/O signals to the baseboard chips, it is essential to ensure that the chip pins and the core boa rd's I/O are at the same voltage level, on the same power rail, or within the same power-up timing domain. Conne cting two I/O signals with incorrect voltage levels or power-up timing domains can lead to communication failures, reduce the lifespan of I/O interfaces, or damage the I/O interfaces. For example, some development board products on the market connect a 3.3VI/O signal from the core board to a CAN interface chip powered by a 5V supply (t he core board's power supply) when designing CAN interfaces. This design has two issues: one is that the 3.3VI/O signal from the core board may not tolerate the 5V signal from the CAN interface chip, leading to unstable com munication or I/O damage; the other is that the 5V power supply comes up before the 3.3VI/O, meaning they are not in the same timing domain. When the 5V power is on but the 3.3V is not yet powered up, the 5V power can enter the 3.3V power network through the I/O connections, causing the 3.3V power network voltage to rise, potent ially resulting in abnormal startup of some components or damage to the I/O interfaces.

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7.1.3. Backup Power

A diode is connected in series between the VBAT backup battery interface and the processor's VDD_SNVS_IN pin. If an external battery is used to power VBAT, there is no need to add another diode on the baseboard.

Since the power consumption of the SNVS power domain is relatively high after the processor loses power, using an external RTC battery for power supply would result in a shortened lifespan of the RTC battery. NXP recommends implementing RTC functionality using an external RTC circuit. If an external RTC circuit is used, the VBAT pin can be left floating.

7.1.4. Pin Definition

Power pin definition table

Pinout	Network Name	Level/Power Rail	type	illustrate
29	VIN_5V	5V/VIN_5V	PWR	
30	VIN_5V	5V/VIN_5V	PWR	
78	VBAT	3.3V/SNVS_IN	PWR	Series diode
79	PWR_ON_EN	3.3V/SNVS_IN	O	

7.2.Launch Configuration

During the startup of the i.MX6ULL processor, it first executes the program stored in the internal Boot ROM. The Boot ROM determines the boot mode and boot device based on the status of the BOOT_MODE register, eFUSEs, configuration pins, etc.

The value of the BOOT_MODE register depends on the levels of the BOOT_MODE0 and BOOT_MODE1 pins during the initial power-up phase, which determines the boot mode. The specific correspondence is shown in the table below:：

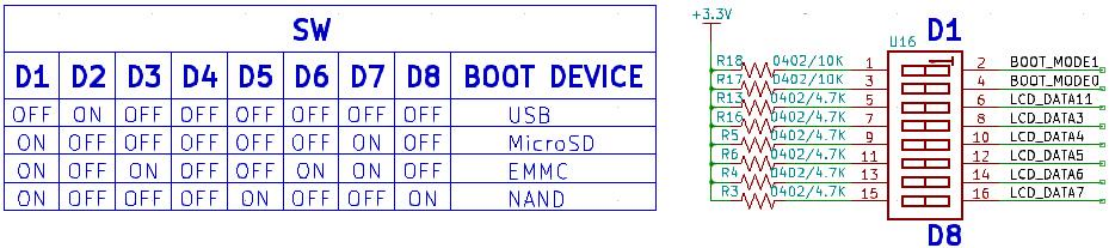
BOOT_MODE boot mode configuration table

BOOT_MODE[1:0]	Startup Mode	Startup Mode Description
00	Boot From Fuses	Read the startup information from the internal fuses. This method is recommended for mass production.
01	Serial Downloader	Supports downloading programs to Flash from USB_OTG1 port. It should be noted that in this mode, UART1 and UART2 have higher priority than USB_OTG. If UART1 and UART2 serial ports detect data in this mode, the downloader cannot burn the program from USB and the computer cannot detect the device.
10	Internal Boot	Read the startup configuration from the Boot Mode pin. This is recommended for development mode and can also be used for mass production.

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11	Reserved	Retention mode.

Typically, the BOOT mode is set to internal Boot mode. In this mode, upon power-on reset, the CPU reads the logic levels on the LCD_DATA0-DATA23 pins to determine the boot device. For the ECK20-6Y28C series core board, the LCD_DATA0-DATA23 pins are internally pulled down. Therefore, when designing the baseboard, only individual pins need to be configured for specific boot device selection. The reference circuit for boot device selection on the baseboard is shown in the figure below:



SW								
D1	D2	D3	D4	D5	D6	D7	D8	BOOT DEVICE
OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	USB
ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	MicroSD
ON	OFF	ON	OFF	OFF	ON	ON	OFF	EMMC
ON	OFF	OFF	OFF	ON	OFF	OFF	ON	NAND

BOOT configuration circuit

The LCD_DATA0-DATA7 pins correspond to the BOOT configuration functions BOOT_CFG1[0]-CFG1[7]. The LCD_DATA8-DATA15 pins correspond to the BOOT configuration functions BOOT_CFG2[0]-CFG2[7]. The BOOT_CFG configuration functions are illustrated in the figure below.

	0/1	0/1	0/1	1	0	0	0	0
TYPE	BOOT_CFG1[7]	BOOT_CFG1[6]	BOOT_CFG1[5]	BOOT_CFG1[4]	BOOT_CFG1[3]	BOOT_CFG1[2]	BOOT_CFG1[1]	BOOT_CFG1[0]
QSPI	0	0	0	1	Reserved	DDRSMP: "000" : Default "001-111"		
WEIM	0	0	0	0	Memory Type: 0 - NOR Flash 1 - OneNAND	Reserved	Reserved	Reserved
Serial-ROM	0	0	1	1	Reserved	Reserved	Reserved	Reserved
SD/eSD	0	1	0	Fast Boot: 0 - Regular 1 - Fast Boot	SD/SDXC Speed 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104		SD Power Cycle Enable '0' - No power cycle '1' - Enabled via USDHC_RST pad (uSDHC3 & 4 only)	SD Loopback Clock Source Sel(for SDR50 and SDR104 only) '0' - through SD pad '1' - direct
MMC/eMMC	0	1	1	Fast Boot: 0 - Regular 1 - Fast Boot	SD/MMC Speed 0 - High 1- Normal	Fast Boot Acknowledge Disable: 0 - Boot Ack Enabled 1 - Boot Ack Disabled	SD Power Cycle Enable '0' - No power cycle '1' - Enabled via USDHC_RST pad (uSDHC3 & 4 only)	SD Loopback Clock Source Sel(for SDR50 and SDR104 only) '0' - through SD pad '1' - direct
NAND	1	BT_TOGGLEMODE	Pages in Block: 00 - 128 01 - 64 10 - 32 11 - 256		Nand Number Of Devices: 00 - 1 01 - 2 10 - 4 11 - Reserved		Nand_Row_address_bytes: 00 - 3 01 - 2 10 - 4 11 - 5	

BOOT_CFG1 Configuration Diagram

	0	0	0	0	1	0	0	0
TYPE	BOOT_CFG2[7]	BOOT_CFG2[6]	BOOT_CFG2[5]	BOOT_CFG2[4]	BOOT_CFG2[3]	BOOT_CFG2[2]	BOOT_CFG2[1]	BOOT_CFG2[0]
QSPI	Reserved	HSPHS: Half Speed Phase Selection 0 : select sampling at non-inverted clock 1: select sampling at inverted clock	HSDLY: Half Speed Delay selection 0 : one clock delay 1: two clock delay	FSPHS: Full Speed Phase Selection 0 : select sampling at non-inverted clock 1: select sampling at inverted clock	FSDLY: Full Speed Delay selection 0: one clock delay 1: two clock delay	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
WEIM	Muxing Scheme: 00 - A/D16 01 - A+DH 10 - A+DL 11- Reserved		OneNand Page Size: 00 - 1KB 01 - 2KB 10 - 4KB 11 - Reserved		Reserved	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
Serial-ROM	Reserved	Reserved	Reserved	Reserved	Reserved	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 250 / 200 MHz	Reserved	Reserved
SD/eSD	SD Calibration Step '00' - 1 TBD		Bus Width: 0 - 1-bit 1 - 4-bit	Port Select: 00 - eSDMC1 01 - eSDHC2 10 - Reserved 11 - Reserved		Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SD1 VOLTAGE SELECTION 0 3.3V 1 - 1.8V	Reserved
MMC/eMMC	Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4) Else - reserved.			Port Select: 00 - eSDHC1 01 - eSDHC2 10 - Reserved 11 - Reserved		Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SD1 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved
NAND	Toggle Mode 33MHz Preamble Delay, Read Latency: '000' - 16 GPMICLK cycles. '001' - 1 GPMICLK cycles. '010' - 2 GPMICLK cycles. '011' - 3 GPMICLK cycles. '100' - 4 GPMICLK cycles. '101' - 5 GPMICLK cycles. '110' - 6 GPMICLK cycles. '111' - 7 GPMICLK cycles.			BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8		Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reset Time '0' - 12ms '1' - 22ms (LBA Nand)	Reserved

BOOT_CFG2 Configuration Diagram

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	0	0	0	0	0	0	0	0
TYPE	BOOT_CFG4[7]	BOOT_CFG4[6]	BOOT_CFG4[5]	BOOT_CFG4[4]	BOOT_CFG4[3]	BOOT_CFG4[2]	BOOT_CFG4[1]	BOOT_CFG4[0]
0x450	Infinit-Loop (Debug USE only) 0 - Disable 1- Enable	EEPROM Recovery Enable '0' - Disabled '1' - Enabled	CS select (SPI only): 00 - CS#0 (default) 01 - CS#1 10 - CS#2 11 - CS#3		SPI Addressing: 0 - 2-bytes (16-bit) 1 - 3-bytes (24-bit)		Port Select: 000 - eCSPI1 001 - eCSPI2 010 - eCSPI3 011 - eCSPI4 100 - Reserved 101 - Reserved 110 - Reserved 111 - Reserved	
0x460	L2_HW_INVALIDATE _DISABLE	Reserved	FORCE_COLD_BOOT (Reflected in SBMR2)	BT_FUSE_SEL	DIR_BT_DIS	Reserved	SEC_CONFIG[1]	Reserved
0x460	Reserved (DDR3 config options)							
0x460	JTAG_SMODE[1:0]	WDOG_ENABLE '0' - Disabled '1' - Enabled	SJC_DISABLE	Reserved	Reserved	Reserved	Reserved	Reserved
0x460	Reserved	Reserved	Reserved	TZASC_ENABLE	JTAG_HEO	KTE	Reserved	DLL_ENABLE 0 - Disable DLL for SD/eMMC 1 - Enable DLL for SD/Emmc
0x470	DLL Override: 0 - DLL Slave Mode for SD/eMMC 1 - DLL Override Mode for SD/eMMC	Reserved	SD2 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved	Disable SDMMC Manufacture mode 0 - Enable 1 - Disable	L1 I-Cache DISABLE	BT MMU _DISABLE	Override Pad Settings (using PAD_SETTINGS value)
0x470	Reserved for unexpected requirements	eMMC 4.4 - RESET TO PRE-IDLE STATE	Override HYS bit for SD/MMC pads	USDHC_PAD_PULL_DOWN 0 - no action 1 - pull down	ENABLE_EMMC_22K_PULLUP 0 - 47K pullup 1 - 22K pullup	ADD_DS_SET_GPR1_16 0 - Set 1 - Don't set	USDHC_IOMUX_SION_BIT_ENABLE 0 - Disable 1 - Enable	USDHC IOMUX SRE Enable 0 - Disable 1 - Enable
0x470	USDHC_CMD_OE_PRE_EN (SD/MMC debug)	LPB_BOOT (Core / DDR- Bus) '00' - LPB Disable '01' - 1 GPIO (def freq) '10' - Div by2 '11' - Div by 4		BT_LPB_POLARITY (GPIO polarity)	POWER_MNG_CFG (LDO's DCDC's) (Reserved - NOT USED)			
0x470	Override NAND Pad Settings (using PAD_SETTINGS value)	MMC_DLL_DLY[6:0] Delay target for SD/eMMC DLL, it is applied to slave mode target delay or override mode target delay depends on DLL Override fuse bit value.						

BOOT_CFG4 configuration diagram

7.2.1. Pin Definition

Startup configuration pin definition table

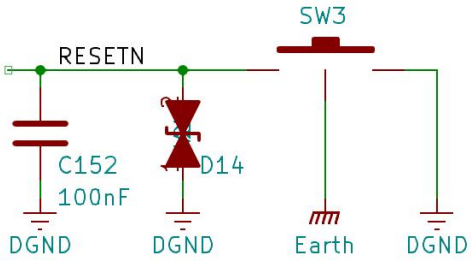
Pinout	Network Name	MPU	Level/Power Rail	type	Trace length	illustrate
twenty three	BOOT_MODE1	U10	3.3V/SNVS_IN	I	654.31	Pull down 100K on chip
twenty four	BOOT_MODE0	T10	3.3V/SNVS_IN	I	705.37	Pull down 100K on chip
107	LCD_DATA07	D11	3.3V/NVCC_3V3	I/O	1117.90	Pull down 47K resistor
108	LCD_DATA06	A10	3.3V/NVCC_3V3	I/O	1118.25	Pull down 47K resistor
109	LCD_DATA05	B10	3.3V/NVCC_3V3	I/O	1118.87	Pull down 47K resistor
110	LCD_DATA04	C10	3.3V/NVCC_3V3	I/O	1117.53	Pull down 47K resistor
111	LCD_DATA03	D10	3.3V/NVCC_3V3	I/O	1121.35	Pull down 47K resistor
103	LCD_DATA11	D12	3.3V/NVCC_3V3	I/O	1116.43	Pull down 47K resistor

7.3.Reset and power buttons

The PWRBTN and RESETN signals brought out by the ECK20-6Y28C series core board can be con nected to external buttons to implement reset and power control functions for the processor.

The RESETN signal has a debounce circuit and pull-up resistor designed into the core board. The P WRBTN signal is connected internally within the core board to the processor chip's ONOFF pin, which a lso includes an internal pull-up resistor. Since both of these signals have internal pull-up resistors on the core board, there is no need to add additional pull-up resistors on the baseboard. These signals can be dir ectly connected to buttons or driven through an open-drain (OD) gate. The reference Schematic for the bu tton connections is shown in the figure below.

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Button reference schematic

Note: Do not arbitrarily pull up the reset and power button signals through resistors. If the pull-up power rail is incorrect, it can lead to unintended signal inputs to the button signal interface when the system is in standby or powered off. For example, some baseboard designs pull the PWRBTN signal up to the NVCC_3V3 power supply. When the system is powered off, the NVCC_3V3 power supply is also turned off, causing the voltage on NVCC_3V3 to drop to 0V. At this point, pulling up the PWRBTN signal to NVCC_3V3 effectively pulls it down to ground, which is equivalent to pressing the PWRBTN button, causing the system to restart. This can ultimately result in the system being unable to shut down properly via software.

7.3.1. Pin Definition

Button pin definition table

Pinout	Network Name	MPU	Level/Power Rail	type	illustrate
27	PWRBTN	R8	3.3V/SNVS_IN	I	Pull-up 100K on chip
80	RESETN		3.3V/SNVS_IN	I	Pull-up 50K on chip

7.4.Display Interface

The ECK20-6Y28C series core board provides a parallel LCD display interface with a maximum resolution support of 1366x768 at 60fps and a maximum pixel clock of up to 85MHz. It supports 24/18/16/8-bit parallel display configurations. Customers can configure the display resolution and data format according to their needs. In LCD and TFT screen applications, GPIO can be used to control screen power and backlight power. PWM output can be utilized to control the backlight brightness. Additionally, I2C and GPIO external interrupts can be used to connect a touchscreen.

For those looking for compatible modules, Yibite's LCD touchscreen modules are recommended. More information on related modules can be found on their official website: https://www.ebyte.com/.

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7.4.1. Interface Definition

Display interface definition table

Pinout	Network Name	MPU	Level/Power Rail	type	Trace length	illustrate
15	LCD_ENABLE	B8	3.3V/NVCC_3V3	I/O	1114.93	
75	LCD_CLK	A8	3.3V/NVCC_3V3	I/O	1119.18	Connect a 10 ohm resistor in series
76	LCD_HSYNC	D9	3.3V/NVCC_3V3	I/O	1117.66	
77	LCD_VSYNC	C9	3.3V/NVCC_3V3	I/O	1121.21	
91	LCD_DATA23	B16	3.3V/NVCC_3V3	I/O	1115.26	Pull down 47K resistor
92	LCD_DATA22	A14	3.3V/NVCC_3V3	I/O	1121.90	Pull down 47K resistor
93	LCD_DATA21	B14	3.3V/NVCC_3V3	I/O	1121.71	Pull down 47K resistor
94	LCD_DATA20	C14	3.3V/NVCC_3V3	I/O	1123.00	Pull down 47K resistor
95	LCD_DATA19	D14	3.3V/NVCC_3V3	I/O	1112.36	Pull down 47K resistor
96	LCD_DATA18	A13	3.3V/NVCC_3V3	I/O	1112.83	Pull down 47K resistor
97	LCD_DATA17	B13	3.3V/NVCC_3V3	I/O	1113.94	Pull down 47K resistor
98	LCD_DATA16	C13	3.3V/NVCC_3V3	I/O	1115.45	Pull down 47K resistor
99	LCD_DATA15	D13	3.3V/NVCC_3V3	I/O	1119.49	Pull down 47K resistor
100	LCD_DATA14	A12	3.3V/NVCC_3V3	I/O	1116.77	Pull down 47K resistor
101	LCD_DATA13	B12	3.3V/NVCC_3V3	I/O	1111.69	Pull down 47K resistor
102	LCD_DATA12	C12	3.3V/NVCC_3V3	I/O	1111.73	Pull down 47K resistor
103	LCD_DATA11	D12	3.3V/NVCC_3V3	I/O	1116.43	Pull down 47K resistor
104	LCD_DATA10	E12	3.3V/NVCC_3V3	I/O	1118.52	Pull down 47K resistor
105	LCD_DATA09	A11	3.3V/NVCC_3V3	I/O	1120.64	Pull down 47K resistor
106	LCD_DATA08	B11	3.3V/NVCC_3V3	I/O	1116.88	Pull down 47K resistor
107	LCD_DATA07	D11	3.3V/NVCC_3V3	I/O	1117.90	Pull down 47K resistor
108	LCD_DATA06	A10	3.3V/NVCC_3V3	I/O	1118.25	Pull down 47K resistor
109	LCD_DATA05	B10	3.3V/NVCC_3V3	I/O	1118.87	Pull down 47K resistor
110	LCD_DATA04	C10	3.3V/NVCC_3V3	I/O	1117.53	Pull down 47K resistor
111	LCD_DATA03	D10	3.3V/NVCC_3V3	I/O	1121.35	Pull down 47K resistor
112	LCD_DATA02	E10	3.3V/NVCC_3V3	I/O	1120.91	Pull down 47K resistor
113	LCD_DATA01	A9	3.3V/NVCC_3V3	I/O	1120.26	Pull down 47K resistor
114	LCD_DATA00	B9	3.3V/NVCC_3V3	I/O	1126.87	Pull down 47K resistor

7.4.2. LAYOUT SUGGESTIONS

- If the baseboard design includes series termination resistors for the LCD signals, it is recommended to place these resistors close to the core board's BTB connector
- The LCD signals are matched in length within the core board, and the trace lengths inside the cor e board can be found in the pin definition table;
- The LCD signals within the core board are controlled with a single-ended impedance of 50Ω±10%.

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It is recommended that the impedance control on the baseboard also maintain this consistency;

- It is recommended that the baseboard LCD signal traces be length-matched, with an allowable error of ±100mil. The spacing between signal lines should be at least 2W (two times the width of the trace).

7.5.Camera interface

The ECK20-6Y28C series core board's CSI interface supports 8-bit or 24-bit YCbCr, YUV, and RGB format data input, as well as 8-bit, 10-bit, or 16-bit Bayer format data input, with a maximum pixel clock of 133.3MHz. The camera interface consumes a large number of I/O pins, which limits the availability of other multiplexed functions. Therefore, it is recommended to use a USB interface camera to implement camera functionality..

7.5.1. Interface Definition

Camera interface definition table

Pinout	Network Name	MPU	Level/Power Rail	type	Trace length	illustrate
119	CSI_MCLK	F5	3.3V/NVCC_CSI	I/O	1350.47	CSI Master Clock
116	CSI_PIXCLK	E5	3.3V/NVCC_CSI	I/O	1348.42	CSI Pixel Clock
1	CSI_VSYNC	F2	3.3V/NVCC_CSI	I/O	1348.21	CSI vertical synchronization signal
120	CSI_HSYNC	F3	3.3V/NVCC_CSI	I/O	1346.67	CSI horizontal synchronization signal
5	CSI_DATA00	E4	3.3V/NVCC_CSI	I/O	1354.05	CSI data bits
4	CSI_DATA01	E3	3.3V/NVCC_CSI	I/O	1356.27	CSI data bits
118	CSI_DATA02	E2	3.3V/NVCC_CSI	I/O	1349.88	CSI data bits
2	CSI_DATA03	E1	3.3V/NVCC_CSI	I/O	1353.75	CSI data bits
6	CSI_DATA04	D4	3.3V/NVCC_CSI	I/O	1353.49	CSI data bits
115	CSI_DATA05	D3	3.3V/NVCC_CSI	I/O	1351.41	CSI data bits
117	CSI_DATA06	D2	3.3V/NVCC_CSI	I/O	1344.27	CSI data bits
3	CSI_DATA07	D1	3.3V/NVCC_CSI	I/O	1347.28	CSI data bits

7.6.uSDHC card interface

The ECK20-6Y28C series core board is equipped with two uSDHC interfaces. The uSDHC interface (Ultra Secured Digital Host Controller) is a proprietary secure digital host controller by NXP, providing a secure communication method between the processor and external SD/SDIO/MMC interface devices.

- The uSDHC 1 function of the processor is externally available and can be used for SD card bootin

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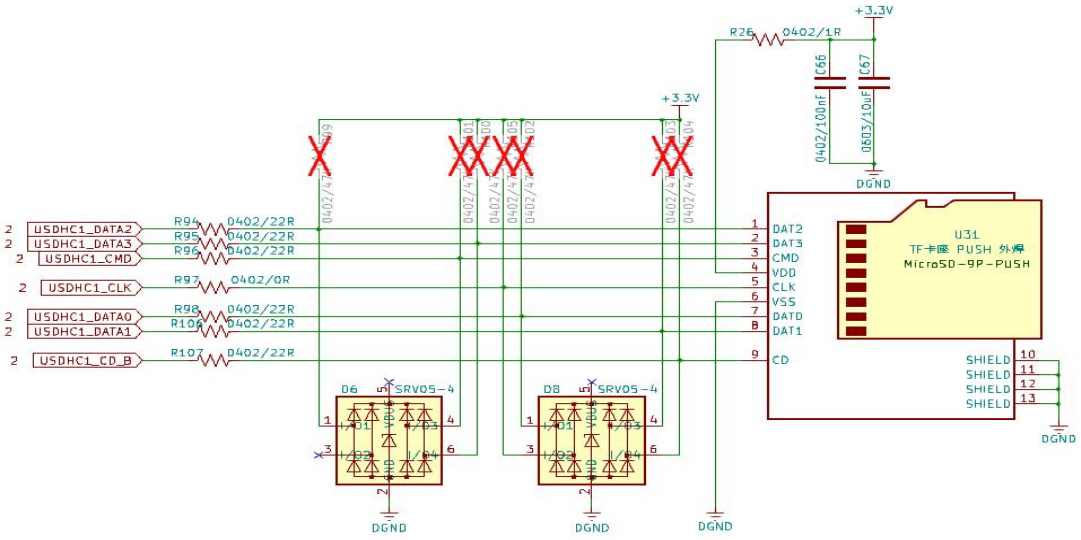
g or SDIO communication.

- The uSDHC 2 function is only externally available through I/O multiplexing on core boards that use a NAND FLASH storage solution. On core boards using eMMC storage, the uSDHC 2 function is occupied and cannot be externally accessed.

The uSDHC 1 interface on the ECK20-6Y28C series core board supports automatic I/O power adjustment. The uSDHC 1 interface I/O voltage level is adjusted via GPIO1_IO05 and supports both 3.3V and 1.8V levels. At the 1.8V level, the uSDHC 1 interface can support a maximum clock frequency of 150MHz.

The processor's I/O can be configured with internal pull-up resistors, which meet the pull-up requirements for SD card interface expansion, eliminating the need for external pull-up resistors in user designs. Additionally, the core board has already included a 10-ohm series matching resistor on the uSDHC clock signal, so there is no need for external series resistors in user designs.

For expanding a Micro SD card through the uSDHC interface, refer to the following schematic design.



SD card reference circuit diagram

7.6.1. Pin Definition

Pinout	Network Name	MPU	Level/Power Rail	type	Trace length	illustrate
7	SD1_CLK	C1	3.3V/1.8V/NVCC_SD	I/O	1155.73	Connect a 10 ohm resistor in series
8	SD1_CMD	C2	3.3V/1.8V/NVCC_SD	I/O	1149.57	Pull-up 10K resistor
9	SD1_DATA2	B1	3.3V/1.8V/NVCC_SD	I/O	1151.28	

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10	SD1_DATA3	A2	3.3V/1.8V/NVCC_SD	I/O	1152.75	
11	SD1_DATA1	B2	3.3V/1.8V/NVCC_SD	I/O	1149.15	
12	SD1_DATA0	B3	3.3V/1.8V/NVCC_SD	I/O	1150.61	Pull-up 10K resistor
14	GPIO1_IO05	M17	3.3V/NVCC_3V3	I/O	2700.36	SD1_VSELECT
47	UART1_RTS_B	J14	3.3V/NVCC_3V3	I/O	1835.40	SD1_CD

uSDHC interface signal pin definition

7.6.2. LAYOUT SUGGESTIONS

- ❖The uSDHC signals within the core board are controlled with a single-ended impedance of 50Ω±10%. It is recommended that the impedance control on the baseboard also maintain this consistency;
- ❖The uSDHC signals are matched in length within the core board, and the trace lengths inside the core board can be found in the pin definition table;
- ❖It is recommended that the baseboard uSDHC signals (excluding the insertion detection signal) be length-matched with an allowable error of ±100mil. The spacing between signal lines should be at least 2W.
- ❖The distance between the clock signal and other signals should follow the 3W rule.

7.7.USB interface

The ECK20-6Y28C series core board supports two USB 2.0 OTG interfaces. If users utilize the USB OTG functionality, it is recommended to use a MICRO USB interface for USB, as this interface has five lines including the USB_ID signal (which can be implemented through GPIO functionality), used to identify HOST and DEVICE, thereby enabling OTG functionality. If users do not use the USB OTG function and only use it as a USB HOST, then either a 4-line or 5-line USB interface can be selected.

USB_OTGx_VBUS is the I/O power supply for the processor's USB interface. To use the USB function, these pins must be used to supply power to the USB interface I/O, with a supply voltage of 5.0V±10% and a maximum supply current of 50mA.

7.7.1. Pin Definition

USBInterface signal pin definition

Pinout	Network Name	MPU	Level/Power Rail	type	Trace length	illustrate
32	USB_OTG2_VBUS	U12	5V/VBUS_5V	PWR		VBUS power input

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33	USB_OTG1_VBUS	T12	5V/VBUS_5V	PWR		VBUS power input
34	USB_OTG2_DP	U13	3.3V/VBUS_3V	I/O	1243.75	
35	USB_OTG2_DN	T13	3.3V/VBUS_3V	I/O	1243.24	
36	USB_OTG1_DP	U15	3.3V/VBUS_3V	I/O	1208.30	
37	USB_OTG1_DN	T15	3.3V/VBUS_3V	I/O	1209.28	
38	USB_OTG1_CHD_B	U16	3.3V/VBUS_3V	I/O		

7.7.2. LAYOUT SUGGESTIONS

❖Perform equal-length control on USB signal traces;

❖Control the differential impedance of USB signals to 90Ω;

❖Keep USB signal traces as short as possible.

7.8.Ethernet interface

The ECK20-6Y28C series core board supports two channels of 10M/100M Ethernet controllers. The Ethernet controllers support both RMII and MII interfaces. The number of signal lines in an RMII interface is half that of an MII interface, which can simplify the design and save resources; therefore, it is recommended to use the RMII interface for connecting with the Ethernet PHY on the core board.

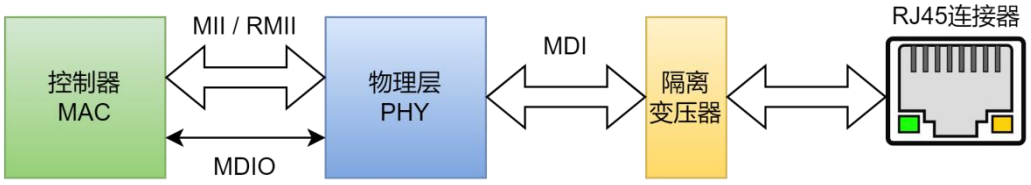
Typically, an RJ45 Ethernet interface consists of the following components:

Ethernet controller MAC (Media Access Control)

Ethernet physical layer interface PHY (Physical Layer)

Ethernet transformer

RJ45 connector



RJ45 Ethernet components

The ECK20-6Y28C series core board does not have an Ethernet PHY circuit designed within it. If users need to utilize Ethernet functionality, they will need to design the PHY interface chip circuit on the baseboard themselves. The design of the PHY interface chip circuit on the baseboard can be referenced from the product drawings of the YiBaiTe i.MX6ULL single-board computer.

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7.8.1. Pin Definition

Ethernet interface signal pin definition

Pinout	Network Name	MPU	Level/Power Rail	type	Trace length	illustrate
60	ENET1_RX_ER	D15	3.3V/NVCC_3V3	I/O	1013.51	RMII Signals
61	ENET1_TX_CLK	F14	3.3V/NVCC_3V3	I/O	1343.51	RMII signal,Connect a 10 ohm resistor in series
62	ENET1_TX_DATA1	E14	3.3V/NVCC_3V3	I/O	1347.76	RMII Signals
63	ENET1_TX_EN	F15	3.3V/NVCC_3V3	I/O	1333.67	RMII Signals
64	ENET1_RX_DATA0	F16	3.3V/NVCC_3V3	I/O	1008.26	RMII Signals
65	ENET1_RX_EN	E16	3.3V/NVCC_3V3	I/O	1006.93	RMII Signals
66	ENET1_RX_DATA1	E17	3.3V/NVCC_3V3	I/O	1018.22	RMII Signals
67	ENET1_TX_DATA0	E15	3.3V/NVCC_3V3	I/O	1342.13	RMII Signals
82	ENET2_RX_DATA0	C17	3.3V/NVCC_3V3	I/O	1513.40	RMII Signals
83	ENET2_RX_DATA1	C16	3.3V/NVCC_3V3	I/O	1504.76	RMII Signals
84	ENET2_TX_DATA0	A15	3.3V/NVCC_3V3	I/O	1069.09	RMII Signals
85	ENET2_TX_DATA1	A16	3.3V/NVCC_3V3	I/O	1066.33	RMII Signals
86	ENET2_RX_ER	D16	3.3V/NVCC_3V3	I/O	1514.31	RMII Signals
87	ENET2_RX_EN	B17	3.3V/NVCC_3V3	I/O	1507.52	RMII Signals
88	ENET2_TX_EN	B15	3.3V/NVCC_3V3	I/O	1070.66	RMII Signals
89	ENET2_TX_CLK	D17	3.3V/NVCC_3V3	I/O	1072.76	RMII signal,Connect a 10 ohm resistor in series
45	GPIO1_IO07	L16	3.3V/NVCC_3V3	I/O	914.25	ENET_MDC
46	GPIO1_IO06	K17	3.3V/NVCC_3V3	I/O	926.46	ENET_MDIO

7.8.2. LAYOUT SUGGESTIONS

- ❖Perform equal-length control on RMII signals with an error tolerance of ±100 mil and maintain a line spacing of at least 2W.;
- ❖Perform equal-length control on network differential signals with an intra-pair error tolerance of ±30 mil and maintain a spacing of at least 3W between adjacent differential pairs;
- ❖Place the Ethernet transformer close to the PHY chip, with a recommended distance of no more than 20mm.;
- ❖Place the decoupling capacitors for the PHY chip's power pins close to the PHY chip.;

7.9.Audio Interface

The ECK20-6Y28C core board supports up to 3 synchronous audio interfaces (SAI), which support full-duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces. In the baseboard circuit design, the SAI interface signals need to be connected to an audio codec chip, through which headphone, m

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icrophone, speaker, and other audio interface functionalities are realized.

In the audio circuit, AUDIO_GND should be isolated from the digital circuit's DGND using 0Ω resistors. Capa citors for power supply pins and filtering capacitors for audio signals should also be connected to AUDIO_GND.

7.10.UART Interface

The ECK20-6Y28C core board supports up to 8 asynchronous serial ports, with a maximum baud rat e of 5.0 Mbps. The core board defaults to using UART 1 as the debugging serial port.

7.11.SPI interface

The ECK20-6Y28C series core board supports up to 4 SPI controllers, with support for both master and slave modes. SPI signals include SPI_CLK, SPI_SS, SPI_MOSI, and SPI_MISO. During design, it is essential to first confirm the relationship between the master and slave devices to determine the direction of the MOSI and MISO signals. Only one device can be connected per SPI bus.

7.12.I2C Interface

The ECK20-6Y28C series core board supports 4 I2C controllers with two clock frequency modes: sta ndard mode at 100 Kbit/s and fast mode at 400 Kbit/s. Multiple devices can be connected on the same I 2C bus. When designing the schematic, consider the following points:

a) Check for address conflicts among devices on the same bus.

b) Ensure that each I2C bus has a pair of pull-up resistors, with recommended values between 2. 2K and 10K ohms, avoiding duplicate additions.

c) Since the core board does not provide pull-up resistors for the I2C bus, users need to add these o n the baseboard.

d) Verify that the I2C interface voltage levels of the devices are 3.3V. If not, level conversion circuit s should be added.

e) Ensure consistency in the power rails for the I2C interfaces. When connecting I2C interfaces from different time domains, consider using bus switch circuits.

f) Avoid connecting too many devices on the same bus, as this could exceed the I2C specification's maximum load capacity limit of 400 pF, potentially affecting signal integrity.

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7.13.CAN interface

The ECK20-6Y28C series core board can provide up to 10 ADC input channels, featuring a single 12-bit ADC converter. The ADC reference voltage VREF uses the internal reference from the processor.

7.14.ADC Interface

The ECK20-6Y28C series core board can provide up to 10 ADC input channels, featuring a single 12-bit ADC converter. The ADC reference voltage VREF uses the internal reference from the processor.

7.15.GPIO interface

The ECK20-6Y28C series core board can provide up to 105 GPIO interfaces, although most of these pins have multiplexed functions. Users can configure the GPIOs flexibly according to their own needs.

7.16.Hardware Design Checklist

- ❖Power Rails: Check for inconsistencies in power rails for I/O interface applications, such as connecting a 1.8V signal to a 3.3V signal. If there is a need to connect signals from different power rails, use level conversion circuits to handle these connections.
- ❖Power-On Sequencing: Verify if there are any issues where signals on the baseboard might power up before those on the core board, or if there is a significant difference in power-up times between the two boards.
- ❖Pull-Up and Pull-Down Resistors: Multiplexed I/O interfaces may have an indeterminate output state before software configuration during power-up. If signals need to maintain a defined level upon power-up, design pull-up or pull-down resistors on the baseboard. Some functional signals also require pull-up or pull-down resistors on the baseboard, such as I2C signals. Pay attention to the design of the pull-up power rail when designing pull-up resistors.
- ❖ESD Protection: Consider appropriate ESD protection designs for external interface signals. The choice of ESD protection solutions should take into account signal speed, communication protocols, and application environment requirements.
- ❖High-Speed Signal Equal Length: For high-speed signals, consider equal-length design on the PCB, including USB, Ethernet, SDIO, display, etc.
- ❖Impedance Control: High-speed signals should consider impedance control on the PCB. The key to impedance control is maintaining continuous impedance. The baseboard should be designed with

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reference to the impedance of the core board signals.

❖These guidelines ensure proper functionality, reliability, and signal integrity across the interconnected boards and their various interfaces.

8. softwareresource

The ECK20-6Y28C series core board runs an operating system based on the Linux 5.10.9 kernel. The development board comes with a cross-compilation toolchain necessary for embedded Linux system development, U-boot source code, Linux kernel and driver module source codes, as well as various development and debugging tools suitable for both Windows and Linux desktop environments.

Operating System:

- Ubuntu 20.04

System Source Code:

- U-boot 2020.04
- Kernel 5.10.9

-Yocto gatesgarth

Development Environment and Tools:

- Flashing Tool: uuu
- Configuration Tool: Config Tools for i.MX V15

These components provide a comprehensive setup for developers to efficiently work on embedded systems projects using the ECK20-6Y28C core board.

8.1.System resources

System Software Resource Table

category	name	describe	Source code
BOOT	u-boot 2020.04	Bootloader	/source/u-boot_2020.04.tar.xz
Kernel	Kernel 5.10.9	Linux Kernel	/source/kernel_5.10.9.tar.xz
Device Driver	MMC	eMMC/TF cardDrivers	drivers/mmc/host/sdhci-esdhc-imx.c
	NAND	MTD Driver	drivers/mtd/nand/raw/gpmi-nand/gpmi-nand.c
	SPI	SPI Driver	drivers/spi/spi-imx.c

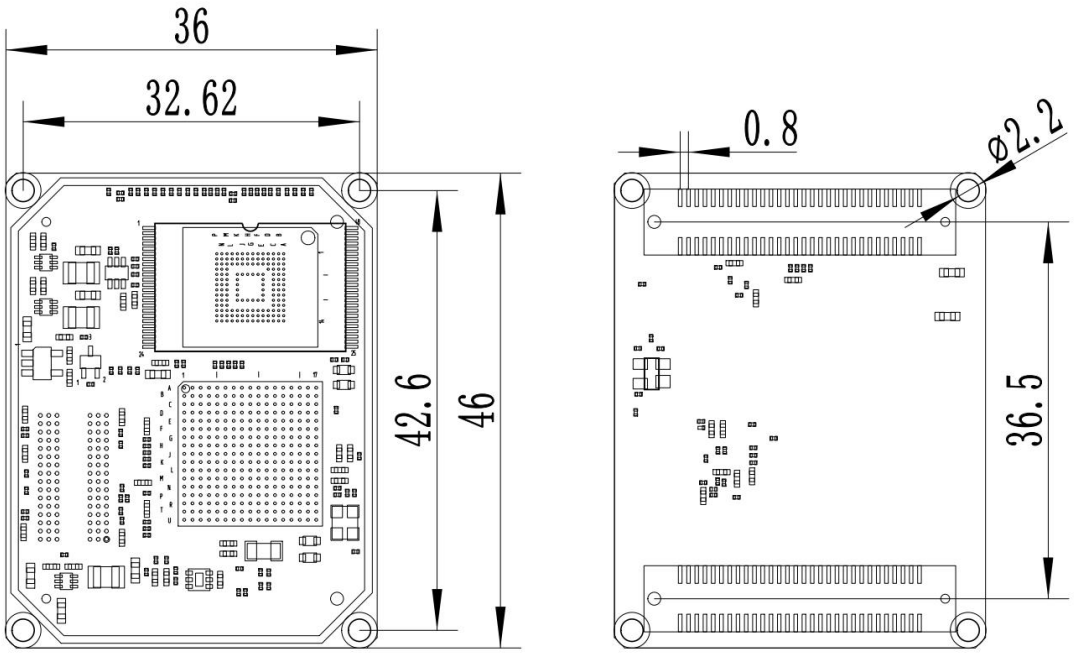
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	I2C	I2CDrivers	drivers/i2c/busses/i2c-imx.c
	USBHost	USB Drivers	drivers/usb/host/ohci-platform.c
	Ethernet	Network Drivers	drivers/net/ethernet/freescale/fec_main.c
	UART	Serial port driver	drivers/tty/serial/imx.c
	Can bus	Can bus driver	drivers/net/can/flexcan.c
	GPIO keys	Key Driver	drivers/input/keyboard/gpio_keys.c
	RTC	RTC Driver	drivers/rtc/rtc-snvs.c
	GPIOLed	Led Driver	drivers/leds/leds-gpio.c
	LCD	LCDIFDrivers	drivers/video/fbdev/mxsfb.c
	Resistive touch	ADC touch driver	drivers/input/touchscreen/imx6ul_tsc.c
operating system	Rootfs	Ubuntu 20.04 system	/images/rootfs.tar.bz2
Development Tools	Yocto gatesgarth	Operating system build	/source/yocto-gatesgarth.tar
	Gcc	Cross-compilation tools	/tools/gcc-linaro-7.5.0-2019.12-x86_64_arm-linux-gnueabihf.tar.xz
	uuu	Burning tool	/tools/uuu
	Config Tools for i.MX	Resource Configuration Tools	/tools/Config_Tools_for_i.MX_v15_x64.exe
	balenaEtcher	SD boot card creation tool	/tools/balenaEtcher-Portable-1.18.11.exe

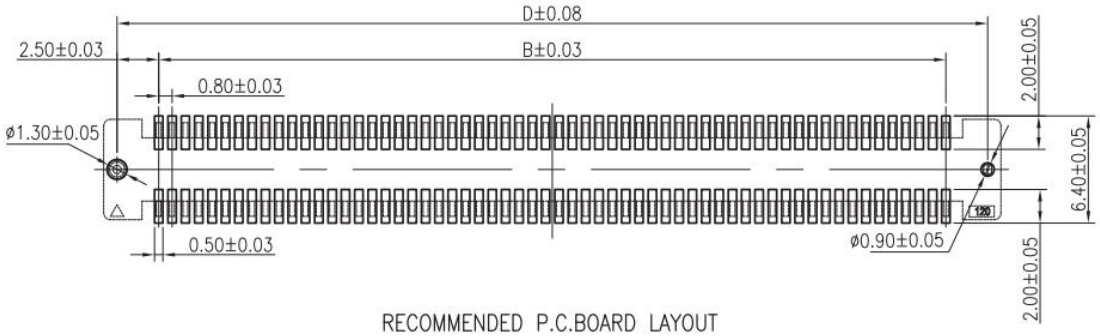
9. Structural dimensions

The ECK20-6Y28C series core board uses a 120-pin, 0.8mm pitch BTB (Board-to-Board) connector interface, allowing for easy and quick insertion with the carrier board. The structural dimensions of the core board are shown in the figure below.

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BTB core board structure size diagram



B=23.20mm D=28.20mm

BTB Connector Dimensions

10. Thermal Design

10.1.Design goals

To ensure the core board operates stably within the industrial temperature range (-40°C to +85°C), th e following objectives must be met:

Junction Temperature Control for Key Components:

i.MX6 Processor: Junction temperature T ≤ 105°C (maximum allowable value).

DDR3/LPDDR2 Memory: T ≤ 95°C, recommended ≤ 85°C.

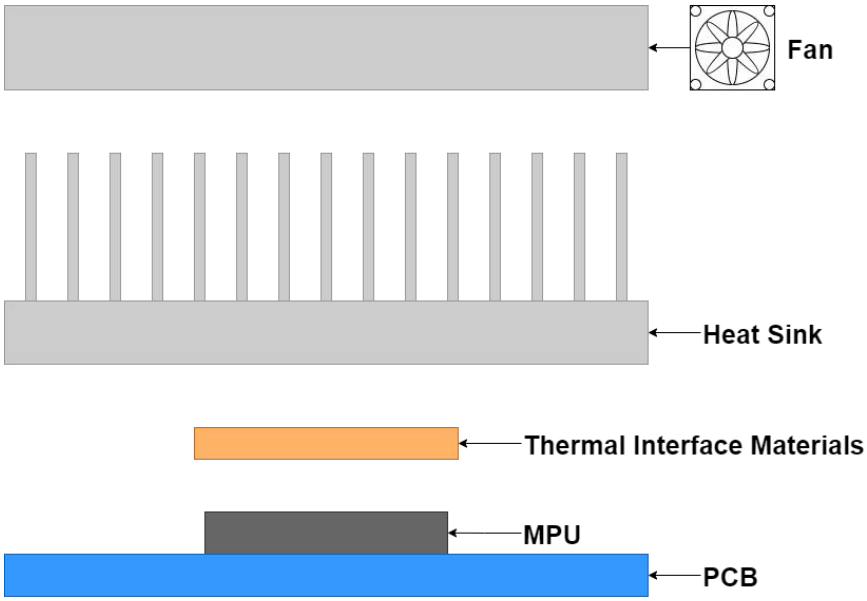
eMMC Storage Chip: T ≤ 105°C, recommended ≤ 95°C.

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10.2.Cooling Solution

Processor Cooling

Since the shield can affect heat dissipation to some extent, it is recommended to remove the shield if using the device in an 85°C environment. Enhance cooling by connecting a heatsink via a thermal pad and installing a fan. Refer to the figure below for reference.

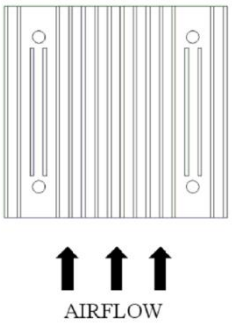


Thermal Design Reference Diagram

It is recommended to use an aluminum black-finned heatsink with dimensions of 40mm x 40mm x 11mm. For the thermal pad, select one with a thickness of 1mm and a thermal conductivity of 7.5 W/m K. The thermal resistance should be 0.198°C-in²/W under conditions of Rthat 40 mils, 10 psi, and 500°C.

System-Level Cooling

It is recommended that the overall chassis airflow design achieves an airspeed of ≥ 1.5 m/s and an airflow volume of ≥ 5 CFM. The orientation of the heatsink should be parallel to the direction of the airflow. Refer to the figure below for reference.



Radiator installation direction reference diagram

10.3.Thermal Design Verification

- Test Conditions

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- Ambient Temperature: 85°C (stabilized for 2 hours).
- Load: Full CPU load (running stress tests under Linux).
- Cooling Solution: Processor cooling.
- Fan Specifications: 5V, 0.2A.
- Test Tools
- Infrared thermal imaging camera, high-temperature test chamber.
- Test Conclusion
- The CPU junction temperature remained at 99.536°C, resulting in a temperature rise of 14.536°C. This indicates that the CPU can sustain long-term heavy-load operation under these conditions.

10.4.Precautions

a.If the system is to be used in a sealed environment, it is necessary to either increase the size of the heatsink or upgrade to active cooling

b.Clean the heatsink every 6 months to remove dust and prevent an increase in thermal resistanc e.

11. Reference Documentation

IMX6ULLIEC.pdf

IMX6ULLRM.pdf

Chip Errata for the i.MX6ULL.pdf

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12. Revision Notes

Revision Notes Table

Version	Modifications	Modification time	prepared by	Proofreading	Approval
V1.0	First Draft	25-02-27	WJ	LqCy	WFX

13. About Us

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