ECK10-13xD Core Board
Product Manual



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1. Product Overview

1.1.Product Introduction

The Ebyte ECK10-13xD series core boards are meticulously designed based on STMicroelectronics' STM32MP13 series processors . These embedded core boards feature gold finger connections for low cost, low power consumption, high cost-performance, and high reliability. They offer a wide range of I/O resources, including up to one LCD display, one digital camera, two Gigabit Ethernet controllers, two USB ports, eight UARTs, two SDIO ports, two CAN ports, and multiple GPIOs.

The ECK10-13xD series core board, based on the STM32MP13 series processor, features integrated power supply circuitry, DDR3L memory, eMMC storage, Wi-Fi, Bluetooth , and USB hub circuitry. It provides stable peripheral circuit references and extensive software development documentation to minimize design complexity and costs.

The ECK10-13xD series core boards include multiple models. These models differ in processor and storage configurations, allowing customers to select the appropriate model based on their needs. For details on product model selection, see the Product Selection section.

The functional block diagram of the core board is as follows:

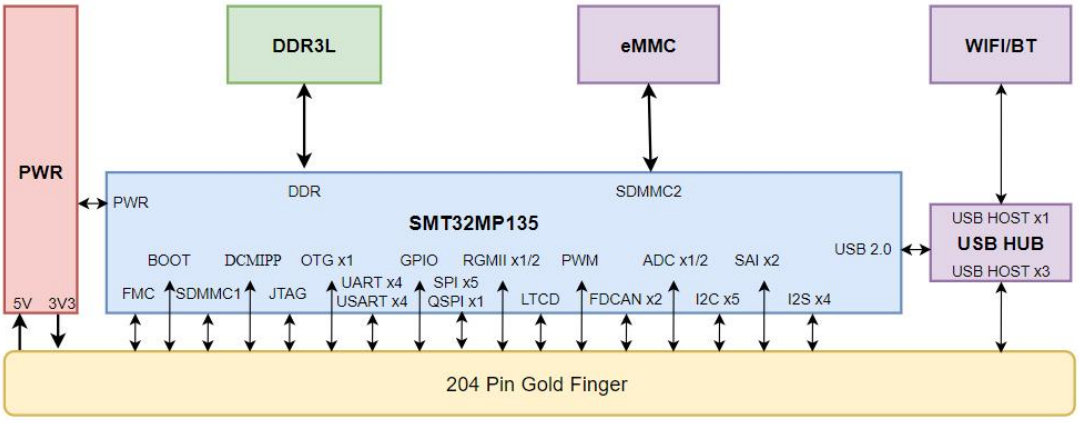


Figure 1.1 Core board functional block diagram

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Physical picture of the core board is as follows:



Figure 1.2 Core board front view



Figure 1.3 Core board back view

1.2.Features

1. Processor: STM32MP13 series processor, main frequency 1GHz ;
2. Memory: On-board DDR3L SDRAM, 256MB/512MB capacity optional;
3. Storage: 8GB eMMC optional;
4. Display: ECK10-13 5D series supports 1 parallel display interface, with a maximum resolution of WXGA (1366×768@60fps) or Full HD (1920×1080@30fps) ;
5. Network: 1 or 2 RGMII interfaces ;
6. USB: 1 USB2.0 OTG interface and 3 USB2.0 HOST interfaces;
7. SDMMC: 1- way MMC/SD/SDIO card interface;
8. Multiple extended I/O interfaces: including UART, CAN, I2C, SPI, SAI, ADC, GPIO , PWM , etc.

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9. Support on-chip watchdog function;

10. Support on-chip RTC function;

11. Interface: 204 -pin DDR3 gold finger ;

12. Power input: single-channel DC +5V±10% power input;

13. Power output: 1-way 3.3V switching power output;

14. Dimensions: 67.6 x 30 x 4.5 mm ;

15. Operating temperature: 0 ℃ -70 ℃ (commercial grade);

16. PCB technology: 8-layer board design, immersion gold, lead-free process , gold finger hard gold plating ;

17. SBC board: ECB10-PGD-I;

1.3.Typical Applications

- Smart home;
- Smart toys;
- Smart cities;
- tablet computers ;
- IoT gateway ;
- Advertising all-in-one machine ;
- Industrial all-in-one machine ;
- Industrial control motherboard;
- Robots and drones.

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2. Model Description

2.1.Model configuration

The ECK10-13xD series core board selection and configuration table is as follows:

Table 2-1 Product selection and configuration table

Serial number	Product Model	Processor model	Memory	storage	Operating temperature
1	ECK10-131D2-C	MP131	256MB DDR3L	/	Commercial Grade 0℃ ~ 70℃
2	ECK10-131D2E8-C	MP131	256MB DDR3L	8GB eMMC	Commercial Grade 0℃ ~ 70℃
3	ECK10-135D2-C	MP135	256MB DDR3L	/	Commercial Grade 0℃ ~ 70℃
4	ECK10-135D5E8-C	MP135	512MB DDR3L	8GB eMMC	Commercial Grade 0℃ ~ 70℃

2.2.Model code

The product model coding is shown in the figure below:

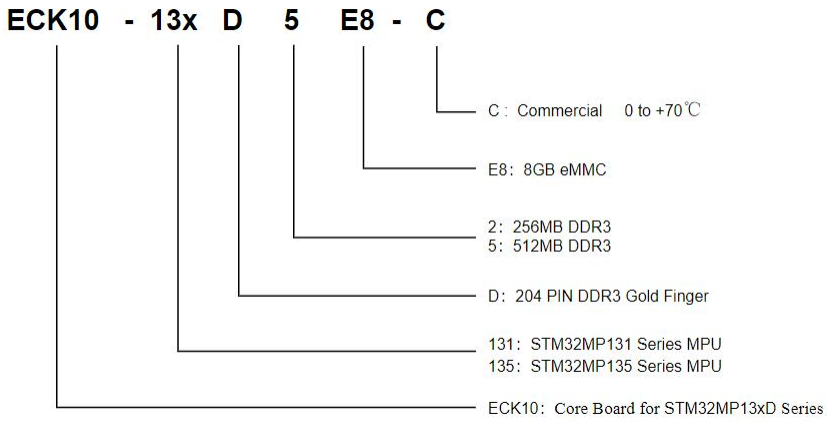


Figure 2.1 Model code description

3. Quick Experience

the ECB10-PGD-I baseboard product of Ebyte allows you to quickly experience the typical application functions, baseboard design, software development, etc. of the ECK10-13xD series core board products.

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4. Functions and parameters

4.1.Product Features

The ECK10-13xD series core board integrates the processor, memory, storage, and power system. Additionally, it includes a Wi-Fi/Bluetooth module and a USB hub, and exposes all available I/O pins on the processor. Users can design a baseboard to utilize the core board's I/O resources and multiplex the I/O into their desired functions.

The following table lists the main integrated functional parameters of the ECK10-13x D series core board and the functional parameters of the reusable I/O resources. The description of each I/O function is the maximum indicator that the core board can use without using other I/O functions (for example, after using the 24-bit RGB interface function and the network interface function, the full UART function cannot be realized).

Table 4-1 Product Function Table

Function	Functional Description
processor	STM32MP131DAF7/STM32MP135DAF7; Single Arm Cortex-A7 core, 1GHz;
Memory	On-board DDR3L SDRAM, 16-bit width, 256MB/512MB optional;
storage	Some models support 8GB eMMC
show	1 parallel display interface, supporting a maximum resolution of WXGA (1366×768@60fps) or Full HD (1920×1080@30fps) (supported only by MP135); Support 24-bit, 18-bit, 16-bit, 8-bit parallel display output;
Camera	1x digital camera input (supported only by MP135);
SDMMC	1 (maximum) BOOT-capable MMC/SD/SDIO card interface;
USB	3x USB2.0 + 1 OTG interface;
Audio	4x (maximum) I2S full-duplex;
Serial Port	4x (maximum) UART; 4x (maximum) USART;
SPI	1x BOOT-capable QSPI; 5x (maximum) SPI, 4 of which can be configured as full-duplex I2S;
Ethernet	2x (maximum) Ethernet MAC, 1x 10/100/1000 Ethernet PHY on board;
CAN	2x (maximum) FDCAN (supported only by MP135);
I2C	5-way (maximum) I2C;
ADC	Supports up to 2 channels (maximum) of 12-bit ADC inputs, each ADC contains multiple channels;
SAI	2-channel SAI, supporting I2S, PDM, and SPDIF transmission;

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JTAG	Support System JTAG Controller;
GPIO	86-channel (maximum) GPIO, supporting interrupt function;
Power consumption	1.55W, see Section 4.4.1 for details;
Power Input	DC +5V±10%@1A；
Power output	3.3V power output, maximum current 500mA.

4.2.Environmental characteristics

Table 4-2 Environmental Characteristics

Operating temperature	Commercial Grade	0℃ ~ 70℃;
Storage temperature	0℃ ~ 70℃;	
Operating humidity	5~95% humidity, non-condensing;	
Storage humidity	60℃@95% humidity, non-condensing;	

4.3.I/O features

4.3.1. I/O pin definition

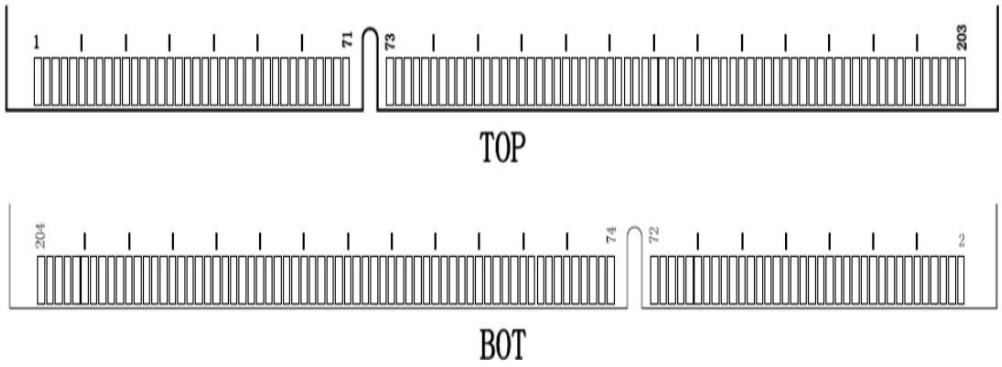


Figure 4.1 Pin numbering diagram

Table 4-3 Pin Definition Table

Pin	Pin Name	MPU Pin	Level/Rail	Type	Length (mil)	Comment
1	VIN_5V	-	5V	PWR	-	
3	VIN_5V	-	5V	PWR	-	
5	VIN_5V	-	5V	PWR	-	
7	VIN_5V	-	5V	PWR	-	

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9	VIN_5V	-	5V	PWR	-	
11	DGND	-	GND	PWR	-	
13	DGND	-	GND	PWR	-	
15	DGND	-	GND	PWR	-	
17	VBAT_EXT	L2	3V3	PWR	1526.37	
19	DGND	-	GND	PWR	-	
21	OTG_VBUS_PI7	AA20	3V3	I/O	2897.48	
23	DGND	-	GND	PWR	-	
25	DGND	-	GND	PWR	-	
27	USB_OTG_HS_DP	AA13	3V3	A	1806.83	
29	USB_OTG_HS_DN	Y13	3V3	A	1807.43	
31	DGND	-	GND	PWR	-	
33	DGND	-	GND	PWR	-	
35	HOST1_USB_DP	-	3V3	A	1810.03	
37	HOST1_USB_DN	-	3V3	A	1809.93	
39	DGND	-	GND	PWR	-	
41	DGND	-	GND	PWR	-	
43	HOST2_USB_DP	-	3V3	A	1779.51	
45	HOST2_USB_DN	-	3V3	A	1779.23	
47	DGND	-	GND	PWR	-	
49	DGND	-	GND	PWR	-	
51	HOST3_USB_DP	-	3V3	A	1845.16	
53	HOST3_USB_DN	-	3V3	A	1845.11	
55	DGND	-	GND	PWR	-	
57	DGND	-	GND	PWR	-	
59	GPIO_PE0	B6	3V3	I/O	786.54	
61	GPIO_PD12	A6	3V3	I/O	738.36	
63	DGND	-	GND	PWR	-	
65	GPIO_PB7	C6	3V3	I/O	543.03	
67	GPIO_PD8	B5	3V3	I/O	696.04	
69	DGND	-	GND	PWR	-	
71	JTRST_NJTRST	V11	3V3	I	1590.17	
73	GPIO_PD1	C5	3V3	I/O	1247.67	
75	GPIO_PA15	B4	3V3	I/O	1214	
77	DGND	-	GND	PWR	-	
79	GPIO_PE12	A4	3V3	I/O	1252.47	
81	GPIO_PD14	C4	3V3	I/O	1220.99	
83	DGND	-	GND	PWR	-	
85	GPIO_PE13	A3	3V3	I/O	1215.88	
87	GPIO_PE14	C3	3V3	I/O	1266.91	
89	DGND	-	GND	PWR	-	
91	GPIO_PA9	A2	3V3	I/O	504.62	
93	GPIO_PE11	B2	3V3	I/O	519.06	

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95	DGND	-	GND	PWR	-	
97	GPIO_PH12	D3	3V3	I/O	582.56	
99	GPIO_PB8	D1	3V3	I/O	543.03	
101	DGND	-	GND	PWR	-	
103	GPIO_PH8	E3	3V3	I/O	1198.97	
105	GPIO_PA8	P2	3V3	I/O	1003.17	
107	DGND	-	GND	PWR	-	
109	GPIO_PF7	P3	3V3	I/O	612.76	
111	GPIO_PG11	R2	3V3	I/O	600.28	
113	DGND	-	GND	PWR	-	
115	GPIO_PG1	R1	3V3	I/O	600.79	
117	GPIO_PG3	W1	3V3	I/O	691.27	
119	DGND	-	GND	PWR	-	
121	GPIO_PA11	Y1	3V3	I/O	976.97	
123	GPIO_PF14	Y2	3V3	I/O	496.66	
125	DGND	-	GND	PWR	-	
127	GPIO_PF13	W4	3V3	I/O	559.73	
129	GPIO_PB11	AA2	3V3	I/O	1096.68	
131	DGND	-	GND	PWR	-	
133	GPIO_PA1	AA3	3V3	I/O	1013.18	
135	GPIO_PA2	Y4	3V3	I/O	653.53	
137	DGND	-	GND	PWR	-	
139	GPIO_PC0	W5	3V3	I/O	986.98	
141	GPIO_PA5	Y5	3V3	I/O	780.94	
143	DGND	-	GND	PWR	-	
145	GPIO_PA4	AA4	3V3	I/O	812.83	
147	GPIO_PC4	Y7	3V3	I/O	979.23	
149	DGND	-	GND	PWR	-	
151	GPIO_PE4	H2	3V3	I/O	1231.73	
153	GPIO_PA12	F4	3V3	I/O	1019.42	
155	DGND	-	GND	PWR	-	
157	GPIO_PG15	H4	3V3	I/O	1013.45	
159	GPIO_PG8	H5	3V3	I/O	1075.27	
161	DGND	-	GND	PWR	-	
163	GPIO_PF12	AA4	3V3	I/O	1077.69	
165	GPIO_PF11	Y6	3V3	I/O	1150.98	
167	DGND	-	GND	PWR	-	
169	GPIO_PB10	E13	3V3	I/O	1570.33	
171	GPIO_PA13	T4	3V3	I/O	1045.86	
173	DGND	-	GND	PWR	-	
175	GPIO_PA6	U10	3V3	I/O	1151.68	
177	GPIO_PB0	W8	3V3	I/O	1066.82	
179	DGND	-	GND	PWR	-	

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181	GPIO_PC1	Y9	3V3	I/O	1142.53	
183	GPIO_PE5	W10	3V3	I/O	1192.3	
185	DGND	-	GND	PWR	-	
187	GPIO_PB13	D14	3V3	I/O	1732.74	
189	GPIO_PB5	B13	3V3	I/O	1667.89	
191	DGND	-	GND	PWR	-	
193	GPIO_PH10	E14	3V3	I/O	1692.92	
195	GPIO_PD6	D2	3V3	I/O	2018.6	
197	DGND	-	GND	PWR	-	
199	GPIO_PF10	H3	3V3	I/O	2205.27	
201	GPIO_PF5	B3	3V3	I/O	2169.56	
203	GPIO_PD0	B1	3V3	I/O	2282.41	
2	VCC_3V3	-	3V3	PWR	-	
4	VCC_3V3	-	3V3	PWR	-	
6	DGND	-	GND	PWR	-	
8	DGND	-	GND	PWR	-	
10	DGND	-	GND	PWR	-	
12	NRST	Y11	3V3	I/O		
14	DGND	-	GND	PWR	-	
16	GPIO_PG10	G2	3V3	I/O	1514.22	
18	GPIO_PD3	C2	3V3	I/O	1318.85	
20	DGND	-	GND	PWR	-	
22	GPIO_PD11	F3	3V3	I/O	1356.27	
24	GPIO_PB6	C1	3V3	I/O	1211.95	
26	DGND	-	GND	PWR	-	
28	GPIO_PC12	A19	3V3	I/O	1403.87	22Ω in series
30	GPIO_PC10	A18	3V3	I/O	1338.61	
32	DGND	-	GND	PWR	-	
34	GPIO_PC11	B18	3V3	I/O	1277.88	
36	GPIO_PD2	C19	3V3	I/O	1322.68	
38	DGND	-	GND	PWR	-	
40	GPIO_PC9	A20	3V3	I/O	1222.47	
42	GPIO_PF3	A13	3V3	I/O	1207.01	
44	DGND	-	GND	PWR	-	
46	GPIO_PH9	C12	3V3	I/O	1229.13	
48	GPIO_PB12	C11	3V3	I/O	1222.85	
50	DGND	-	GND	PWR	-	
52	GPIO_PF1	B11	3V3	I/O	968.01	
54	GPIO_PH13	A12	3V3	I/O	948.55	
56	DGND	-	GND	PWR	-	
58	GPIO_PE10	C10	3V3	I/O	910.74	
60	GPIO_PH14	B8	3V3	I/O	863.73	

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62	DGND	-	GND	PWR	-	
64	GPIO_PG0	A7	3V3	I/O	1951.66	
66	GPIO_PE9	B7	3V3	I/O	1240.95	
68	DGND	-	GND	PWR	-	
70	GPIO_PD4	C7	3V3	I/O	1208.35	
72	GPIO_PD5	C8	3V3	I/O	1201.29	
74	GPIO_PE15	A9	3V3	I/O	1208.15	
76	GPIO_PG7	A10	3V3	I/O	1209.49	
78	DGND	-	GND	PWR	-	
80	GPIO_PE8	B9	3V3	I/O	681.76	
82	GPIO_PG4	B10	3V3	I/O	1207.24	
84	DGND	-	GND	PWR	-	
86	GPIO_PC8	C18	3V3	I/O	1247.05	
88	GPIO_PF2	D11	3V3	I/O	674.21	
90	DGND	-	GND	PWR	-	
92	GPIO_PD9	C9	3V3	I/O	1297.46	
94	GPIO_PD15	E9	3V3	I/O	1213.05	
96	DGND	-	GND	PWR	-	
98	GPIO_PE7	D8	3V3	I/O	1213.42	
100	GPIO_PD10	D6	3V3	I/O	1262.25	
102	DGND	-	GND	PWR	-	
104	GPIO_PE1	E8	3V3	I/O	669.22	
106	GPIO_PG9	F2	3V3	I/O	532.46	
108	GPIO_PH2	E2	3V3	I/O	1231.72	
110	DGND	-	GND	PWR	-	
112	GPIO_PF6	G1	3V3	I/O	656.98	
114	GPIO_PF8	F1	3V3	I/O	1200.43	
116	GPIO_PD13	J2	3V3	I/O	1206.69	
118	DGND	-	GND	PWR	-	
120	GPIO_PG5	G3	3V3	I/O	674.41	
122	GPIO_PH7	J1	3V3	I/O	1200.18	
124	DGND	-	GND	PWR	-	
126	GPIO_PB2	J3	3V3	I/O	738.56	
128	GPIO_PH6	N3	3V3	I/O	996.07	
130	DGND	-	GND	PWR	-	
132	GPIO_PE2	N1	3V3	I/O	631.3	
134	GPIO_PG2	V3	3V3	I/O	624.2	
136	DGND	-	GND	PWR	-	
138	GPIO_PD7	V1	3V3	I/O	565.02	
140	GPIO_PG12	W2	3V3	I/O	593.31	
142	DGND	-	GND	PWR	-	
144	GPIO_PH3	R3	3V3	I/O	1199.5	
146	GPIO_PE6	T2	3V3	I/O	782.57	

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148	DGND	-	GND	PWR	-	
150	GPIO_PF4	N2	3V3	I/O	983.88	
152	GPIO_PC3	W6	3V3	I/O	846.58	
154	DGND	-	GND	PWR	-	
156	GPIO_PC5	AA7	3V3	I/O	952.79	
158	GPIO_PG13	AA9	3V3	I/O	1137.92	
160	DGND	-	GND	PWR	-	
162	GPIO_PH11	K3	3V3	I/O	1066.61	
164	GPIO_PI3	L4	3V3	I/O	1071.97	
166	DGND	-	GND	PWR	-	
168	GPIO_PF9	J5	3V3	I/O	1140.16	
170	GPIO_PC13	M3	3V3	I/O	1266.72	
172	GPIO_PA7	V6	3V3	I/O	1024.1	
174	DGND	-	GND	PWR	-	
176	GPIO_PF15	Y12	3V3	I/O	1140.09	
178	GPIO_PB1	Y8	3V3	I/O	1076.12	
180	GPIO_PA3	W9	3V3	I/O	1136.39	
182	DGND	-	GND	PWR	-	
184	GPIO_PG14	Y10	3V3	I/O	1207.18	
186	GPIO_PC2	AA10	3V3	I/O	1231.64	
188	GPIO_PI5-BOOT1	AA15	3V3	I/O	1298.8	10KΩ pull up
190	DGND	-	GND	PWR	-	
192	GPIO_PI6-BOOT2	Y15	3V3	I/O	1355.39	10KΩ pull up
194	GPIO_PI4-BOOT0	Y17	3V3	I/O	1389.42	10KΩ pull up
196	GPIO_PA14	W13	3V3	I/O	1350.39	
198	DGND	-	GND	PWR	-	
200	GPIO_PA10	AA19	3V3	I/O	1405.93	
202	GPIO_PH5	W18	3V3	I/O	1531.93	
204	GPIO_PH4	Y19	3V3	I/O	1480.8	

Note:

- In the "Type" column, "A" represents a special pin; "I" represents digital input; "I/O" represents digital input and output; PWR represents power supply;
- Generally, the single-ended signal impedance is 50±10%Ω, and the trace length unit is mil;
- For detailed information on the pin multiplexing functions of the gold finger connector, please refer to the ECK10-13xD Pin List document.

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4.3.2. Differential impedance

Table 4-4 Differential trace impedance control table

Pins	Pin Name	Trace length	Impedance control	illustrate
27	USB_OTG_HS_DP	1806.83	90±10%Ω	USB signal
29	USB_OTG_HS_DN	1807.43	90±10%Ω	USB signal
35	HOST1_USB_DP	1810.03	90±10%Ω	USB signal
37	HOST1_USB_DN	1809.93	90±10%Ω	USB signal
43	HOST2_USB_DP	1779.51	90±10%Ω	USB signal
45	HOST2_USB_DN	1779.23	90±10%Ω	USB signal
51	HOST3_USB_DP	1845.16	90±10%Ω	USB signal
53	HOST3_USB_DN	1845.11	90±10%Ω	USB signal

4.4.Electrical characteristics

4.4.1. Power consumption

The following parameters were measured on the ECK10-135D5E8-C core board at room temperature. The measured power consumption does not include the baseboard power consumption. Heavy-load power consumption was measured while running memory and eMMC test programs, network and USB communications, with no display, and without baseboard SDIO access. Factors such as test methods, usage functions, and ambient temperature can affect power consumption. The following power consumption data is for reference only.

Table 4-5 Power consumption table

Power Status	Test environment	Power supply voltage	Current	Power consumption
BOOT	UBOOT running process	5.0V	0.15A	0.75W
PWRUP	Entering the system without running the application	5.0V	0.22A	1.10W
PWRUP	Software reload testing	5.0V	0.31A	1.55W
SLEEP	mem mode sleep state	5.0V	0.05A	0.25W

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5. Core board hardware design

5.1.processor

5.1.1. STM32MP131D processor

Features			STM32MP131AAE STM32MP131DAE	STM32MP131AAG STM32MP131DAG	STM32MP131AAF STM32MP131DAF	Miscellaneous
			LFBGA289	TFBGA289	TFBGA320	
Package		Body size (mm)	14x14	9x9	11x11	-
		Pitch (mm)	0.8	0.5	0.5	
		Ball size (mm)	0.40	0.30	0.30	
		Thickness (mm)	< 1.4	< 1.2	< 1.2	
		Ball count	289	289	320	
CPU			Cortex-A7 FPU Neon TrustZone			-
		Caches size	32-Kbyte L1 data cache			
			32-Kbyte L1 instruction cache			
			128-Kbyte L2 unified coherent cache			
		Frequency	STM32MP131A: 650 MHz STM32MP131D: 1 GHz			
ROM			128 Kbytes (secure)			-
Embedded SRAM		System RAM	128 Kbytes (securable)			168 Kbytes
		Backup	8 Kbytes (securable, tamper protected)			
		AHB SRAM	32 Kbytes			
SDRAM			Securable			-
	LPDDR2/3	16-bit 533 MHz	Up to 1 Gbyte, single rank			
	DDR3/3L	16-bit 533 MHz				
Backup registers			128 bytes (32x32-bit, securable, tamper protected)			-
Timers	Advanced	16 bits	2			24 timers
	General purpose	16 bits	8 (6 securable)			
		32 bits	2			
	Basic	16 bits	2			
	Low power	16 bits	5 (2 securable)			
	A7 timers	64 bits	4 (secure, non-secure, virtual, hypervisor)			
	RTC/AWU		1 (securable)			

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Features			STM32MP131AAE STM32MP131DAE	STM32MP131AAG STM32MP131DAG	STM32MP131AAF STM32MP131DAF	Miscellaneous
			LFBGA289	TFBGA289	TFBGA320	
Watchdogs			2 (independent, independent secure)			-
Communication peripherals	SPI		5 (2 securable)			-
		Having I2S	4			
	I2C (with SMB/PMB support)		5 (3 securable)			
	USART (smartcard, SPI, IrDA, LIN) + UART (IrDA, LIN)		4 + 4 (including 2 securable USART), some can be a boot source			Boot
	SAI		2 (up to 4 audio channels), with I2S master/slave, PCM input, SPDIF-TX			-
	USB	EHCI/OHCI Host	2 ports			-
			Embedded HSPHY with BCD			
		OTG HS	Embedded HS PHY with BCD (securable), can be a boot source			Boot
		Embedded PHYs	2 × HS shared between Host and OTG			-
	SPDIFRX		4 inputs			-
SDMMC (SD, SDIO, e•MMC)			2 (8 + 8 bits) (securable), e•MMC or SD can be a boot source 2 optional independant power supplies for SD card interfaces			Boot
QUADSPI			1 (dual-quad) (securable), can be a boot source			Boot (1)
FMC	Parallel address/data 8/16-bit		4 × CS, up to 4 × 64 Mbyte			-
	Parallel AD-mux 8/16-bit					
	NAND 8/16-bit		Yes, 2× CS, SLC, BCH4/8, can be a boot source			Boot
10/100M/Gigabit Ethernet			1 x (MII, RMI, RGMII) with PTP and EEE (securable)			-
DMA			3 instances (1 secure), 33-channel MDMA			-
Hash			SHA-1, SHA-224, SHA-256, SHA-384, SHA-512, SHA-3, HMAC (securable)			-
True random number generator			True-RNG (securable)			-
Fuses (one-time programmable)			3072 effective bits (secure, 1280 bits available for the user)			-
GPIOs with interrupt (total count)			135(2)			-
	Securable GPIOs		All			
	Wakeup pins		6			
	Tamper pins (active tamper)		12 (5)			

Features		STM32MP131AAE STM32MP131DAE	STM32MP131AAG STM32MP131DAG	STM32MP131AAF STM32MP131DAF	Miscellaneous
		LFBGA289	TFBGA289	TFBGA320	
DFSDM		4 input channels with 2 filters			-
Up to 12-bit synchronized ADC		1 (up to 5 Msps on 12-bit each) (securable)			-
	12-bit ADC channels in total(3)	ADC2: 18 channels including 6x internal, 12 channels available for user including 6x differential			
Internal ADC VREF		1.65 V, 1.8 V, 2.048 V, 2.5 V or VREF+ input			-
	VREF+ input pin	Yes			

Figure 5.1 STM32MP131D processor function table

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5.1.2. STM32MP135D processor

Features			STM32MP135AAE STM32MP135DAE	STM32MP135AAG STM32MP135DAG	STM32MP135AAF STM32MP135DAF	Miscellaneous
			LFBGA289	TFBGA289	TFBGA320	
Package		Body size (mm)	14x14	9x9	11x11	-
		Pitch (mm)	0.8	0.5	0.5	
		Ball size (mm)	0.40	0.30	0.30	
		Thickness (mm)	< 1.4	< 1.2	< 1.2	
		Ball count	289	289	320	
CPU			Cortex-A7 FPU Neon TrustZone			-
		Caches size	32-Kbyte L1 data cache			
			32-Kbyte L1 instruction cache			
			128-Kbyte L2 unified coherent cache			
		Frequency	STM32MP135A: 650 MHz STM32MP135D: 1 GHz			
ROM			128 Kbytes (secure)			-
Embedded SRAM		System RAM	128 Kbytes (securable)			168 Kbytes
		Backup	8 Kbytes (securable, tamper protected)			
		AHB SRAM	32 Kbytes			
SDRAM			Securable			-
	LPDDR2/3	16-bit 533 MHz	Up to 1 Gbyte, single rank			
	DDR3/3L	16-bit 533 MHz				
Backup registers			128 bytes (32x32-bit, securable, tamper protected)			-
Timers	Advanced	16 bits	2			24 timers
	General purpose	16 bits	8 (6 securable)			
		32 bits	2			
	Basic	16 bits	2			
	Low power	16 bits	5 (2 securable)			
	A7 timers	64 bits	4 (secure, non-secure, virtual, hypervisor)			
	RTC/AWU		1 (securable)			

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Features			STM32MP135AAE STM32MP135DAE	STM32MP135AAG STM32MP135DAG	STM32MP135AAF STM32MP135DAF	Miscellaneous
			LFBGA289	TFBGA289	TFBGA320	
Watchdogs			2 (independent, independent secure)			-
Communication peripherals	SPI		5 (2 securable)			-
		Having I2S	4			
	I2C (with SMB/PMB support)		5 (3 securable)			
	USART (smartcard, SPI, IrDA, LIN) + UART (IrDA, LIN)		4 + 4 (including 2 securable USART), some can be a boot source			Boot
	SAI		2 (up to 4 audio channels), with I2S master/slave, PCM input, SPDIF-TX			-
	USB	EHCI/OHCI Host	2 ports			-
			Embedded HSPHY with BCD			
		OTG HS	Embedded HS PHY with BCD (securable), can be a boot source			Boot
		Embedded PHYs	2 × HS shared between Host and OTG			-
	SPDIFRX		4 inputs			-
	FDCAN		2 (1 × TTCAN), clock calibration, 10 Kbyte shared buffer			-
SDMMC (SD, SDIO, e•MMC)			2 (8 + 8 bits) (securable), e•MMC or SD can be a boot source 2 optional independant power supplies for SD card interfaces			Boot
QUADSPI			1 (dual-quad) (securable), can be a boot source			Boot (1)
FMC	Parallel address/data 8/16-bit		4 × CS, up to 4 × 64 Mbyte			-
	Parallel AD-mux 8/16-bit					
	NAND 8/16-bit		Yes, 2× CS, SLC, BCH4/8, can be a boot source			Boot
10/100M/Gigabit Ethernet			2 x (MII, RMI, RGMII) with PTP and EEE (securable)			-
LCD-TFT		Parallel interface	Up to 24-bit data, 1 secure layer, YUV on 1 layer (up to 1366×768 @ 60 fps) or up to Full HD (1920 x 1080) @ 30 fps Pixel clock up to 90 MHz			-
DMA			3 instances (1 secure), 33-channel MDMA			-
Hash			SHA-1, SHA-224, SHA-256, SHA-384, SHA-512, SHA-3, HMAC (securable)			-
True random number generator			True-RNG (securable)			-
Fuses (one-time programmable)			3072 effective bits (secure, 1280 bits available for the user)			-
Camera interface		Bus width	16-bit			-

Features		STM32MP135AAE STM32MP135DAE	STM32MP135AAG STM32MP135DAG	STM32MP135AAF STM32MP135DAF	Miscellaneous
		LFBGA289	TFBGA289	TFBGA320	
GPIOs with interrupt (total count)		135(2)			-
	Securable GPIOs	All			
	Wakeup pins	6			
	Tamper pins (active tamper)	12 (5)			
DFSDM		4 input channels with 2 filters			-
Up to 12-bit synchronized ADC		2(3) (up to 5 Msps on 12-bit each) (securable)			-
	12-bit ADC channels in total(4)	ADC1: 19 channels including 1x internal, 18 channels available for user including 8x differential ADC2: 18 channels including 6x internal, 12 channels available for user including 6x differential			
Internal ADC VREF		1.65 V, 1.8 V, 2.048 V, 2.5 V or VREF+ input			-
	VREF+ input pin	Yes			

Figure 5.2 STM32MP135D processor function table

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5.2.Memory

The ECK10-13xD series core boards feature on-board DDR3L SDRAM memory chips. Designed with a 16-bit memory data width, they are available in 256MB and 512MB capacities.

5.3.clock

The ECK10-13xD series core board provides a 32.768KHz crystal (passive) oscillator circuit and a

24MHz crystal (passive) oscillator circuit, used as the processor system clock source.

Table 5-1 Clock I/O Allocation Table

MPU I/O pins	Function
PC14	32.768KHz IN
PC15	32.768KHz OUT
PH0	24MHz IN
PH1	24MHz OUT

5.4.storage

5.4.1. Onboard storage

The ECK10-13xD series core boards feature an onboard eMMC storage solution. This storage solution utilizes eMMC chips as the storage medium, offering large storage capacity, low unit storage cost, and ease of use. Currently, the ECK10-131D2E8-C and ECK10-135D5E8-C core boards feature an 8GB 8-bit eMMC.

Table 5-2 eMMC chip I/O allocation table

MPU I/O pins	Function
PB14	SDMMC2_D0
PB15	SDMMC2_D1
PB3	SDMMC2_D2
PB4	SDMMC2_D3
PF0	SDMMC2_D4
PB9	SDMMC2_D5
PC6	SDMMC2_D6
PC7	SDMMC2_D7
PG6	SDMMC2_CMD
PE3	SDMMC2_CK

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PA0	RESET

5.4.2. Extended storage interface

In addition to onboard storage, the core board provides SDMMC and FMC interfaces for users to expand SD cards, eMMC storage, NAND storage, WiFi, and other functions. Note that some functions are reused. For example, if PE8 uses the UART7_TX function, the FMC_D5 function cannot be used. Users need to weigh the function allocation. FMC consumes a large amount of IO, so it is recommended to use SDMMC for storage expansion. The recommended interface pin assignments are shown in the table below:

Table 5-3 SDMMC interface I/O allocation table

Gold finger pin	MPU I/O pins	Function	Length (mil)	illustrate
28	PC12	SDMMC1_CK	1403.87	
36	PD2	SDMMC1_CMD	1322.68	internal pull-up
86	PC8	SDMMC1_D0	1247.05	internal pull-up
40	PC9	SDMMC1_D1	1222.47	internal pull-up
30	PC10	SDMMC1_D2	1338.61	internal pull-up
34	PC11	SDMMC1_D3	1277.88	internal pull-up

Table 5-4 FMC interface I/O allocation table

	MPU I/O pins	Function	Length (mil)	illustrate
106	PG9	FMC_NCE	532.46	
61	PD12	FMC_ALE	738.36	
twenty two	PD11	FMC_CLE	1356.27	
70	PD4	FMC_NOE	1208.35	
72	PD5	FMC_NWE	1201.29	
91	PA9	FMC_NWAIT	504.62	internal pull-up
81	PD14	FMC_D0	1220.99	internal pull-up
94	PD15	FMC_D1	1213.05	internal pull-up
203	PD0	FMC_D2	2282.41	internal pull-up
73	PD1	FMC_D3	1213.05	internal pull-up
98	PE7	FMC_D4	1213.42	internal pull-up
80	PE8	FMC_D5	681.76	internal pull-up
66	PE9	FMC_D6	1240.95	internal pull-up
58	PE10	FMC_D7	910.74	internal pull-up
93	PE11	FMC_D8	519.06	internal pull-up
79	PE12	FMC_D9	1252.47	internal pull-up
85	PE13	FMC_D10	1215.88	internal pull-up

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87	PE14	FMC_D11	1266.91	internal pull-up
74	PE15	FMC_D12	1208.15	internal pull-up
99	PB8	FMC_D13	543.03	internal pull-up
92	PD9	FMC_D14	1297.46	internal pull-up
100	PD10	FMC_D15	1262.25	internal pull-up

5.4.3. LAYOUT Suggestions

- signal in the core board is controlled according to the single-ended 50Ω±10% impedance. It is recommended that the impedance control of the baseboard remain consistent.
- The SDMMC signals have been processed into equal lengths in the core board. For the trace lengths in the core board, see the pin definition table.
- It is recommended that the SDMMC signal (excluding the insertion detection signal) on the baseboard be routed with equal length control, with an error range of ± 100 mil , and the signal line spacing be at least 3 W. It is recommended that the clock signal be grounded.
- The FMC signal core board does not have equal length control. If the user wants to use it, he can control the equal length according to the length in the table and the baseboard design.

5.5.power supply

5.5.1. Power supply solution

The ECK10-13xD series core boards utilize a discrete power supply solution, designed strictly in accordance with the voltage, power, and timing requirements specified in the STM32MP13x series chip manual. The ECK10-13xD series core boards are powered by a DC +5V power supply. Only the V5_IN power input is required externally; all other power is generated internally by the core board, eliminating the need for an external power supply.

The ECK10-13xD series core board also provides a VCC_3V power output, which can be used to power low-power devices on the baseboard and control the power-on timing of the baseboard I/O interfaces. The power-related pins are shown in the table below.

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Table 5-5 Power Interface Definition Table

Gold finger pin	Power network name	Power supply type	Typical voltage	Maximum current
1	VIN_5V	POWER-I	5.0V	2500mA
3	VIN_5V	POWER-I	5.0V	
5	VIN_5V	POWER-I	5.0V	
7	VIN_5V	POWER-I	5.0V	
9	VIN_5V	POWER-I	5.0V	
2	VCC_3V3	POWER-O	3.3V	500mA
4	VCC_3V3	POWER-O	3.3V	
17	VBAT_EXT	POWER-I	3.3V	

Note: The maximum VBAT_EXT current is related to the VBAT configuration mode and operating temperature. For details, please refer to "Table 27. Current consumption in VBAT mode " in the STM32MP13xD chip manual.

5.5.2. VDD_CPU power supply

The VDD_CPU power supply design of the ECK10-13xD series core board supports 1.25V and 1.35V level switching. The hardware design uses PWR_OVRDRV as the control pin for voltage switching, which is the GPIO function of the processor PI0 pin.

Pay attention to the configuration of PI0 when configuring I/O hardware and functions.

Table 5-6 VDD_CPU power configuration table

PWR_OVRDR status	VDD_CPU power supply
H	1.35V
L	1.25V

The hardware schematic is as follows.

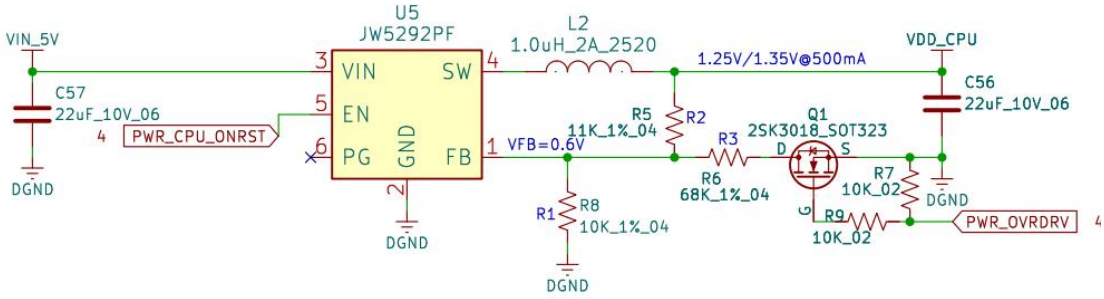


Figure 5.3 VDD_CPU power supply schematic

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5.5.3. VDD_CORE power supply

The VDD_CORE power supply design of the ECK10-13xD series core boards supports voltage switching between 0.9V and 1.25V. The hardware design uses the processor's PWR_LP as the voltage switching control pin.

Table 5-7 VDD_CPU power configuration table

PWR_LP status	VDD_COER power supply
H	1.25V
L	0.9V

The hardware schematic is as follows.

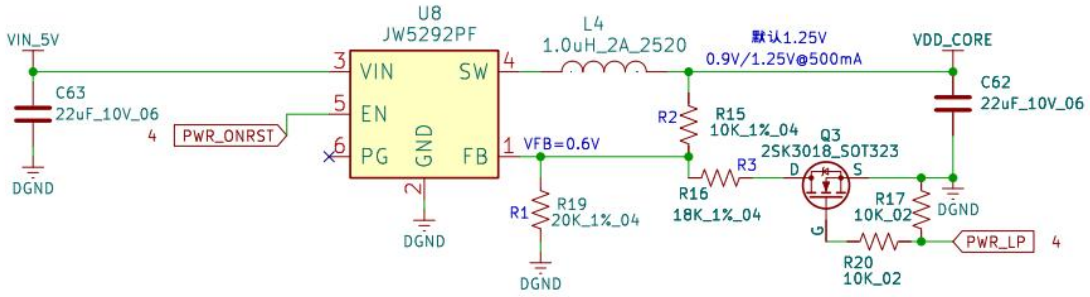


Figure 5.4 VDD_COER power supply schematic

5.5.4. VDD_SD power supply

The SDMMC1 interface on the ECK10-13xD series core boards supports 3.3V and 1.8V I/O voltage levels. The hardware design uses SD_VSEL as the voltage switching control pin, which functions as the GPIO pin PI2 on the processor. Software should pay attention to the configuration of PI0 when configuring I/O hardware and functions.

Table 5-8 VDD_SD power supply configuration table

SD_VSEL status	VDD_SD power supply
H	1.8V
L	3.3V

The hardware schematic is as follows.

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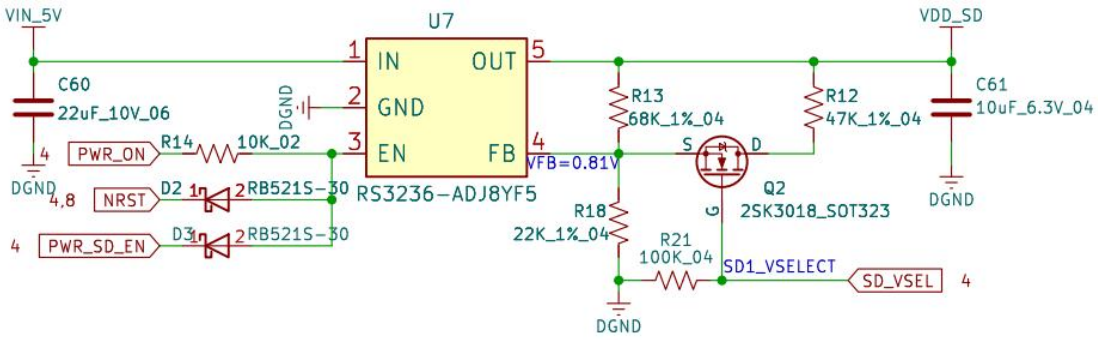


Figure 5.5 VDD_SD power supply schematic

5.5.5. RTC power supply

VBAT_EXT is the RTC backup battery interface, corresponding to pin 17 of the gold finger, and can be powered by an external battery.

Its function is to supply power to the core board RTC power supply through the external battery when the core board 5V power supply is lost, so as to maintain the normal operation of the processor's internal RTC function, power management function, and some configuration registers. The voltage range of VBAT_EXT is 1.6-3.6V.

In the core board, the VBAT_EXT power supply is connected in parallel with the 3.3V power supply on the board and then input to the VBAT pin of the MPU chip. The parallel circuit is shown in the figure below.

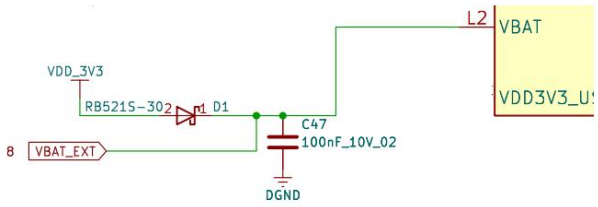


Figure 5.6 VBAT power supply parallel circuit diagram

As shown in the figure above, when two power supplies are connected in parallel on the core board, the VBAT_EXT power supply has no series diode.

The board uses a button battery to provide RTC backup power. To prevent the internal power supply from charging the battery after power is turned on, the bottom board should be

A diode is connected in series to the VBAT_EXT circuit, as shown in the figure below.

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Figure 5.7 Baseboard VBAT power supply reference circuit diagram

If the RTC backup battery and related functions are not used, the VBAT_EXT pin can be left floating.

5.5.6. Core board power timing

The ECK10-13xD series core board power domains and power-up sequence are very simple. The main power domains consist of VIN, VIO, and VCORE. VCORE is only relevant to the processor and has no bearing on user I/O interfaces, so it is not a concern in applications. The power-up sequence for the ECK10-13xD series core board is shown in the figure below.

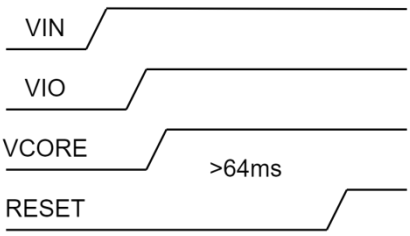


Figure 5.8 Core board power-on timing diagram

All external I/O interfaces of the ECK10-13xD series core boards belong to the VIO power domain. The baseboard can use the VCC_3V3 power output by the core board as the control signal for the baseboard I/O interface power domain.

5.6.Launch Configuration

5.6.1. Boot order configuration

The ECK10-13xD core board supports multiple boot modes. After powering on, the chip reads the voltage level on the BOOT[2:0] pins. Different voltage levels correspond to specific boot modes. BOOT[2:0] has a 10K pull-up resistor on the core board. In general, a pull-down resistor can be designed on the baseboard; a 1K pull-down resistor is recommended. The BOOT

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configuration mode is shown below.

Table 2. Boot modes

BOOT2	BOOT1	BOOT0	Initial boot mode	Comments
0	0	0	UART and USB(1)	Wait incoming connection on: – USART3/6 and UART4/5/7/8 on default pins – USB high-speed device on OTG_HS_DP/DM pins(2)
0	0	1	Serial NOR flash(3)	Serial NOR flash on QUADSPI(5)
0	1	0	*e*•MMC(3)	*e*•MMC on SDMMC2 (default)(5)(6)
0	1	1	NAND flash(3)	SLC NAND flash on FMC
1	0	0	Development boot (no flash memory boot)	Used to get debug access without boot from flash memory(4)
1	0	1	SD card(3)	SD card on SDMMC1 (default)(5)(6)
1	1	0	UART and USB(1)(3)	Wait incoming connection on: – USART3/6 and UART4/5/7/8 on default pins – USB high-speed device on OTG_HS_DP/DM pins(2)
1	1	1	Serial NAND flash(3)	Serial NAND flash on QUADSPI(5)

Figure 5.9 BOOT mode configuration diagram

For the ECK10-13xD core board, if booting from the core board's eMMC, configure BOOT[2:0] to 010. If booting from the SD card on the baseboard's SDMMC1 port, configure BOOT[2:0] to 101. If booting from USB OTG in debug mode, configure BOOT[2:0] to 000. The baseboard circuit design corresponding to the BOOT[2:0] signal is shown in the figure below.

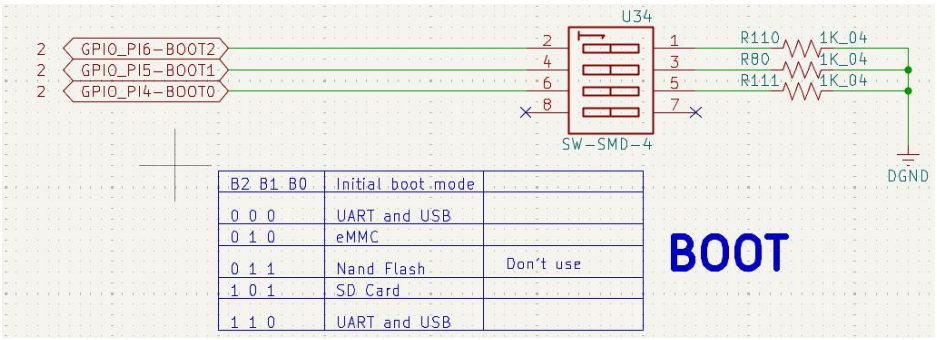


Figure 5.10 BOOT signal baseboard circuit reference diagram

5.6.2. BOOT pin definition

Table 5-9 BOOT mode interface definition table

Gold finger pin	MPU I/O pins	Function	Length (mil)	illustrate
194	PI4	BOOT0	1389.42	10K pull-up
188	PI5	BOOT1	1298.8	10K pull-up
192	PI6	BOOT2	1355.39	10K pull-up

5.7.Reset button

The NRST signal from the ECK10-13xD series core board can be connected to an external

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button to reset the processor. The NRST signal is a bidirectional input/output signal that can be used as an external reset input to reset the processor and also serves as the core board power reset signal output. The NRST signal has a built-in pull-up resistor in the processor. Therefore, when using the NRST signal as a manual reset input on the backplane, do not connect a pull-up resistor. Instead, connect it directly to the button or drive it through an OD gate. Also, do not drive the NRST signal through a push-pull output interface. When connecting a manual input button, place a small capacitor and TVS to reduce interference and improve ESD performance. The reference schematic for the button is shown below.

5.7.1. Reference Circuit

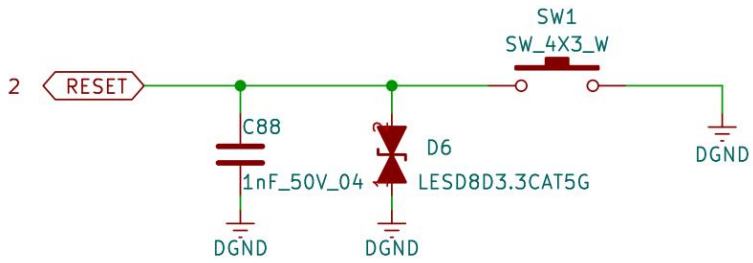


Figure 5.11 button reference schematic

Note: Do not arbitrarily pull up the reset and power button signals through resistors. If the pull-up power rail is incorrect, it will cause uncertain signals to be input to the button signal interface when the system is in standby or shutdown.

5.7.2. Reset pin definition

Table 5-10 Button Pin Definitions

Gold finger pin	MPU I/O pins	Function	Length (mil)	illustrate
12	NRST	NRST	1229.13	internal pull-up

5.7.3. LAYOUT Suggestions

- The reset signal is a sensitive signal and can be processed in a package or away from signals with greater interference ;
- Place the reset signal TVS tube as close to the button as possible.

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5.8.Display Interface

The ECK10-135D series core board provides a 24-bit parallel digital RGB display interface, supporting resolutions up to WXGA (1366×768 @ 60fps) or Full HD (1920×1080 @ 30fps), a maximum pixel clock of 90MHz, and support for RGB888, RGB666, RGB565, RGB332, and YUV422 data formats. It also provides the signals required for all LCD and TFT displays. Customers can configure the display resolution and data format according to their needs. The ECK10-131D series core board does not support RGB functionality.

In LCD and TFT screen applications, GPIO can be used to control screen power and backlight power. PWM output can be used to control backlight brightness. I2C and GPIO external interrupt functions can also be used to connect to the touch screen. Related reference interface definition

See Display Interface Reference Definition Table.

Table 5-11 shows the interface reference definition table

Gold finger pin	MPU I/O pins	Function	Length (mil)
46	PH9	LCD_DE	1229.13
92	PD9	LCD_CLK	1297.46
82	PG4	LCD_VSYNC	1207.24
66	PE9	LCD_HSYNC	1240.95
75	PA15	LCD_R0	1214
70	PD4	LCD_R1	1208.35
76	PG7	LCD_R2	1209.49
48	PB12	LCD_R3	1222.85
81	PD14	LCD_R4	1220.99
98	PE7	LCD_R5	1213.42
103	PH8	LCD_R6	1198.97
22	PD11	LCD_R7	1356.27
87	PE14	LCD_G0	1266.91
108	PH2	LCD_G1	1231.72
73	PD1	LCD_G2	1247.67
42	PF3	LCD_G3	1207.01
116	PD13	LCD_G4	1206.69
100	PD10	LCD_G5	1262.25
79	PE12	LCD_G6	1252.47
151	PE4	LCD_G7	1231.73
72	PD5	LCD_B0	1201.29

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85	PE13	LCD_B1	1215.88
122	PH7	LCD_B2	1200.18
114	PF8	LCD_B3	1200.43
144	PH3	LCD_B4	1199.5
94	PD15	LCD_B5	1213.05
twenty four	PB6	LCD_B6	1211.95
74	PE15	LCD_B7	1208.15

5.8.1. LAYOUT Suggestions

- If the baseboard LCD signal is designed with a series matching resistor , it is recommended to place it close to the core board gold finger connector ;
- The LCD signal has been processed into equal length in the core board. The length of the trace in the core board is shown in the pin definition table;
- signal in the core board is controlled according to the single-ended 50Ω ±10% impedance. It is recommended that the impedance control of the baseboard remain consistent.
- It is recommended that the LCD signal traces on the baseboard be aligned with the LCD_CLK clock signal for equal length control, with an error range of ± 100 mil and a minimum spacing of 3 mils between signal traces .

5.9.Digital camera interface

The ECK10-135D series core board supports a single DCMIPP digital camera interface. It supports a 120MHz pixel clock and an 8-bit, 10-bit, 12-bit, 14-bit, or 16-bit parallel interface. This camera interface consumes a large number of I/O pins in an application, reducing the availability of other functions. Therefore, it is recommended to use a USB camera for camera functionality. The ECK10-131D series core board does not support the digital camera interface.

5.10.USB interface

The ECK10-13xD series core boards integrate a USB hub chip, providing up to four USB 2.0

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interfaces. One USB_OTG_HS_DP/USB_OTG_HS_DN interface supports OTG functionality, and the remaining three interfaces support USB 2.0 host functionality. The core board also exposes the OTG_HS_VBUS signal, which can be used to detect host or device mode in software when using the OTG interface. If the OTG_HS_VBUS function is not used, this pin can also be used as a GPIO.

5.10.1. USB pin definition

Table 5-12 USB interface signal pin definitions

Gold finger pin	MPU I/O pins	Function	Length (mil)
twenty one	PI7	OTG_HS_VBUS	2897.48
27	USB_DP2	USB_OTG_HS_DP	1806.83
29	USB_DM2	USB_OTG_HS_DN	1807.43
35	/	HOST1_USB_DP	1810.03
37	/	HOST1_USB_DN	1809.93
43	/	HOST2_USB_DP	1779.51
45	/	HOST2_USB_DN	1779.23
51	/	HOST3_USB_DP	1845.16
53	/	HOST3_USB_DN	1845.11

5.10.2. LAYOUT 建议

- The USB signal traces are of equal length , with an intra-differential pair error of ± 20 mil and a spacing of more than 3W between adjacent differential pairs.
- is controlled to 90Ω ±10% .

5.11.Ethernet interface

The ECK10-131D series core board provides one Ethernet MAC/GMAC supporting the IEEE 1588v2 standard and MII/RMII/RGMII interfaces . The ECK10-135D series core board supports two Ethernet MAC/GMAC supporting the IEEE 1588v2 standard and MII/RMII/RGMII interfaces .

Typically, an RJ45 Ethernet interface is mainly composed of an Ethernet controller MAC

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(Media Access Control), an Ethernet physical layer interface PHY (Physical Layer), an Ethernet transformer, and an RJ45 connector, as shown in the figure below.

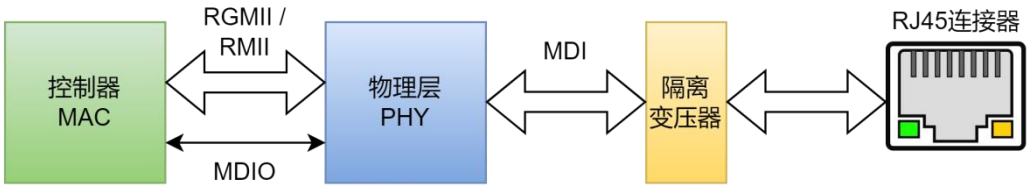


Figure 5.12 RJ45 Ethernet components

The ECK10-13xD series core boards do not have an Ethernet PHY circuit built into them. Instead, they provide as many GPIO ports as possible. To use Ethernet functionality, users must design a PHY interface chip circuit on the baseboard. For information on baseboard PHY interface chip circuit design, refer to the ECB10-PGD-I product drawing.

5.11.1. Pin Definition

Table 5-13 Recommended pin definitions for Ethernet interface signals

Gold finger pin	MPU I/O pins	Function	Length (mil)	illustrate
135	PA2	ETH1_MDIO	653.53	
134	PG2	ETH1_MDC	624.2	
133	PA1	ETH1_RGMII_RX_CLK	1013.18	
172	PA7	ETH1_RGMII_RX_CTL	1024.1	
147	PC4	ETH1_RGMII_RXD0	979.23	
156	PC5	ETH1_RGMII_RXD1	952.79	
177	PB0	ETH1_RGMII_RXD2	1066.82	
178	PB1	ETH1_RGMII_RXD3	1076.12	
181	PC1	ETH1_RGMII_GTX_CLK	1142.53	
129	PB11	ETH1_RGMII_TX_CTL	1096.68	
158	PG13	ETH1_RGMII_TXD0	1137.92	
184	PG14	ETH1_RGMII_TXD1	1207.18	
186	PC2	ETH1_RGMII_TXD2	1231.64	
183	PE5	ETH1_RGMII_TXD3	1192.3	
126	PB2	ETH2_MDIO	738.56	ECK10-131D series core boards do not support this function
120	PG5	ETH2_MDC	674.41	
162	PH11	ETH2_RGMII_RX_CLK	1066.61	
153	PA12	ETH2_RGMII_RX_CTL	1019.42	
150	PF4	ETH2_RGMII_RXD0	983.88	
121	PA11	ETH2_RGMII_RXD1	976.97	

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128	PH6	ETH2_RGMII_RXD2	996.07	
105	PA8	ETH2_RGMII_RXD3	1003.17	
117	PG3	ETH2_RGMII_GTX_CLK	691.27	
112	PF6	ETH2_RGMII_TX_CTL	656.98	
109	PF7	ETH2_RGMII_TXD0	612.76	
111	PG11	ETH2_RGMII_TXD1	600.28	
115	PG1	ETH2_RGMII_TXD2	600.79	
146	PE6	ETH2_RGMII_TXD3	782.57	

5.11.2. LAYOUT 建议

- RGMII signal TX and RX are respectively referenced to the CLK clock signal for group equal length control, with an error of ± 100 mil and a line spacing of more than 3W ;
- The network differential signal impedance is controlled at 100Ω ±10% , the length of the differential pair is controlled to be equal, the error is ± 20 mil, and the spacing between adjacent differential pairs is more than 3W;
- The network port transformer should be placed close to the PHY chip, with a recommended distance of no more than 20 mm.
- The decoupling capacitors for the power pins of the PHY chip should be placed close to the PHY chip;

5.12.WiFi/Bluetooth

The ECK10-13x D series core board integrates Wi-Fi and Bluetooth modules, including the Ebyte WM103-WF8723DU high-performance Wi-Fi + BT dual-mode module. This module utilizes USB 2.0 communication, complies with IEEE 802.11b/g/n standards and Bluetooth 4.2, and offers a maximum data rate of 150 Mbps. For more information, refer to the EWM103-WF8723DU User Manual.

The core board provides a WiFi/Bluetooth antenna interface using an IPX micro RF connector. Users can connect to a WiFi/Bluetooth dedicated antenna with an operating frequency band of 2.4GHz to 2.484GHz.

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5.13.Audio Interface

The STM32MP13 series processors provide a variety of audio interface types. The ECK10-13xD series core boards recommend using the I2S audio interface. When using the I2S interface signal to implement audio functions, an external audio codec is required to implement audio interface functions such as headphones, microphones, and speakers through the codec.

5.14.UART interface

The ECK10-13x D series core board supports up to 4 UART interfaces and 4 USART interfaces. By default, the core board uses UART 4 as the debug serial port.

5.15.SPI interface

The ECK10-13xD series core board provides one QSPI interface for BOOT to facilitate users' use of various BOOT modes. In addition, it supports up to five SPI interfaces.

5.16.CAN interface

The ECK10-135D series core board supports up to two CAN bus functions (not supported by the STM32MP131 series). The CAN bus of the ECK10-135D series core board uses TTL signals and requires an external CAN interface chip to implement the final CAN bus interface function.

5.16.1. CAN pin definition

Table 5-14 USB interface signal pin definition

Gold finger pin	MPU I/O pins	Function	Length (mil)	Illustrate
106	PG9	FDCAN1_TX	532.46	
16	PG10	FDCAN1_RX	1514.22	
64	PG0	FDCAN2_TX	1951.66	
59	PE0	FDCAN2_RX	786.54	

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5.17.I2C interface

The ECK10-13xD series core board supports up to 5 I2C buses. Several devices can be connected to the same I2C bus. When designing the schematic, please note the following points:

a) Check whether the device addresses on the same bus conflict;

b) Ensure that each I2C bus has a pair of pull-up resistors. The recommended resistance is 2.2K~10K, but do not add multiple resistors.

c) The core board does not provide an I2C bus pull-up resistor, so the user needs to pull it up when using the baseboard;

d) Check whether the I2C interface voltage level of the device is 3.3V. If not, a level conversion circuit needs to be added;

e) Check whether the I2C interface power rails are consistent. When interconnecting I2C interfaces in different time domains, the bus switching circuit needs to be considered;

f) Do not use too many devices on the same bus; otherwise, the load capacitance limit of 400pF required by the I2C specification may be exceeded, affecting the signal waveform.

5.18.GPIO interface

The ECK10-13xD series core boards provide a maximum of 117 GPIO interfaces, most of which are reused. Users can flexibly configure the GPIOs based on their needs.

5.19.Hardware design checklist

- Power rails: Check if there are inconsistent power rails in the I/O interface application, such as connecting a 1.8V signal to a 3.3V signal. If there is a need to connect signals with different power rails, use a level conversion circuit.
- Power-on sequence: Check the signals connecting the baseboard and core board to see if the baseboard signal is powered on first, or if there is a significant difference in the power-on time between the two board signals.

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- Pull-up and pull-down resistors: Multiplexed I/O interfaces may have uncertain output states before power-up software configuration. If signals need to maintain a defined level during power-up, pull-up and pull-down resistors should be designed on the baseboard. Some functional signals, such as I2C signals, also require pull-up or pull-down resistors on the baseboard. When designing pull-up resistors, pay attention to the design of the pull-up power rail.
- ESD protection: Corresponding ESD protection design should be considered for external interface signals. The selection of ESD solution should take into account the requirements of signal rate, communication protocol and application environment.
- Equal length of high-speed signals: High-speed signals should consider equal length design of PCB, including USB, Ethernet, SDMMC, display, etc.
- Impedance control: High-speed signals should consider PCB impedance control. The key to impedance control is to maintain impedance continuity. The baseboard should be designed with reference to the impedance of the core board signal.

6. Software Resources

The ECK10-13xD core board runs an operating system based on the Linux 5.15 kernel. It also ships with a cross-compilation toolchain for embedded Linux system development, along with TF-A source code, Optee-OS source code, U-boot source code, the source code for the Linux kernel and various driver modules, and various development and debugging tools for both Windows and Linux desktop environments.

operating system:

Ubuntu 18.04 system

System source code:

TF-A 2.6

Op-tee 3.16

U-boot 2021.10

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Kernel 5.15.67

BuildRoot 2022.02.3

Development environment and IDE:

Burning tool: STM32CubeProgrammer

Development tool: STM32CubeMX

System software resources are shown in the following table:

Table 6-1 System software resources

Category	Name	Description	Source code
F SBL	T FA	First-stage bootloader	/ source/tf- a.tar.g z
S SBL	Op-tee	Second stage bootloader	/source/optee.tar.gz
S SBL	U-boot	Second stage bootloader	/source/u-boot.tar.gz
Linux kernel	Kernel	Linux kernel	/ source/linux . tar.gz
Devic e D river	USB Host	USB Host	kernel/
	USB OTG	USB OTG	kernel/
	I2C	I2C bus driver	kernel/
	S PI	S PI bus driver	kernel
	T TY	TT serial port driver	kernel
	R S232	TTY serial port driver	kernel
	R S485	TTY serial port driver	kernel
	C AN	CAN bus driver	kernel
	Ethernet	10M/100M/1000M drivers	kernel
	M MC	eMMC/TF card storage driver	kernel
	N AND	Nand Flash storage driver	kernel
	L CD	RGB display driver	kernel
	P WM	PWM control drive	kernel
	A DC	ADC Driver	kernel
	R TC	Real-time clock driver	kernel
	G PIO	GPIO Driver	kernel
	Touch	Capacitive touch driver	kernel
	Watchdog	Watchdog Driver	kernel
Operating system	R ootfs	Buildroot system Ubuntu 18.04 system	/images/rootfs.ext4 /images/ubuntu-1804.ext4
Developm ent Tools	Building R oot	Operating system build	/source /ebyte-mp135-sdk-buildroot.tar.gz
	S DK	arm-ostl-linux-gnueabi-gcc	/tools/SDK-x86_64-stm32mp1-openst

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		11.3	linux.tar.gz
	STM32CubeProgrammer	Burning Tools	/ tools/SetupSTM32CubeProgrammer-2.5.0.exe
	S TM32C ube MX	Resource allocation tools	/tools/en.stm32cubemx_v6-0-1.zip
	Win32DiskImager	Make SD card boot tool	/tools/Win32DiskImager-1.0.0-binary

7. Structural dimensions

The ECK10-13xD series core boards utilize a 204-pin, DDR3 gold finger interface for easy installation and removal. The core boards include two 2.2mm mounting holes for securing the core boards. Detailed dimensions can be found in the ECK10-13xD_2D_V1.0.dxf file. See the figure below for the core board dimensions.

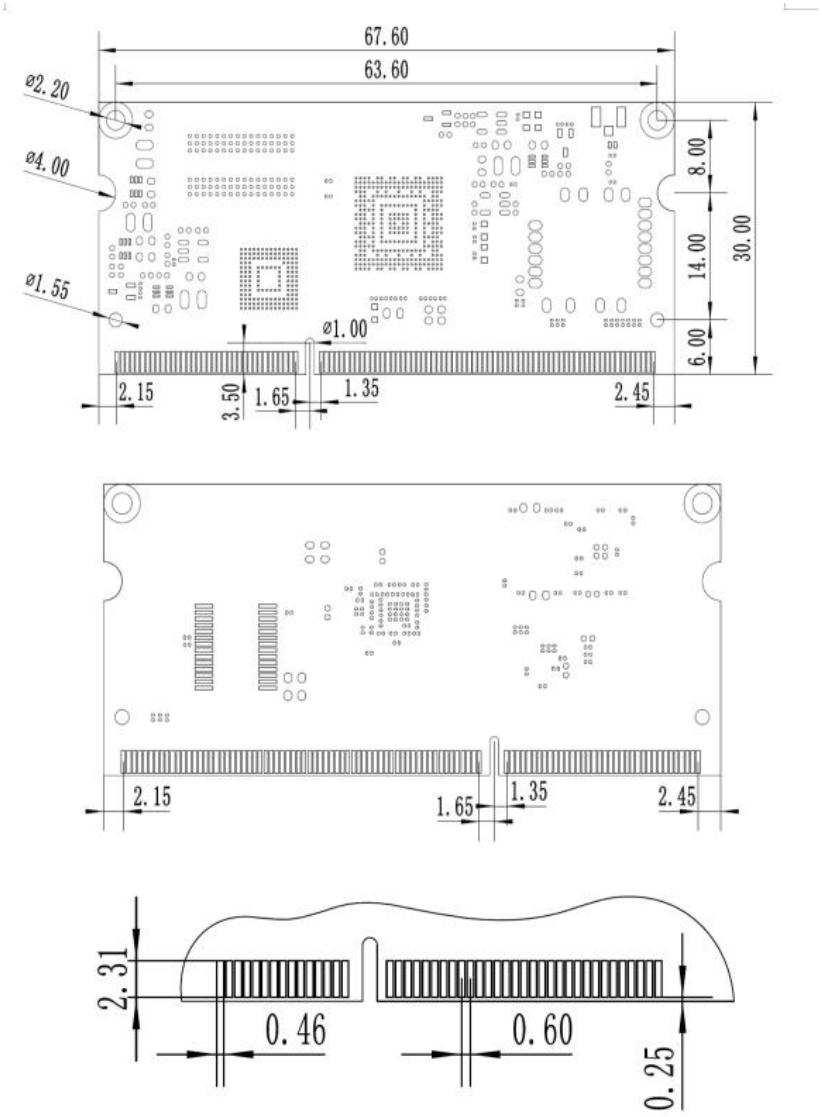


Figure 7.1 Core board structure dimensions

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8. Reference Documentation

STM32MP131DAF7 Datasheet.pdf

STM32MP135DAF7 Datasheet .pdf

EWM103-WF8723DU_UserManual_CN_v1.0.pdf

9. Revision Notes

Table 9-1 Revision Description Table

Version	Modifications	Modification time	Prepared by	Proof reading	Approval
V1.0	First Draft	25-08-18	WJ	LQ	WFX
V1.1	Revise the processor model in Product Function Table 4-1	26-06-29	WJ	LQ	WFX

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