Product Manual

ECK10-13xA Core Board



Chengdu Ebyte Electronic Technology Co.,Ltd.

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1、Product description

1.1. Product description

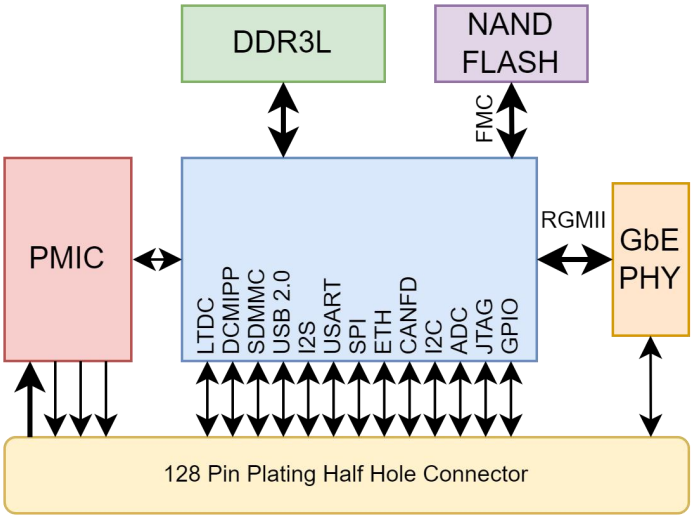
The ECK10-13xA series core board of Ebyte is a low-cost, low-power, cost-effective and highly reliable embedded core board designed based on the STM32MP13 series processor launched by STMicroelectronics.

STMicroelectronics' STM32MP13 series processor uses a single ARM Cortex-A7 core with a maximum main frequency of 1000MHz, which can provide rich I/O resources such as 1 LCD display, 1 digital camera, 2 Gigabit Ethernet controllers, 2 USBs, 8 UARTs, 2 SDIOs, 2 CANs, and multiple GPIOs.

The ECK10-13xA series core board is centered on the STM32MP13 series processor, and the power supply circuit, DDR3L memory circuit, NAND FLASH storage circuit, and Gigabit Ethernet PHY circuit are designed on the board to minimize the difficulty and cost of user baseboard design.

The ECK10-13xA series core board includes a variety of product models. They have some differences in storage configuration, and customers can choose the appropriate model according to their needs. For product model selection, please refer to the product selection section for details.

The core board functional block diagram is as follows:



Core board functional block diagram

The physical picture of the core board is as follows:

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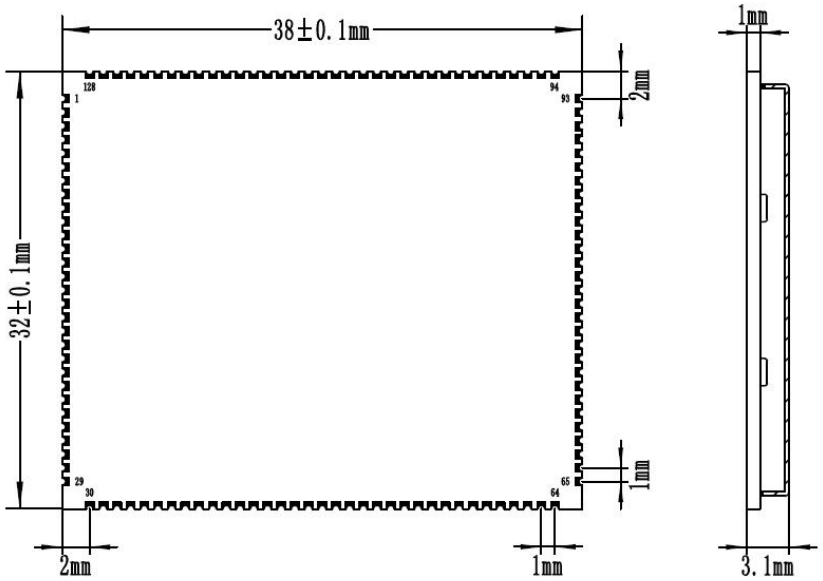


Core board physical picture

1.2. Features

1. Processor: STM32MP13 series processor, main frequency 650MHz;
2. Memory: On-board DDR3L SDRAM, 256MB/512MB capacity optional;
3. Storage: 256MB/512MB parallel NAND FLASH optional;
4. Display: 1 parallel display interface, maximum resolution supports WXGA (1366×768@60fps);
5. Network: 1 Gigabit Ethernet electrical port and 1 Gigabit Ethernet MAC, support RGMII interface;
6. USB: 1 USB2.0 OTG interface and 1 USB2.0 HOST interface;
7. SDMMC: 2-way MMC/SD/SDIO card interface;
8. Multiple extended I/O interfaces: including UART, CAN, I2C, SPI, SAI, ADC, GPIO, etc.;
9. Support on-chip watchdog function;
10. Support on-chip RTC function;
11. Interface: 128-pin stamp hole;
12. Power input: single-channel DC +5V±10% power input;
13. Power output: 1-way 3.3V switching power output, 2-way software programmable LDO power output;
14. Size: 38 x 32 x 3.1mm, as shown in the figure below:

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Dimensions

15. Operating temperature: -40℃-85℃ (industrial grade), 0℃-70℃ (commercial grade);

16. PCB process: 8-layer board design, immersion gold, lead-free process;

17. SBC board: ECB10-135A5M5M-I;

1.3. Typical application

- Smart home;
- Smart toys;
- Smart City;
- tablet ;
- IoT Gateway
- Advertising all-in-one machine ;
- Industrial all-in-one machine ;
- Industrial control motherboard;
- Robots and drones.

2. Quick experience

Choose the ECB10-135A5M5M-I series single board computer products to quickly experience the typical application functions of the ECK10-13xA series core board products.

3. Specifications

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3.1. Product Features

Function Table

processor	STM32MP131AAF3 / STM32MP135AAF3; Single Arm Cortex-A7 core, 650MHz;	
storage	Memory	On-board DDR3L SDRAM, 16-bit width, 256MB/512MB optional;
	FLASH	On-board 256MB/512MB parallel NAND FLASH optional;
show	1 parallel display interface, maximum resolution supports WXGA (1366×768@60fps) (supported only by MP135); Support 24bit, 18bit, 16bit, 8bit parallel display output;	
Camera	1 digital camera input (only supported by MP135);	
SDMMC	2 (maximum) BOOT-capable MMC/SD/SDIO card interfaces;	
USB	2 USB 2.0 ports or 1 USB2.0 port + 1 OTG port;	
Audio	4-way (maximum) I2S full-duplex;	
Serial Port	4-channel (maximum) UART; 3-way (maximum) USART;	
SPI	1-way BOOT-capable QSPI; 5-way (maximum) SPI;	
Ethernet	2 (maximum) Ethernet MAC, 1 10/100/1000 Ethernet PHY on board;	
CAN	2-channel (maximum) FDCAN (supported only by MP135);	
I2C	4-way (maximum) I2C;	
ADC	Supports up to 8 (maximum) 12-bit ADC input channels;	
JTAG	Support System JTAG Controller;	
GPIO	86 (maximum) GPIO, supporting interrupt function;	
Power Output	1 3.3V power output, maximum current 1A; 1 PMIC LDO1 software adjustable voltage (1.7-3.0V) power output, maximum current 350mA; 1 PMIC LDO2 software adjustable voltage (1.7-3.0V) power output, maximum current 350mA;	

3.2. Environmental characteristics

Environmental characteristics table

Operating temperature	Commercial Grade	0℃ ~ 70℃;
	Industrial Grade	-40℃ ~ 85℃;
Storage temperature	-40℃ ~ 85℃;	
Working humidity	5~95% humidity, non-condensing;	
Storage humidity	60℃@95% humidity, non-condensing;	

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3.3. I/O Features

3.3.1. Pin Definition

Pin Definition Table

Pinout	Pin Name	Chip Pins	Level	type	Trace length	illustrate
1	DGND			PWR		
2	GPIO_PF2	MPU.PF2	3.3V	I/O	1115.35	
3	GPIO_PH13	MPU.PH13	3.3V	I/O	1130.81	
4	GPIO_PB5	MPU.PB5	3.3V	I/O	1145.64	
5	GPIO_PB9	MPU.PB9	3.3V	I/O	1076.5	
6	GPIO_PC7	MPU.PC7	3.3V	I/O	1118.04	
7	GPIO_PF3	MPU.PF3	3.3V	I/O	1110.54	
8	GPIO_PH9	MPU.PH9	3.3V	I/O	1131.18	
9	GPIO_PF1	MPU.PF1	3.3V	I/O	1112.99	
10	DGND			PWR		
11	GPIO_PE1	MPU.PE1	3.3V	I/O	1071.26	
12	GPIO_PD10	MPU.PD10	3.3V	I/O	1067.91	
13	GPIO_PD9	MPU.PD9	3.3V	I/O	1079.89	
14	GPIO_PH14	MPU.PH14	3.3V	I/O	1085.84	
15	GPIO_PG0	MPU.PG0	3.3V	I/O	1072.7	
16	GPIO_PA15	MPU.PA15	3.3V	I/O	1096.22	
17	GPIO_PB8	MPU.PB8	3.3V	I/O	1089.73	
18	GPIO_PH12	MPU.PH12	3.3V	I/O	1101.75	
19	GPIO_PA12	MPU.PA12	3.3V	I/O	1110.43	
20	DGND			PWR		
twenty one	GPIO_PB12	MPU.PB12	3.3V	I/O	1112.35	
twenty two	GPIO_PG7	MPU.PG7	3.3V	I/O	1131.52	
twenty three	GPIO_PG4	MPU.PG4	3.3V	I/O	1118.8	
twenty four	GPIO_PE15	MPU.PE15	3.3V	I/O	1123.52	
25	GPIO_PG15	MPU.PG15	3.3V	I/O	1151.23	
26	GPIO_PG8	MPU.PG8	3.3V	I/O	1089.58	
27	GPIO_PH8	MPU.PH8	3.3V	I/O	1150.65	
28	GPIO_PF6	MPU.PF6	3.3V	I/O	1087.99	
29	DGND			PWR		
30	DGND			PWR		
31	GPIO_PH11	MPU.PH11	3.3V	I/O	1104.47	
32	GPIO_PD13	MPU.PD13	3.3V	I/O	1095.39	

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33	GPIO_PE12	MPU.PE12	3.3V	I/O	1115.52	
34	GPIO_PE11	MPU.PE11	3.3V	I/O	1108.1	
35	GPIO_PE13	MPU.PE13	3.3V	I/O	1095.81	
36	GPIO_PF5	MPU.PF5	3.3V	I/O	1100.05	
37	GPIO_PD3	MPU.PD3	3.3V	I/O	1097.97	
38	GPIO_PD6	MPU.PD6	3.3V	I/O	1113.25	
39	DGND			PWR		
40	GPIO_PB6	MPU.PB6	3.3V	I/O	1092.06	
41	GPIO_PE0	MPU.PE0	3.3V	I/O	1119.28	
42	GPIO_PD8	MPU.PD8	3.3V	I/O	1142.54	
43	VBAT_EXT	MPU.VBAT	3.3V	PWR-I		
44	QSPI_CLK_PF10_R	MPU.PF10	3.3V	I/O	810.44	Connect a 22 ohm resistor in series
45	QSPI_BK2_IO0_PH2	MPU.PH2	3.3V	I/O	744.04	
46	QSPI_BK2_IO1_PG10	MPU.PG10	3.3V	I/O	766.74	
47	DGND			PWR		
48	QSPI_BK2_IO2_PE14	MPU.PE14	3.3V	I/O	771.63	
49	QSPI_BK2_NCS_PE4	MPU.PE4	3.3V	I/O	789.01	
50	QSPI_BK2_IO3_PH7	MPU.PH7	3.3V	I/O	723.97	
51	GPIO_PG3	MPU.PG3	3.3V	I/O	1102.96	
52	GPIO_PA11	MPU.PA11	3.3V	I/O	1104.08	
53	GPIO_PA0	MPU.PA0	3.3V	I/O	1095.1	
54	GPIO_PF13	MPU.PF13	3.3V	I/O	1121.18	
55	DGND			PWR		
56	GPIO_PA1	MPU.PA1	3.3V	I/O	1120.32	
57	GPIO_PG11	MPU.PG11	3.3V	I/O	1086.64	
58	GPIO_PG1	MPU.PG1	3.3V	I/O	1066.09	
59	GPIO_PA8	MPU.PA8	3.3V	I/O	1141.64	
60	GPIO_PE6	MPU.PE6	3.3V	I/O	1072.64	
61	GPIO_PH3	MPU.PH3	3.3V	I/O	1096.77	
62	GPIO_PF9	MPU.PF9	3.3V	I/O	1138.68	
63	GPIO_PA13	MPU.PA13	3.3V	I/O	1088.44	
64	GPIO_PC0	MPU.PC0	3.3V	I/O	1164.76	
65	JTCK_SWCLK_PF14	MPU.PF14	3.3V	I/O	1132.23	
66	GPIO_PA4	MPU.PA4	3.3V	I/O	1090.07	
67	GPIO_PC3	MPU.PC3	3.3V	I/O	1099.8	
68	GPIO_PA5	MPU.PA5	3.3V	I/O	1086.04	
69	GPIO_PA3	MPU.PA3	3.3V	I/O	1077.51	
70	ETH1_LEDG	PHY.33	3.3V	O		4.7K pull-down
71	ETH1_LEDY	PHY.34	3.3V	O		4.7K pull-down
72	JTRST_NJTRST	MPU.NJTRST	3.3V	I	1153.19	
73	GPIO_PA6	MPU.PA6	3.3V	I/O	1119.88	
74	GPIO_PI6-BOOT2	MPU.PI6	3.3V	I/O	1109.19	On-chip pull-down

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75	DGND			PWR		
76	USBH_HS1_DM	MPU.USB_DM1	USB	I/O	923.39	
77	USBH_HS1_DP	MPU.USB_DP1	USB	I/O	922.36	
78	DGND			PWR		
79	USB_OTG_HS_DM	MPU.USB_DM2	USB	I/O	904.81	
80	USB_OTG_HS_DP	MPU.USB_DP2	USB	I/O	904.27	
81	DGND			PWR		
82	ETH1_MDIN2	PHY.MDIN2	ETH	I/O	882.82	
83	ETH1_MDIP2	PHY.MDIP2	ETH	I/O	881.92	
84	DGND			PWR		
85	ETH1_MDIN0	PHY.MDIN0	ETH	I/O	894.9	
86	ETH1_MDIP0	PHY.MDIP0	ETH	I/O	895.92	
87	DGND			PWR		
88	ETH1_MDIN1	PHY.MDIN1	ETH	I/O	865.31	
89	ETH1_MDIP1	PHY.MDIP1	ETH	I/O	866.58	
90	DGND			PWR		
91	ETH1_MDIN3	PHY.MDIN3	ETH	I/O	890.17	
92	ETH1_MDIP3	PHY.MDIP3	ETH	I/O	888.93	
93	DGND			PWR		
94	JTDO_SWO_PH5	MPU.PH5	3.3V	I/O	1173.71	
95	JTDI_PH4	MPU.PH4	3.3V	I/O	1143.64	
96	GPIO_PI4-BOOT0	MPU.PI4	3.3V	I/O	1164.07	On-chip pull-down
97	OTG_VBUS_PI7	MPU.PI7	3.3V	I/O	1025.11	
98	JTMS_SWDIO_PF15	MPU.PF15	3.3V	I/O	1223.66	
99	GPIO_PA14	MPU.PA14	3.3V	I/O	1147.88	
100	GPIO_PI5-BOOT1	MPU.PI5	3.3V	I/O	1099.46	On-chip pull-down
101	DGND			PWR		
102	SDMMC2_CMD_PG6	MPU.PG6	3.3V	I/O	1405.41	
103	SDMMC2_CK_PE3_R	MPU.PE3	3.3V	I/O	1433.22	Connect a 22 ohm resistor in series
104	SDMMC2_D3_PB4	MPU.PB4	3.3V	I/O	1465.48	
105	SDMMC2_D0_PB14	MPU.PB14	3.3V	I/O	1453.64	
106	SDMMC2_D2_PB3	MPU.PB3	3.3V	I/O	1457.94	
107	DGND			PWR		
108	SDMMC2_D1_PB15	MPU.PB15	3.3V	I/O	1427.23	
109	SDMMC1_CMD_PD2	MPU.PD2	3.3V	I/O	1403.51	
110	SDMMC1_D3_PC11	MPU.PC11	3.3V	I/O	1395.3	
111	SDMMC1_D1_PC9	MPU.PC9	3.3V	I/O	1396.27	
112	SDMMC1_D0_PC8	MPU.PC8	3.3V	I/O	1406.37	
113	SDMMC1_D2_PC10	MPU.PC10	3.3V	I/O	1412.57	
114	DGND			PWR		
115	SDMMC1_CK_PC12_R	MPU.PC12	3.3V	I/O	1390.97	Connect a 22 ohm resistor in series

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116	GPIO_PH10	MPU.PH10	3.3V	I/O	1145.61	
117	GPIO_PB10	MPU.PB10	3.3V	I/O	1068.7	
118	GPIO_PB13	MPU.PB13	3.3V	I/O	1073.64	
119	GPIO_PC6	MPU.PC6	3.3V	I/O	1080.43	
120	GPIO_PF0	MPU.PF0	3.3V	I/O	1086.14	
121	P_LDO1_R0	PMIC.LDO1	3.3V	PWR- O		
122	P_LDO2_R0	PMIC.LDO2	3.3V	PWR- O		
123	NRST_CPU	MPU.NRST	3.3V	I		10K pull-up
124	P3V3_OUT_R2	PMIC.BUCK4	3.3V	PWR- O		Series magnetic beads
125	P3V3_OUT_R2	PMIC.BUCK4	3.3V	PWR- O		Series magnetic beads
126	PMIC_PONKEY	PMIC.PON	5.0V	I		On-chip pull-up
127	VIN_5V		5.0V	PWR-I		
128	VIN_5V		5.0V	PWR-I		

Note: The unit of trace length is mil, and the trace impedance of single-ended signal is 55 ohms.

3.3.2. Differential routing

Differential trace impedance control table

Pin out	Pin Name	Trace length	Impedance Control	illustrate
76 / 77	USBH_HS1_DM / USBH_HS1_DP	923.39 / 922.36	90 ohm	USB Signal
79 / 80	USB_OTG_HS_DM / USB_OTG_HS_DP	904.81 / 904.27	90 ohm	USB Signal
82 / 83	ETH1_MDIN2 / ETH1_MDIP2	882.82 / 881.92	100 ohm	Ethernet signal
85 / 86	ETH1_MDIN0 / ETH1_MDIP0	894.9 / 895.92	100 ohm	Ethernet signal
88 / 89	ETH1_MDIN1 / ETH1_MDIP1	865.31 / 866.58	100 ohm	Ethernet signal
91 / 92	ETH1_MDIN3 / ETH1_MDIP3	890.17 / 888.93	100 ohm	Ethernet signal

3.4. Electrical characteristics

3.4.1. Power consumption

Power Consumption Table

Power Status	test environment	voltage	Typical current	Power consumption
PWRUP	BOOT stage	5.0V	0.24	1.2W
PWRUP	System LOAD completed	5.0V	0.19A	0.95W
PWRUP	Software reload testing	5.0V	0.28A	1.4W
SLEEP	Standby to Memory	5.0V	0.1A	0.5W
PWRDN	VBAT_EXT power supply	3.2V	5.8uA	

Note: The power consumption measurement does not include the power consumption of the core board's external output power supply.

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4. Core board hardware design

4.1. processor

4.1.1. STM32 MP131 processor

Table 1. STM32MP131A/D features and peripheral counts

Features			STM32MP131AAE STM32MP131DAE	STM32MP131AAG STM32MP131DAG	STM32MP131AAF STM32MP131DAF	Miscellaneous
			LFBGA289	TFBGA289	TFBGA320	
Package		Body size (mm)	14x14	9x9	11x11	-
		Pitch (mm)	0.8	0.5	0.5	
		Ball size (mm)	0.40	0.30	0.30	
		Thickness (mm)	< 1.4	< 1.2	< 1.2	
		Ball count	289	289	320	
CPU			Cortex-A7 FPU Neon TrustZone			-
		Caches size	32-Kbyte L1 data cache			
			32-Kbyte L1 instruction cache			
			128-Kbyte L2 unified coherent cache			
		Frequency	STM32MP131A: 650 MHz STM32MP131D: 1 GHz			
ROM			128 Kbytes (secure)			-
Embedded SRAM		System RAM	128 Kbytes (securable)			168 Kbytes
		Backup	8 Kbytes (securable, tamper protected)			
		AHB SRAM	32 Kbytes			
SDRAM			Securable			-
	LPDDR2/3	16-bit 533 MHz	Up to 1 Gbyte, single rank			
	DDR3/3L	16-bit 533 MHz				
Backup registers			128 bytes (32x32-bit, securable, tamper protected)			-
Timers	Advanced	16 bits	2			24 timers
	General purpose	16 bits	8 (6 securable)			
		32 bits	2			
	Basic	16 bits	2			
	Low power	16 bits	5 (2 securable)			
	A7 timers	64 bits	4 (secure, non-secure, virtual, hypervisor)			
	RTC/AWU		1 (securable)			

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Table 1. STM32MP131A/D features and peripheral counts (continued)

Features			STM32MP131AAE STM32MP131DAE	STM32MP131AAG STM32MP131DAG	STM32MP131AAF STM32MP131DAF	Miscellaneous
			LFBGA289	TFBGA289	TFBGA320	
Watchdogs			2 (independent, independent secure)			-
Communication peripherals	SPI		5 (2 securable)			-
		Having I2S	4			
	I2C (with SMB/PMB support)		5 (3 securable)			
	USART (smartcard, SPI, IrDA, LIN) + UART (IrDA, LIN)		4 + 4 (including 2 securable USART), some can be a boot source			Boot
	SAI		2 (up to 4 audio channels), with I2S master/slave, PCM input, SPDIF-TX			-
	USB	EHCI/OHCI Host	2 ports			-
			Embedded HSPHY with BCD			
		OTG HS	Embedded HS PHY with BCD (securable), can be a boot source			Boot
		Embedded PHYs	2 × HS shared between Host and OTG			-
	SPDIFRX		4 inputs			-
SDMMC (SD, SDIO, e•MMC)			2 (8 + 8 bits) (securable), e•MMC or SD can be a boot source 2 optional independant power supplies for SD card interfaces			Boot
QUADSPI			1 (dual-quad) (securable), can be a boot source			Boot (1)
FMC	Parallel address/data 8/16-bit		4 × CS, up to 4 × 64 Mbyte			-
	Parallel AD-mux 8/16-bit					
	NAND 8/16-bit		Yes, 2× CS, SLC, BCH4/8, can be a boot source			Boot
10/100M/Gigabit Ethernet			1 x (MII, RMI, RGMII) with PTP and EEE (securable)			-
DMA			3 instances (1 secure), 33-channel MDMA			-
Hash			SHA-1, SHA-224, SHA-256, SHA-384, SHA-512, SHA-3, HMAC (securable)			-
True random number generator			True-RNG (securable)			-
Fuses (one-time programmable)			3072 effective bits (secure, 1280 bits available for the user)			-
GPIOs with interrupt (total count)			135(2)			-
	Securable GPIOs		All			
	Wakeup pins		6			
	Tamper pins (active tamper)		12 (5)			

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Table 1. STM32MP131A/D features and peripheral counts (continued)

Features		STM32MP131AAE STM32MP131DAE	STM32MP131AAG STM32MP131DAG	STM32MP131AAF STM32MP131DAF	Miscellaneous
		LFBGA289	TFBGA289	TFBGA320	
DFSDM		4 input channels with 2 filters			-
Up to 12-bit synchronized ADC		1 (up to 5 Msps on 12-bit each) (securable)			-
	12-bit ADC channels in total(3)	ADC2: 18 channels including 6x internal, 12 channels available for user including 6x differential			
Internal ADC VREF		1.65 V, 1.8 V, 2.048 V, 2.5 V or VREF+ input			-
	VREF+ input pin	Yes			

4.1.2. STM32 MP13 5 processor

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Table 1. STM32MP135A/D features and peripheral counts

Features			STM32MP135AAE STM32MP135DAE	STM32MP135AAG STM32MP135DAG	STM32MP135AAF STM32MP135DAF	Miscellaneous
			LFBGA289	TFBGA289	TFBGA320	
Package		Body size (mm)	14x14	9x9	11x11	-
		Pitch (mm)	0.8	0.5	0.5	
		Ball size (mm)	0.40	0.30	0.30	
		Thickness (mm)	< 1.4	< 1.2	< 1.2	
		Ball count	289	289	320	
CPU			Cortex-A7 FPU Neon TrustZone			-
		Caches size	32-Kbyte L1 data cache			
			32-Kbyte L1 instruction cache			
			128-Kbyte L2 unified coherent cache			
		Frequency	STM32MP135A: 650 MHz STM32MP135D: 1 GHz			
ROM			128 Kbytes (secure)			-
Embedded SRAM		System RAM	128 Kbytes (securable)			168 Kbytes
		Backup	8 Kbytes (securable, tamper protected)			
		AHB SRAM	32 Kbytes			
SDRAM			Securable			-
	LPDDR2/3	16-bit 533 MHz	Up to 1 Gbyte, single rank			
	DDR3/3L	16-bit 533 MHz				
Backup registers			128 bytes (32x32-bit, securable, tamper protected)			-
Timers	Advanced	16 bits	2			24 timers
	General purpose	16 bits	8 (6 securable)			
		32 bits	2			
	Basic	16 bits	2			
	Low power	16 bits	5 (2 securable)			
	A7 timers	64 bits	4 (secure, non-secure, virtual, hypervisor)			
	RTC/AWU		1 (securable)			

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Table 1. STM32MP135A/D features and peripheral counts (continued)

Features			STM32MP135AAE STM32MP135DAE	STM32MP135AAG STM32MP135DAG	STM32MP135AAF STM32MP135DAF	Miscellaneous
			LFBGA289	TFBGA289	TFBGA320	
Watchdogs			2 (independent, independent secure)			-
Communication peripherals	SPI		5 (2 securable)			-
		Having I2S	4			
	I2C (with SMB/PMB support)		5 (3 securable)			
	USART (smartcard, SPI, IrDA, LIN) + UART (IrDA, LIN)		4 + 4 (including 2 securable USART), some can be a boot source			Boot
	SAI		2 (up to 4 audio channels), with I2S master/slave, PCM input, SPDIF-TX			-
	USB	EHCI/OHCI Host	2 ports			-
			Embedded HSPHY with BCD			
		OTG HS	Embedded HS PHY with BCD (securable), can be a boot source			Boot
		Embedded PHYs	2 × HS shared between Host and OTG			-
	SPDIFRX		4 inputs			-
	FDCAN		2 (1 × TTCAN), clock calibration, 10 Kbyte shared buffer			-
SDMMC (SD, SDIO, *e*•MMC)			2 (8 + 8 bits) (securable), *e*•MMC or SD can be a boot source 2 optional independant power supplies for SD card interfaces			Boot
QUADSPI			1 (dual-quad) (securable), can be a boot source			Boot (1)
FMC	Parallel address/data 8/16-bit		4 × CS, up to 4 × 64 Mbyte			-
	Parallel AD-mux 8/16-bit					
	NAND 8/16-bit		Yes, 2× CS, SLC, BCH4/8, can be a boot source			Boot
10/100M/Gigabit Ethernet			2 x (MII, RMI, RGMII) with PTP and EEE (securable)			-
LCD-TFT		Parallel interface	Up to 24-bit data, 1 secure layer, YUV on 1 layer (up to 1366×768 @ 60 fps) or up to Full HD (1920 x 1080) @ 30 fps Pixel clock up to 90 MHz			-
DMA			3 instances (1 secure), 33-channel MDMA			-
Hash			SHA-1, SHA-224, SHA-256, SHA-384, SHA-512, SHA-3, HMAC (securable)			-
True random number generator			True-RNG (securable)			-
Fuses (one-time programmable)			3072 effective bits (secure, 1280 bits available for the user)			-
Camera interface		Bus width	16-bit			-

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Table 1. STM32MP135A/D features and peripheral counts (continued)

Features		STM32MP135AAE STM32MP135DAE	STM32MP135AAG STM32MP135DAG	STM32MP135AAF STM32MP135DAF	Miscellaneous
		LFBGA289	TFBGA289	TFBGA320	
GPIOs with interrupt (total count)		135(2)			-
	Securable GPIOs	All			
	Wakeup pins	6			
	Tamper pins (active tamper)	12 (5)			
DFSDM		4 input channels with 2 filters			-
Up to 12-bit synchronized ADC		2(3) (up to 5 Msps on 12-bit each) (securable)			-
	12-bit ADC channels in total(4)	ADC1: 19 channels including 1x internal, 18 channels available for user including 8x differential ADC2: 18 channels including 6x internal, 12 channels available for user including 6x differential			
Internal ADC VREF		1.65 V, 1.8 V, 2.048 V, 2.5 V or VREF+ input			-
	VREF+ input pin	Yes			

4.2. Memory

The ECK10-13xA series core board is equipped with DDR3L SDRAM memory chips on the board. It is designed with 16-bit memory data width and has two capacities of 256MB/512MB available;

4.3. Clock

The ECK10-13xA series core board provides one 32.768KHz crystal (passive) oscillator circuit and one 24MHz crystal (passive) oscillator circuit as system clock sources.

4.3.1. I/O Allocation

Clock I/O Allocation Table

MPU I/O Pins	Function
PC14	32.768KHz IN
P C15	32.768KHz OUT
PH0	24MHz IN
PH1	24MHz OUT

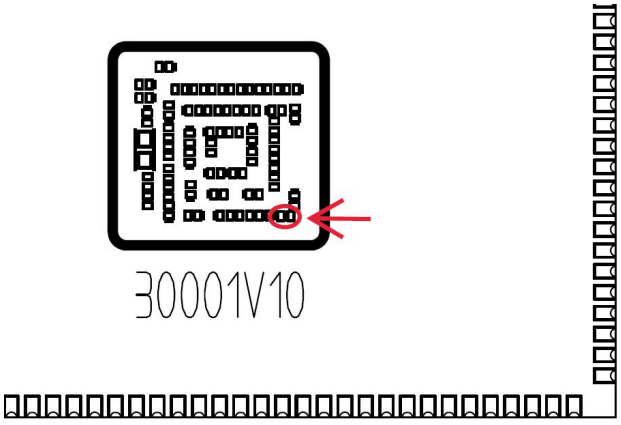
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4.4. Storage

In the storage design of the ECK10-13xA series core board, in order to reserve more SDMMC interfaces for user applications and facilitate the expansion of SD card, eMMC storage, WiFi and other functions, only one parallel NAND FLASH storage solution is designed on the board. Users can flexibly configure multiple storage solutions including SD card, eMMC, NAND FLASH, NOR FLASH, etc. on the baseboard.

The core board product provides two optional parallel NAND FLASH configurations of 256MB and 512MB . NAND FLASH is connected to the processor via the FMC (Flexible memory controller) interface. It supports 8-bit parallel bus access.

The core board is designed with a configurable resistor at the bottom. After welding the resistor, the write protection function of the NAND FLASH chip can be realized. The short-circuit resistor can be selected to be 100 ohms or less. The resistor position is shown in the figure below.



Write protection configuration resistor location diagram

4.4.1. I/O Allocation

NAND FLASH chip I/O allocation table

MPU I/O Pins	Function
PD11	FMC_CLE
PD12	FMC_ALE
PD4	FMC_NOE
PG9	FMC_NCE
PD5	FMC_NWE
PA9	FMC_NWAIT
PD14	FMC_D0
PD15	FMC_D1
PD0	FMC_D2

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PD1	FMC_D3
PE7	FMC_D4
PE8	FMC_D5
PE9	FMC_D6
PE10	FMC_D7

4.5. Ethernet

The ECK10-13xA series core board design is designed to facilitate the user's baseboard Gigabit network application and reduce the user's baseboard BOM cost and software development cost. The Ethernet PHY chip and related circuits are designed on the core board. The Ethernet PHY chip and the processor are connected through the RGMII (Gigabit Ethernet MAC interface) interface. The core board Ethernet PHY chip supports IEEE 802.3 10BASE-T, IEEE 802.3u 100BASE-TX and IEEE 802.3ab 1000BASE-T protocols, and can easily realize the 10M/100M/1000Mbps adaptive Ethernet electrical port function on the baseboard.

4.5.1. I/O Allocation

Ethernet PHY chip I/O allocation table

MPU I/O Pins	Function
PC4	ETH1_RXD0
PC5	ETH1_RXD1
PB0	ETH1_RXD2
PB1	ETH1_RXD3
PD7	ETH1_RX_CLK
PA7	ETH1_RX_CTL
PG13	ETH1_TXD0
PG14	ETH1_TXD1
PC2	ETH1_TXD2
PE5	ETH1_TXD3
PB11	ETH1_TX_CTL
PC1	ETH1_GTX_CLK
PA2	ETH1_MDIO
PG2	ETH1_MDC
PG12	ETH1_PHY_INTN
PF7	ETH1_CLK125
PH6	ETH1_NRST

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4.6. USB

The USB function can be configured as 2-way USB2.0 or 1-way USB OTG and 1-way USB2.0.

4.6.1. I/O Allocation

USB I/O Assignment Table

MPU I/O Pins	Function
PA7	USB_OTG_HS_VBUS
USB_DM1	USBH_HS1_DM
USB_DP1	USBH_HS1_DP
USB_DM2	USB_OTG_HS_DM
USB_DP2	USB_OTG_HS_DP

4.7. Power supply

The ECK10-13xA series core board uses ST's original PMIC (STPMIC1APQR) solution to implement the power system design. The original PMIC solution not only provides high-performance power functions, but also provides precise power-on and power-off timing control to ensure system operation reliability and service life, while also providing extremely high functional density.

The PMIC chip can provide 4 BUCK, 6 LDO, 1 BOOST, and 1 REFDDR power supplies. The core board power distribution is shown in the following table.

PMIC power distribution table

PMIC Power Supply	Network Name	Design voltage	illustrate	Power-on sequence RANK
BUCK1	VDD_CORE	1.2V	Processor core power	RANK 2
BUCK2	VDD_DDR	1.35V	Memory	RANK 0
BUCK3	VDD_3V3	3.3V	Processor I/O power	RANK 1
BUCK4	P3V3	3.3V	Peripheral I/O	RANK 2
BOOST	-	-	Unused	N/A
REFDDR	VREF_DDR	0.675V	Memory reference circuit	RANK 0
LDO1	P_LDO1_R0	1.8V	Output LDO power supply	RANK 0
LDO2	P_LDO2_R0	1.8V	Output LDO power supply	RANK 0
LDO3	-	-	Unused	RANK 0
LDO4	VDD_USB	3.3V	USB Power	RANK 3
LDO5	VDD_ADC	2.9V	ADC power supply	RANK 2

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			VDDA	
LDO6	-	-	Unused	RANK 0

Note: The reference power supply VREF+ of the processor ADC uses an internal reference.

4.7.1. I/O Allocation

The following table shows the pins that connect the processor to the PMIC, mainly including I2C and WAKEUP signals.

PMIC I/O Assignment Table

MPU I/O Pins	PMIC Pinout
PB7	PMIC SDA
P E2	PMIC SCL
PC13	PMIC WAKEUP
PF8	PMIC INTn

5. Baseboard hardware design

5.1. Power interface

For embedded product design, the design of the power supply system is crucial . It is necessary to consider not only the basic electrical parameters of the power supply itself, but also various factors such as the stability design and timing design of the power supply. Considering the reduction of user application difficulty and cost, the ECK10-13xA series core board not only adopts a single power supply solution, but also provides a 3-way power output function. In some conventional applications, users do not need to design an additional power supply.

5.1.1. Power input

The ECK10-13xA series core board is powered by a single DC +5V power supply, corresponding to pins 127 and 128 of the stamp hole connector. The supply voltage range is 5.0V±10%.

5.1.2. Power Output

To facilitate the user's baseboard design and reduce the baseboard BOM cost, the core board outputs 3 power supplies, including 1 Buck output 3.3V power supply and 2 LDO output software adjustable power supplies. When the power is sufficient, the user's baseboard does not need to design a separate power supply, and can directly use the power provided by the core board to

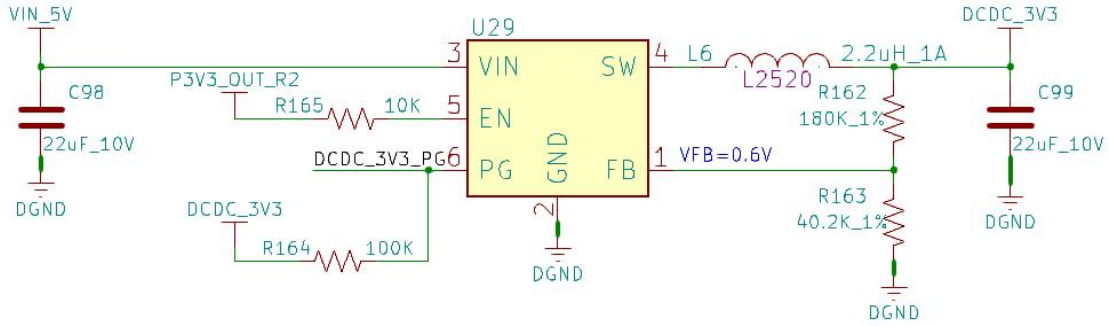
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power the baseboard chip and I/O interface.

The 3.3V power supply output by the Buck is named P3V3_OUT_R2, which corresponds to pins 124 and 125 of the stamp hole connector. The maximum current output by this power supply is 1A. This power supply is output by BUCK4 of the PMIC chip on the core board, and the power-on sequence belongs to RANK2.

The names of the 2 LDO output power supplies are P_LDO1_R0 and P_LDO2_R0, which correspond to the 121 and 122 pins of the stamp hole connector respectively. The maximum current of the 2 LDO power outputs is 350mA. The P_LDO1_R0 power supply is output by the LDO1 of the PMIC chip on the core board. The power-on sequence belongs to RANK0. There is no output when powered on. It needs to be configured by software before it can be output. The P_LDO2_R0 power supply is output by the LDO2 of the PMIC chip on the core board. The power-on sequence belongs to RANK0. There is no output when powered on. It needs to be configured by software before it can be output.

The power output by the core board meets the system power supply power-on timing requirements. When designing the baseboard power supply, you can use the P3V3_OUT_R2 power supply as the power enable control signal to control the power-on of the baseboard chip I/O interface. The reference original diagram is shown in the figure below.



Backplane I/O Power Sequencing Reference Schematic

Note: The 3-way power output cannot be directly connected in parallel.

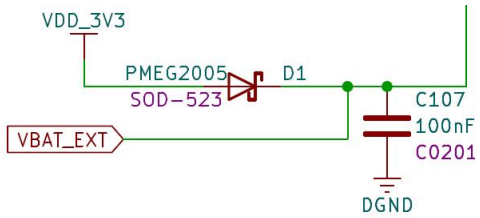
5.1.3. VBAT power supply

VBAT_EXT is the RTC backup battery interface, corresponding to the 43rd pin of the stamp hole connector, and can be powered by an external battery. Its function is to supply power to the core board RTC power supply through an external battery when the core board 5V power supply is powered off, so as to maintain the normal operation of the processor's internal RTC function,

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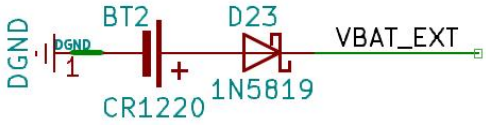
power management function, and some configuration registers. The voltage range of VBAT_EXT is 1.6-3.6V.

In the core board, the VBAT_EXT power supply is connected in parallel with the 3.3V power supply in the board and then input to the VBAT pin of the MPU chip. The parallel circuit is shown in the figure below.



VBAT power supply parallel circuit diagram

As shown in the figure above, when two power supplies are connected in parallel on the core board, there is no diode in series with the VBAT_EXT power supply. If the baseboard uses a button battery to provide RTC backup power, a diode should be connected in series with the baseboard VBAT_EXT circuit to prevent the internal power supply from charging the battery after power-on. The circuit is shown in the figure below.



Baseboard VBAT power supply reference circuit diagram

If the RTC backup battery and related functions are not used, the VBAT_EXT pin can be left floating.

5.1.4. Pin Definition

Power Interface Definition Table

Pinout	Pin Name	Chip Pins	Level	type	illustrate
43	VBAT_EXT	MPU.VBAT	3.3V	PWR-I	No diode inside the board
121	P_LDO1_R0	PMIC.LDO1	3.3V	PWR-O	
122	P_LDO2_R0	PMIC.LDO2	3.3V	PWR-O	
124	P3V3_OUT_R2	PMIC.BUCK4	3.3V	PWR-O	
125	P3V3_OUT_R2	PMIC.BUCK4	3.3V	PWR-O	
127	VIN_5V		5.0V	PWR-I	
128	VIN_5V		5.0V	PWR-I	

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5.2. Launch Configuration

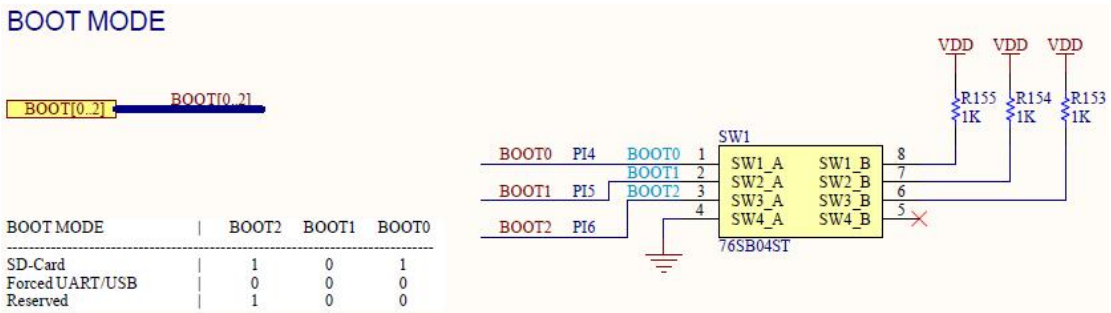
The ECK10-13xA core board supports multiple boot modes. After the chip is powered on, the level status on the BOOT[2:0] pin will be read. Different level statuses correspond to specific boot modes. BOOT[2:0] has a pull-down resistor inside the processor. Usually, the baseboard can be designed with a pull-up resistor. The BOOT configuration mode is shown in the figure below.

Table 2. Boot modes

BOOT2	BOOT1	BOOT0	Initial boot mode	Comments
0	0	0	UART and USB(1)	Wait incoming connection on: – USART3/6 and UART4/5/7/8 on default pins – USB high-speed device on OTG_HS_DP/DM pins(2)
0	0	1	Serial NOR flash(3)	Serial NOR flash on QUADSPI(5)
0	1	0	e•MMC(3)	e•MMC on SDMMC2 (default)(5)(6)
0	1	1	NAND flash(3)	SLC NAND flash on FMC
1	0	0	Development boot (no flash memory boot)	Used to get debug access without boot from flash memory(4)
1	0	1	SD card(3)	SD card on SDMMC1 (default)(5)(6)
1	1	0	UART and USB(1)(3)	Wait incoming connection on: – USART3/6 and UART4/5/7/8 on default pins – USB high-speed device on OTG_HS_DP/DM pins(2)
1	1	1	Serial NAND flash(3)	Serial NAND flash on QUADSPI(5)

BOOT mode configuration diagram

For ECK10-13xA core board, if booting from the on-board NAND FLASH, configure BOOT[2:0] to 011; if booting from the SD card on the SDMMC1 interface of the baseboard, configure BOOT[2:0] to 101; if in debug mode, booting from USB OTG, configure BOOT[2:0] to 000. The baseboard circuit design corresponding to the BOOT[2:0] signal can be referred to the figure below.



BOOT signal baseboard reference schematic diagram

5.2.1. Pin Definition

BOOT mode interface definition table

Pinout	Pin Name	Chip Pins	Level	type	illustrate
96	GPIO_PI4-BOOT0	MPU.PI4	3.3V	I/O	On-chip pull-down

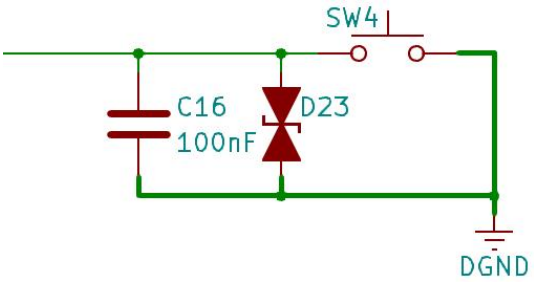
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100	GPIO_PI5-BOOT1	MPU.PI5	3.3V	I/O	On-chip pull-down
74	GPIO_PI6-BOOT2	MPU.PI6	3.3V	I/O	On-chip pull-down

5.3. Reset and power buttons

The two signals NRST_CPU and PMIC_PONKEY led out by the ECK10-13xA series core board can be used to connect external buttons to achieve processor reset and power control.

The NRST_CPU signal is designed to be pulled up to 3.3VI/O power supply with a 10K resistor in the core board. The PMIC_PONKEY signal is connected to the PMIC chip PONKEYn pin in the core board and pulled up to 5V power supply in the PMIC chip. Since these two signals have pull-up resistors in the core board and the pull-up power rails are different, do not connect the pull-up resistors directly to the buttons or drive them through OD gates when used in the baseboard. The button reference schematic is shown in the figure below.



Button reference schematic

Note: Do not pull up the reset and power button signals through resistors at will. If the pull-up power rail is incorrect, it may cause uncertain signals to be input to the button signal interface when the system is in standby or shutdown.

5.3.1. Pin Definition

Button interface definition table

Pinout	Pin Name	Chip Pins	Level	type	illustrate
123	NRST_CPU	MPU.NRST	3.3V	I	No diode inside the board, 10K pull-up
126	PMIC_PONKEY	PMIC.PON	5.0V	I	No diode inside the board, internal pull-up

5.4. Display Interface

The ECK10-13xA series core board provides a 24-bit parallel digital RGB display interface, with a maximum resolution of 1366 x 768@60 fps, a maximum pixel clock of 90MHz, and supports RGB888, RGB666, RGB565, RGB332, and YUV422 data formats. It also provides all

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the signals required for LCD and TFT screens. Customers can configure the display resolution and display data format according to their needs .

In LCD and TFT screen applications, GPIO can be used to control screen power and backlight power. PWM output can be used to control backlight brightness. I2C and GPIO external interrupt functions can also be used to connect to the touch screen. For related reference interface definitions, see the display interface reference definition table.

5.4.1. Interface definition

Display interface reference definition table

Pin out	Pin Name	Function	Remark
34	GPIO_PE11	LTDC_R0	Show red data
twenty two	GPIO_PG7	LTDC_R1	Show red data
27	GPIO_PH8	LTDC_R2	Show red data
twenty one	GPIO_PB12	LTDC_R3	Show red data
11	GPIO_PE1	LTDC_R4	Show red data
36	GPIO_PF5	LTDC_R5	Show red data
35	GPIO_PE13	LTDC_R6	Show red data
28	GPIO_PF6	LTDC_R7	Show red data
120	GPIO_PF0	LTDC_G0	Show Green Data
9	GPIO_PF1	LTDC_G1	Show Green Data
3	GPIO_PH13	LTDC_G2	Show Green Data
7	GPIO_PF3	LTDC_G3	Show Green Data
32	GPIO_PD13	LTDC_G4	Show Green Data
15	GPIO_PG0	LTDC_G5	Show Green Data
6	GPIO_PC7	LTDC_G6	Show Green Data
16	GPIO_PA15	LTDC_G7	Show Green Data
13	GPIO_PD9	LTDC_B0	Show blue data
5	GPIO_PB9	LTDC_B1	Show blue data
12	GPIO_PD10	LTDC_B2	Show blue data
2	GPIO_PF2	LTDC_B3	Show blue data
14	GPIO_PH14	LTDC_B4	Show blue data
41	GPIO_PE0	LTDC_B5	Show blue data
40	GPIO_PB6	LTDC_B6	Show blue data
twenty four	GPIO_PE15	LTDC_B7	Show blue data
4	GPIO_PB5	LTDC_DE	Display data is valid
119	GPIO_PC6	LTDC_HSYNC	Display Line

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			Synchronization
33	GPIO_PE12	LTDC_VSYNC	Display field sync
118	GPIO_PB13	LTDC_CLK	Display Pixel Clock
44	GPIO_PF10_R	LCD_VDD_EN	Screen power enable
31	GPIO_PH11	LCD_BL_EN	Screen backlight enable
25	GPIO_PG15	LCD_BL_PWM	Screen backlight brightness control
45	GPIO_PH2	TP_INT	Touch screen interrupt
37	GPIO_PD3	TP_I2C1_SDA	Touch screen I2C data
17	GPIO_PB8	TP_I2C1_SCL	Touch screen I2C clock

5.4.2. LAYOUT SUGGESTIONS

- If the display signal is designed with a 22Ω series matching resistor , it is recommended to place it close to the stamp hole of the core board ;
- All GPIO signals have been processed to equal length in the core board. See the pin definition table for the wiring length in the core board;
- It is recommended that the baseboard LCD signal lines be of equal length with an error range of ±100mil and the signal line spacing be at least 2W.

5.5. Camera interface

The ECK10-13xA series core board uses the STM32MP135 series MPU chip to support 1 digital camera interface. The camera interface will occupy a large number of I/O pins in the application, reducing other multiplexing functions. It is recommended to use a USB interface camera to implement the camera function.

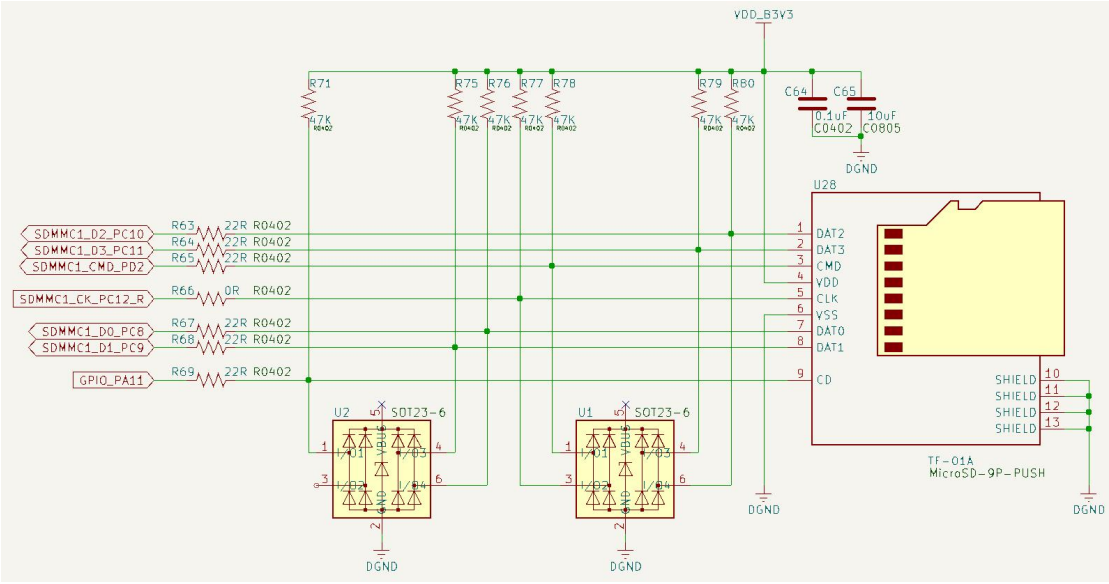
5.6. SDMMC card interface

The STM32MP13 series processors provide two SDMMC controllers. To ensure that users can expand more functional interfaces through SDMMC, the ECK10-13xA series core board is designed to lead the signals of the two SDMMC controllers to the stamp holes. Through the SDMMC interface signals, you can expand SD cards, eMMC and other storage on the baseboard, and you can also expand communication interfaces such as WiFi and Bluetooth.

The I/O of the STM32MP13x processor can be configured with on-chip pull-up resistors. These pull-up resistors can meet the pull-up requirements when the SD card interface is expanded,

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and the user design does not need external pull-up resistors. The core board has already connected a 22- ohm matching resistor in series with the SDMMC clock signal, and the user design does not need external series resistors. To expand the Micro SD card through the SDIO interface, please refer to the original design below. It should be noted that the core board SDMMC signal only provides 3.3V I/O level, and does not support 1.8V I/O level modes such as USH-I.



SD card reference circuit diagram

5.6.1. Pin Definition

SDMMC signal pin definition

Pinout	Pin Name	Chip Pins	Level	type	Trace length	illustrate
102	SDMMC2_CMD_PG6	MPU.PG6	3.3V	I/O	1405.41	
103	SDMMC2_CK_PE3_R	MPU.PE3	3.3V	I/O	1433.22	Connect a 22 ohm resistor in series
104	SDMMC2_D3_PB4	MPU.PB4	3.3V	I/O	1465.48	
105	SDMMC2_D0_PB14	MPU.PB14	3.3V	I/O	1453.64	
106	SDMMC2_D2_PB3	MPU.PB3	3.3V	I/O	1457.94	
108	SDMMC2_D1_PB15	MPU.PB15	3.3V	I/O	1427.23	
109	SDMMC1_CMD_PD2	MPU.PD2	3.3V	I/O	1403.51	
110	SDMMC1_D3_PC11	MPU.PC11	3.3V	I/O	1395.3	
111	SDMMC1_D1_PC9	MPU.PC9	3.3V	I/O	1396.27	
112	SDMMC1_D0_PC8	MPU.PC8	3.3V	I/O	1406.37	
113	SDMMC1_D2_PC10	MPU.PC10	3.3V	I/O	1412.57	
115	SDMMC1_CK_PC12_R	MPU.PC12	3.3V	I/O	1390.97	Connect a 22 ohm resistor in series

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5.6.2. LAYOUT SUGGESTIONS

- The recommended single-ended impedance for SDMMC signals is 50Ω;
- The data line and control line should be as equal in length as possible;
- The distance between the clock signal and other signals follows the 3W rule.

5.7. USB interface

The ECK10-13xA series core board supports 2 USB 2.0 HOST interfaces, or 1 USB OTG interface and 1 USB 2.0 HOST interface. At the same time, the core board also leads to the OTG_HS_VBUS signal, which can be used for software switching between HOST and DEVICE modes when the OTG interface is used. If the OTG_HS_VBUS function is not used, this pin can also be used for GPIO.

5.7.1. Pin Definition

USB signal pin definition

Pinout	Pin Name	Chip Pins	Level	type	Trace length	illustrate
76	USBH_HS1_DM	MPU.USB_DM1	USB	I/O	923.39	
77	USBH_HS1_DP	MPU.USB_DP1	USB	I/O	922.36	
79	USB_OTG_HS_DM	MPU.USB_DM2	USB	I/O	904.81	
80	USB_OTG_HS_DP	MPU.USB_DP2	USB	I/O	904.27	
97	OTG_VBUS_PI7	MPU.PI7	3.3V	I/O	1025.11	Support 5V tolerance

5.7.2. LAYOUT SUGGESTIONS

- The USB signal routing is controlled to be of equal length;
- The differential impedance of the USB signal is controlled at 90Ω;
- The USB signal cable should be as short as possible;
- Try not to change layers for USB signals. If you do, place a GND return via near the layer-changing via .
- split USB signals across planes to ensure the continuity of the reference plane;
- Keep USB signals away from other clock and digital signals.

5.8. audio port

The STM32MP13 series processors provide a variety of audio interface forms. The

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ECK10-13xA series core board recommends the use of the I2S audio interface. When using the I2S interface signal to implement audio functions, an external audio codec is required to implement audio interface functions such as headphones, microphones, and speakers through the codec.

5.9. UART Interface

The ECK10-13xA series core board can support up to 4 UART interfaces and 3 USART interfaces. The core board uses UART 4 as the debug serial port by default.

5.10. SPI interface

The ECK10-13xA series core board provides a QSPI interface that can be used for BOOT to facilitate the application of multiple BOOT modes. The CLK signal of the QSPI has been connected in series with a 22-ohm resistor inside the core board. In addition, it can support up to 5 SPI interface functions.

5.10.1. Pin Definition

QSPI signal pin definition

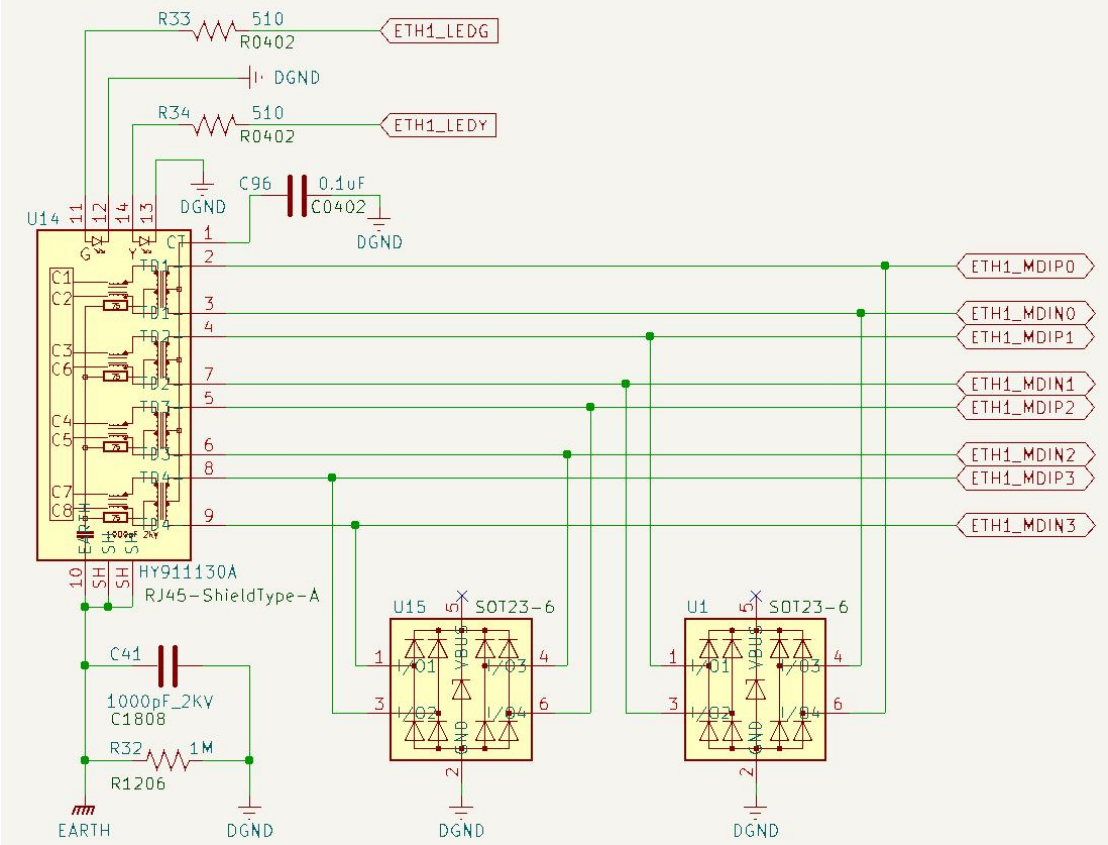
Pinout	Pin Name	Chip Pins	Level	type	Trace length	illustrate
44	QSPI_CLK_PF10_R	MPU.PF10	3.3V	I/O	810.44	Connect a 22 ohm resistor in series
45	QSPI_BK2_IO0_PH2	MPU.PH2	3.3V	I/O	744.04	
46	QSPI_BK2_IO1_PG10	MPU.PG10	3.3V	I/O	766.74	
48	QSPI_BK2_IO2_PE14	MPU.PE14	3.3V	I/O	771.63	
49	QSPI_BK2_NCS_PE4	MPU.PE4	3.3V	I/O	789.01	
50	QSPI_BK2_IO3_PH7	MPU.PH7	3.3V	I/O	723.97	

5.11. Ethernet interface

To expand the Ethernet interface using the ECK10-13xA series core board, you only need to design an Ethernet transformer and an RJ45 connector on the baseboard. It should be noted that the Ethernet interface signals are dedicated signals and cannot be used or configured as other functional I/Os. If the network function is not used, these pins can be left floating. Due to the limitation of I/O pin multiplexing, the ECK10-13xA series core board can only expand a maximum of 1 Gigabit Ethernet interface. The baseboard Ethernet interface expansion can refer to

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the design shown in the figure below.



Baseboard Ethernet Interface Reference Schematic

The core board provides two Ethernet LED indicator signal outputs, named ETH1_LEDG and ETH1_LEDY, which are connected to the LED1 and LED2 pins of the PHY chip in the core board respectively. Under the default software configuration conditions, the high level of ETH1_LEDG indicates a 100M network link, and the high-low change indicates that the 100M network is active; the high level of ETH1_LEDY indicates a 1000M network link, and the high-low change indicates that the 1000M network is active. In the baseboard application, these two signals can be used directly to drive the LED lights.

It should be noted that the two signals ETH1_LEDG and ETH1_LEDY are used for the power-on configuration function of the PHY chip. Both signals are pulled down in the core board, so when driving LEDs or other devices, care should be taken not to affect the power-on status of these two signals. It is recommended to drive the anode of the LED directly or drive the cathode of the LED after passing through a buffer device.

5.11.1. Pin Definition

Ethernet Interface Definition Table

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Pinout	Pin Name	Chip Pins	Level	type	Trace length	illustrate
70	ETH1_LEDG	PHY.33	3.3V	O		4.7K pull-down
71	ETH1_LEDY	PHY.34	3.3V	O		4.7K pull-down
82	ETH1_MDIN2	PHY.MDIN2	ETH	I/O	882.82	
83	ETH1_MDIP2	PHY.MDIP2	ETH	I/O	881.92	
84	DGND			PWR		
85	ETH1_MDIN0	PHY.MDIN0	ETH	I/O	894.9	
86	ETH1_MDIP0	PHY.MDIP0	ETH	I/O	895.92	
87	DGND			PWR		
88	ETH1_MDIN1	PHY.MDIN1	ETH	I/O	865.31	
89	ETH1_MDIP1	PHY.MDIP1	ETH	I/O	866.58	
90	DGND			PWR		
91	ETH1_MDIN3	PHY.MDIN3	ETH	I/O	890.17	
92	ETH1_MDIP3	PHY.MDIP3	ETH	I/O	888.93	

5.11.2. LAYOUT SUGGESTIONS

- Ethernet MDI signals are differential signals, so differential routing should be done during Layout design;
- The Ethernet MDI signal differential line pair has an equal length of <5mil and a differential impedance of 100Ω;
- The Ethernet MDI signal in the core board has been equal-length and impedance-controlled;
- The spacing between adjacent signal traces should be 3W;
- If the connector and transformer are separated, the transformer is placed close to the RJ45 connector.

5.12. CAN interface

The ECK10-13xA series core board can support up to 2 CAN bus functions (supported by the STM32MP135 series MPU chip). The CAN bus signal of the ECK10-13xA series core board also requires an external CAN interface chip to realize the final CAN bus interface function.

5.13. I2C Interface

The ECK10-13xA series core board can support up to 4 I2C buses. It should be noted that I2C4 in the I2C bus controller provided by the MPU is specifically used for PMIC control and is not led out to the stamp hole. In addition, all I2C bus signals do not provide pull-up resistors on

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the core board, and it is necessary to design pull-up resistors for the I2C bus on the baseboard. When designing the pull-up resistor on the baseboard, pay attention to the selection of the pull-up power rail.

5.14. ADC Interface

The ECK10-13xA series core board can provide up to 8 ADC input channels. The core board has an MPU chip, and the ADC power supply VDDA is powered by PMIC's LDO5, with a default output voltage of 2.9V. The ADC reference voltage VREF uses the MPU internal reference.

5.15. GPIO interface

The ECK10-13xA series core board can provide up to 86 GPIO interfaces, but most of them have multiplexing functions. Users can flexibly configure GPIO according to their own needs.

5.16. Hardware Design Checklist

- Power rail: Check whether there is an inconsistency in the power rails of the I/O interface application, such as a 1.8V signal connected to a 3.3V signal. If there is a need to connect signals with different power rails, a level conversion circuit should be used.
- Power-on sequence: Check whether the signals connecting the baseboard and the core board are powered on first, or whether the power-on time of the two board signals is very different.
- Pull-up and pull-down resistors: The output state of the multiplexed I/O interface is uncertain before the power-on software configuration. If the signal needs to maintain a certain level when powered on, pull-up and pull-down resistors should be designed on the baseboard. Some functional signals also need to be designed with pull-up or pull-down resistors on the baseboard, such as I2C signals. When designing pull-up resistors, attention should be paid to the design of the pull-up power rail.
- ESD protection: The corresponding ESD protection design should be considered for the external interface signal. The selection of ESD solution should take into account the requirements of signal rate, communication protocol and application environment.
- High-speed signals should be of equal length: High-speed signals should consider the equal length design of PCB, including USB, Ethernet, SDMMC, display, etc.

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6. Software Resources

The ECK10-13xA series core board is equipped with an operating system based on the Linux 6.1.28 kernel. The development board comes with a cross-compilation tool chain required for embedded Linux system development, TF-A source code, Optee-os source code, U-boot source code, Linux kernel and driver module source code, as well as various development and debugging tools suitable for Windows desktop environment and Linux desktop environment.

operating system:

Ubuntu 18.04 system with XFCE desktop

System source code:

TFA 2.8.6

Op-tee 3.19

U-boot 2022.10

Kernel 6.1.28

Building Road 2020.02.6

Development environment and IDE:

Burning tool: STM32CubeProgrammer

Development tool: STM32C ube MX

6.1. System resource

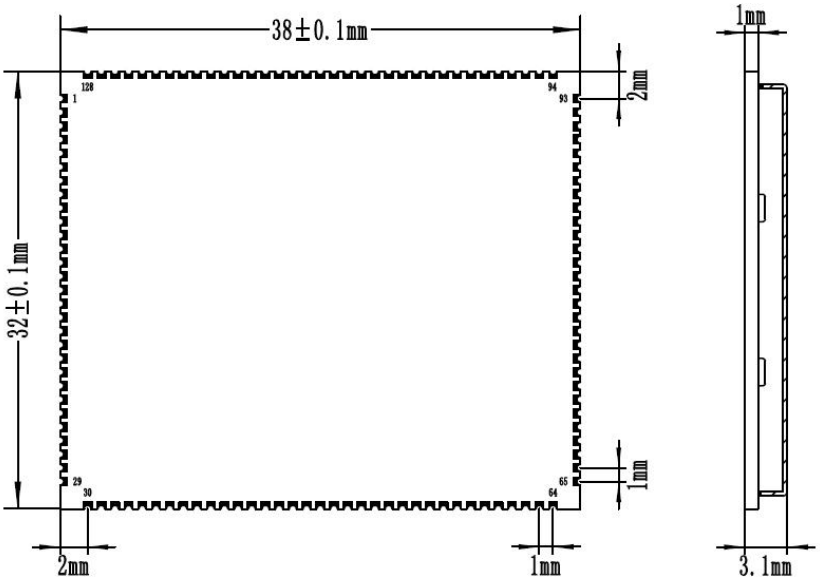
System Software Resource Table

category	name	Description	Source code
F SBL	TFA 2.8.6	First stage bootloader	/source/tf-a.tar.xz
S SBL	Op-tee 3.19	Second stage bootloader	/source/optee-os.tar.xz
S SBL	U-boot 2022.10	Second stage bootloader	/source/u-boot.tar.xz
Linux kernel	Kernel 6.1.28	Linux kernel	/ source / linux-6.1.28 . tar.gz
Device D river	USB Host	USB Host	kernel/
	USB OTG	USB OTG	kernel/
	I2C	I2C bus driver	kernel/
	SP	S PI bus driver	kernel
	T TY	TTY serial port driver	kernel
	R S232	TTY serial port driver	kernel
	R S485	TTY serial port driver	kernel
	C AN	CAN bus driver	kernel
	Ethernet	10M/100M/1000M driver	kernel
	M MC	eMMC/TF card storage	kernel

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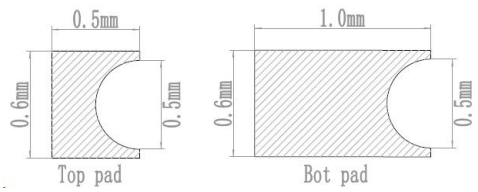
		driver	
	N AND	Nand Flash storage driver	kernel
	L C	RGB, HDMI display driver	kernel
	P W M	PWM control drive	kernel
	A DC	ADC Driver	kernel
	R	Real-time clock driver	kernel
	G PIO	GPIO Driver	kernel
	Touch	Capacitive touch driver	kernel
	Watchdog	Watchdog Driver	kernel
operating system	R ootfs	Ubuntu with XFCE desktop 18.04 System	/images/ubuntu18.ext4
development tools	Building Road 2020.02.6	Operating system build	/tools/buildroot-2020.02.6.tar.bz2
	S D K	arm-none-linux-gnueabihf 10.3	/tools/gcc-arm-10.3-2021.07-x86 _64-arm-none-linux-gnueabihf.tar.xz
	STM32CubeProgrammer	Burning tool	/ tools/SetupSTM32Cube Programmer-2.5.0.exe
	S TM32CubeMX	Resource Configuration Tools	/tools/en.stm32cubemx_v6-0-1.zip
	Win32DiskImager	Make SD card boot tool	/tools/Win32DiskImager-1.0.0-binary

7. Structure size



Stamp hole core board structure size drawing

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Stamp hole half hole size chart

8. Welding Instructions

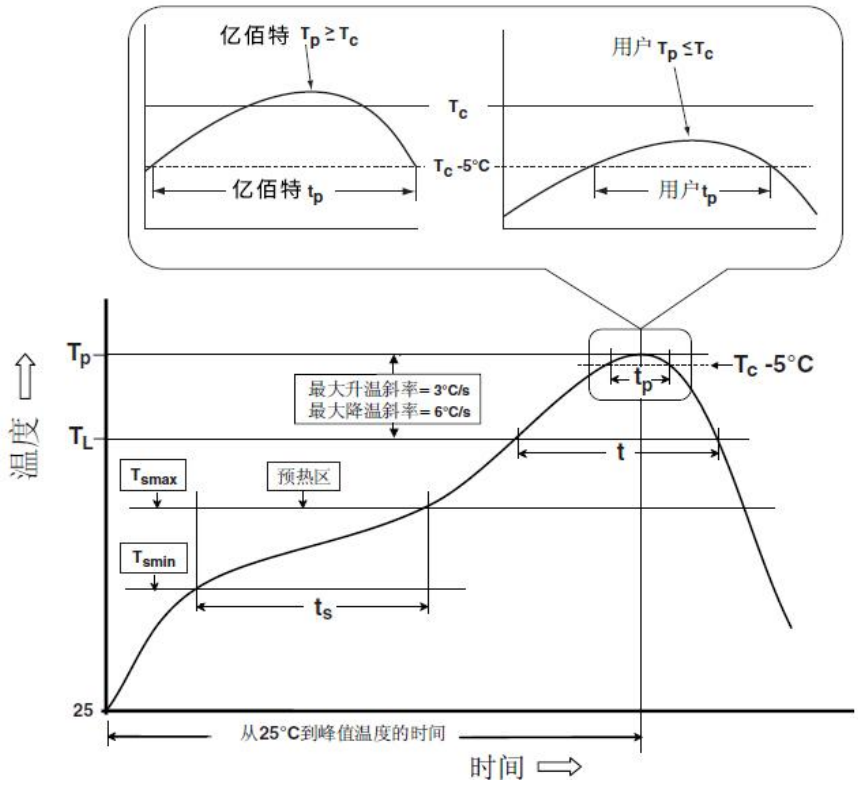
8.1. Reflow temperature

Reflow Temperature Table

Reflow profile characteristics		Leaded process assembly	Lead-free assembly
Preheating/keeping	Minimum temperature (Tsmin)	100℃	150℃
	Maximum temperature (Tsmax)	150℃	200℃
	Time (Tsmin~Tsmin)	60-120 seconds	60-120 seconds
Heating slope (TL~Tp)		3℃/sec, max.	3℃/sec, max.
Liquidus temperature (TL)		183℃	217℃
Keep time above TL		60~ 90 seconds	60~ 90 seconds
Package peak temperature Tp		Users must not exceed the temperature stated on the product's "Moisture Sensitivity" label.	Users must not exceed the temperature stated on the product's "Moisture Sensitivity" label.
The time (Tp) within 5°C of the specified classification temperature (Tc) is shown in the figure below.		20 seconds	30 seconds
Cooling slope (Tp~TL)		6℃/sec, max.	6℃/sec, max.
Time from room temperature to peak temperature		6 minutes, longest	8 minutes, longest
※The peak temperature (Tp) tolerance of the temperature curve is defined as the upper limit of the user			

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8.2. Reflow Oven Profile



Reflow Oven Profile

9. product model

9.1. Model configuration

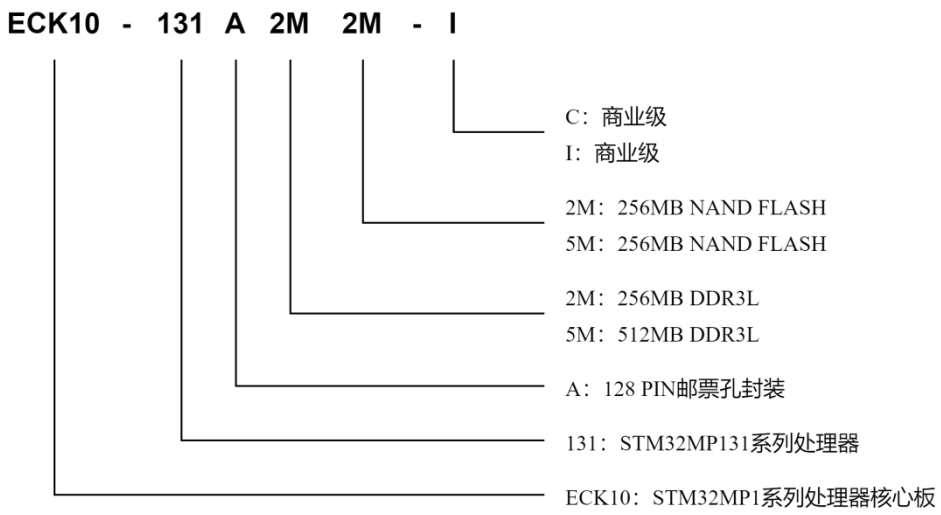
The selection configuration table is as follows:

Product Selection and Configuration Table

Serial number	Product number	Processor model	Frequency	Memory	storage	Operating temperature
1	ECK10-135A5M5M-I	STM32MP135AAF3	650 MHz	512MB DDR3L	512MB NAND	Industrial Grade -40°C ~ 85°C
2	ECK10-131A2M2M-I	STM32MP131AAF3	650 MHz	256MB DDR3L	256MB NAND	Industrial Grade -40°C ~ 85°C

The product model number is described as follows:

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Model Number Description

10. Reference documentation

- STM32MP131 Datasheet
- STM32MP13 5 Data Sheet
- STPMIC1 Data Sheet
- AN 5474 Application Note

11. Revision notes

Revision Notes Table

Version	Modifications	Change the time	prepared by	Proofreading	Approval
V1.0	First Draft	24-04-29	WFX	LqCy	WFX

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