Product manual
ECB33-PGB Single Board Computer



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Chengdu Ebyte Electronic Technology Co.,Ltd.

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1. Product Overview

1.1.Product Introduction

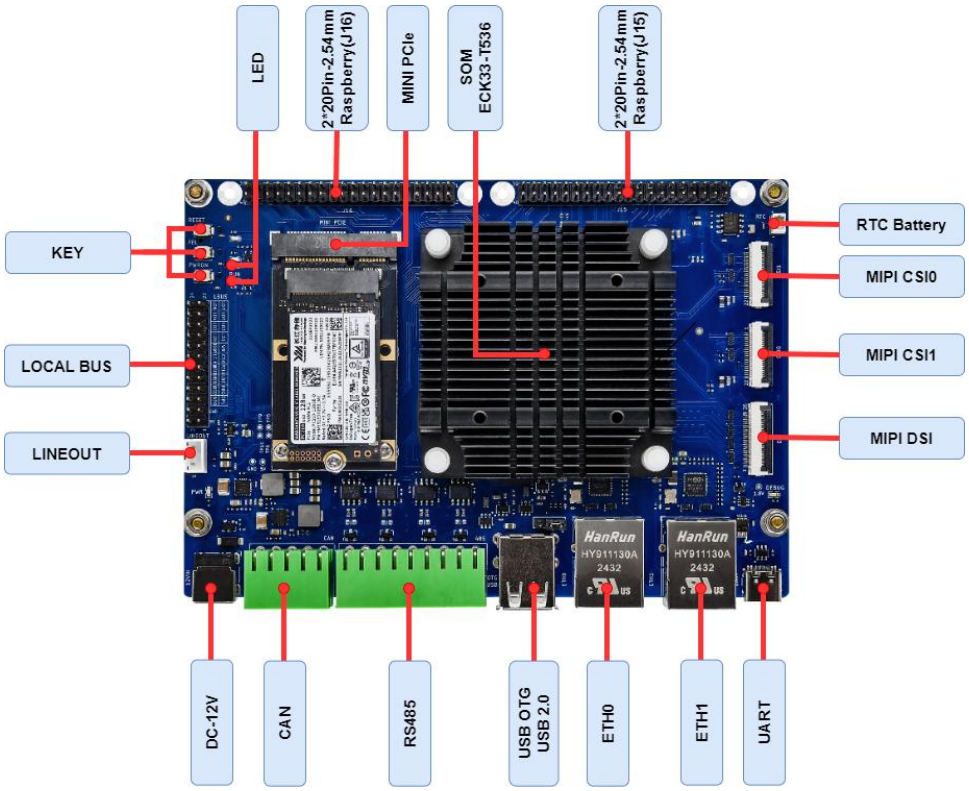
Ebyte has launched the ECB33-PGB single board computer based on the ECK33-B series core board. The core board is a 381-pin LGA package and can be soldered onto the carrier board via SMT. The carrier board design fully utilizes the core board's interfaces, bringing out MIPI DSI display interface, MIPI CSI camera interface, LOCAL BUS interface, USB2.0, USB OTG, debug interface, Ethernet interface, audio interface, MINI PCIe interface, CAN bus interface, RS485 interface, and a rich set of extended GPIO interfaces. The design level of the single board computer exceeds that of ordinary development boards, allowing it not only to verify core board functionality but also to be deployed in bulk for industrial scenarios.

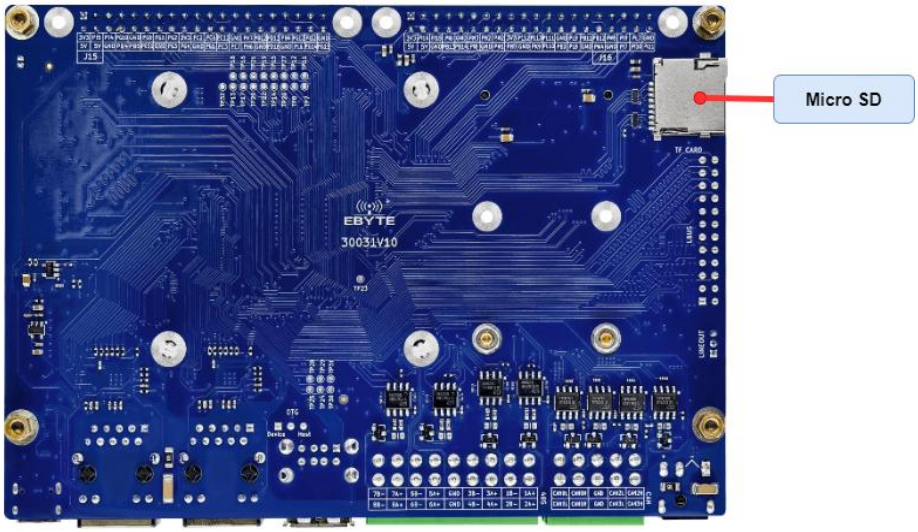
Ebyte provides a stable reference design and a comprehensive software development environment, offering users hardware design documents, software development manuals, and open-source carrier board schematics, footprint files, and PCB design files. This effectively helps users verify core board functions, improve development efficiency, shorten development cycles, optimize design quality, and accelerate product development and time to market.

The functional block diagram of the single board computer is as follows:

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Single Board Computer Functional Description Diagram

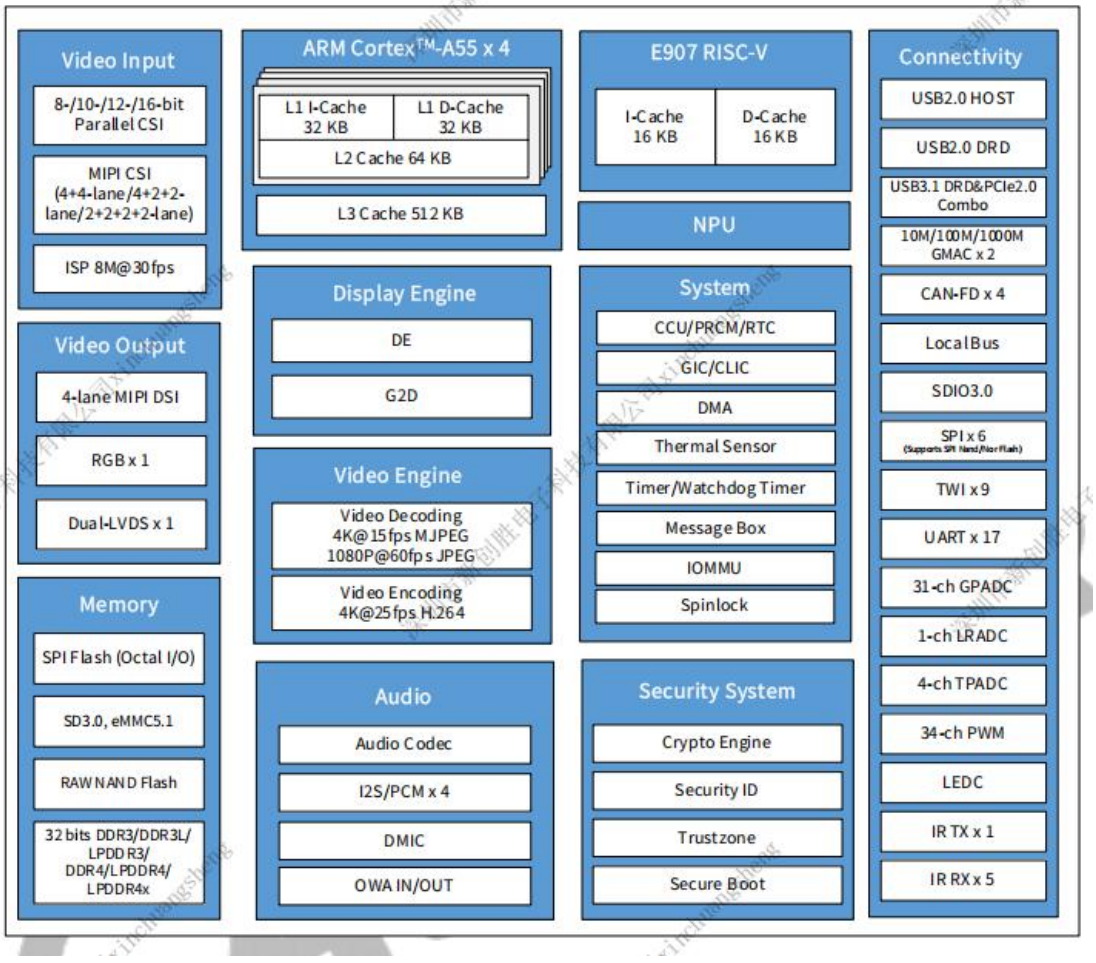
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1.2. Allwinner T536 Chip Introduction

The Allwinner T536 series is a high-performance quad-core Cortex-A55 AI platform SoC family designed for commercial, industrial, and automotive applications.

It integrates a quad-core Cortex-A55 CPU, an E907RISC-V MCU,a 2TOPS NPU.32-bit DDR3/DDR3L/DDR4/LPDDR3/LPDDR4/LPDDR4X DRAM, high-speed interfaces (PCIe 2.1 and USB 3.1), automotive interfaces (CAN FD), multiple video output interfaces (RGB, dual-link LVDS, MIPI-DSI), and video input interfaces (MIPI-CSI). The family supports a 4K@25 fps H.264 encoder, a 4K@15 fps MJPEG encoder, and geometric distortion correction (GDC)—including lens distortion correction (LDC) and fisheye correction (FEC)—to provide efficient video capture and processing.



T536 System Functional Block Diagram

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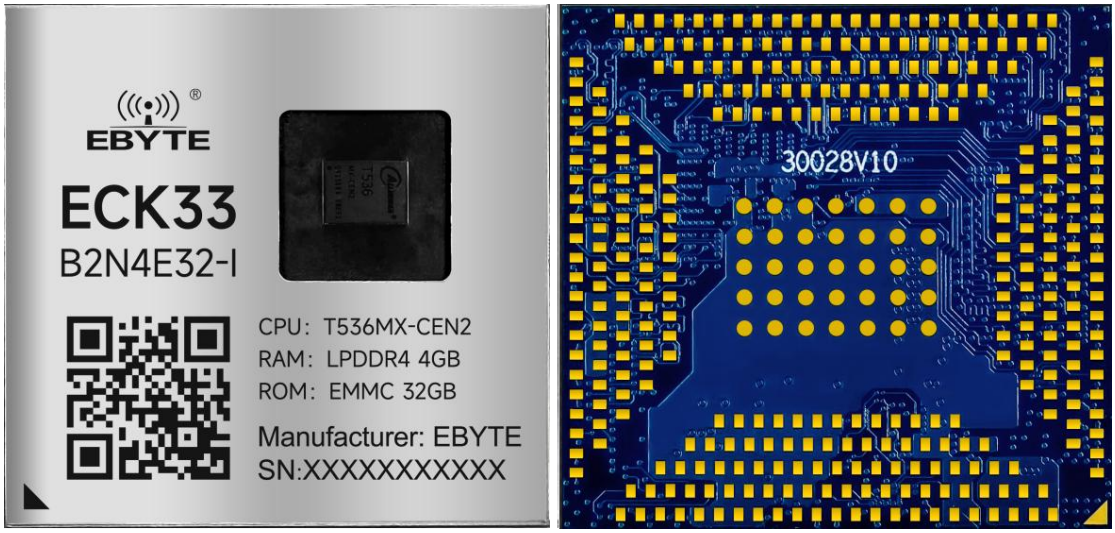
1.3.ECK33-B Series Core Board Introduction

Ebyte's ECK33-B series core boards are meticulously designed based on Allwinner's T536 series processors, adopting a new LGA interface format to deliver high performance, low power consumption, high reliability, and fully domestic industrial-grade embedded cor e boards. They can be widely applied in content sharing and self-service terminals, smart manufacturing, and other electronic commercial and industrial devices.

For details, please refer to "ECK33-B_ProductManual_EN_V1.0".

The ECK33-B series core boards include three specific product models, all designed with fully domestic industrial-grade components. They mainly differ in NPU support, DRA M memory capacity, eMMC storage capacity, and operating temperature range. Customers can choose the appropriate model according to their needs. For model selection details, ple ase see the "Model Selection" section of "ECK33-B_ProductManual_EN_V1.0".

ECK33-B series core board front view (no components on the underside) is shown be low:

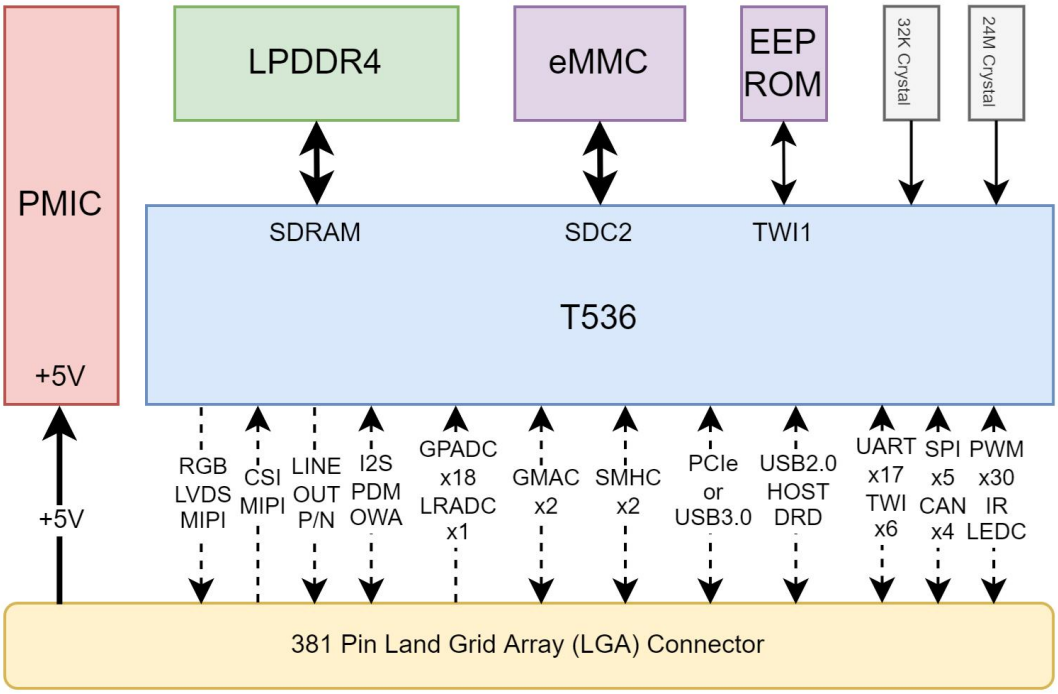


ECK33-B Series Core Board Front View

The functional block diagram of the ECK33-B series core board is as follows:

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ECK33-B Series Core Board Functional Block Diagram

1.4.Typical Applications

- Industrial control carrier board;
- Automotive electronics;
- Industrial all-in-one machine;
- Smart city;
- Tablet computer;
- IoT gateway;
- Advertising all-in-one machine;
- Robots.

2. Product Selection

2.1.Model Configuration

The model configuration table for the ECB33-PGB series single board computers is s hown in the table below:

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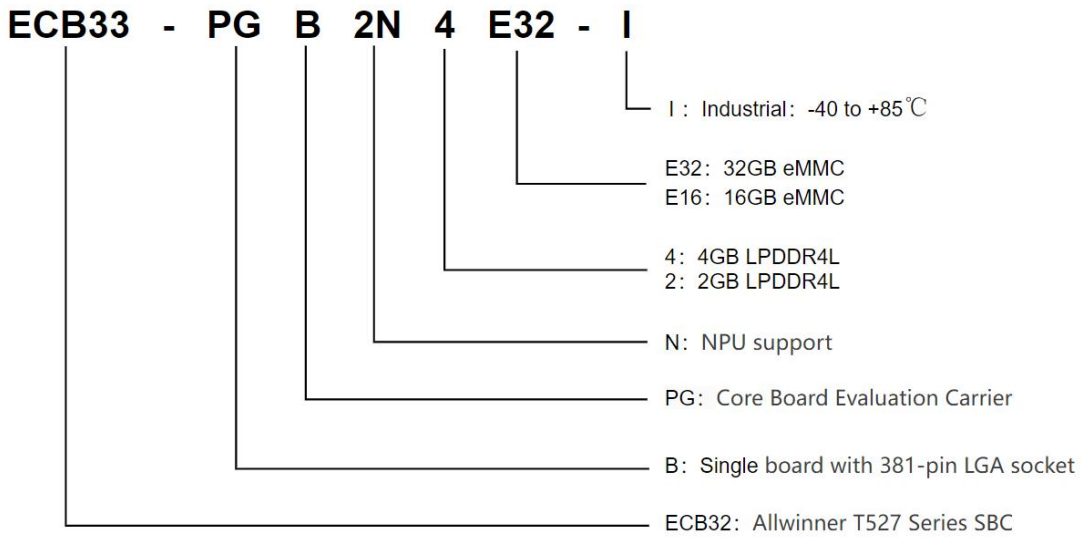
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Product Selection and Configuration Table

No.	Product Model	Core Board Model	Memory	Storage	Operating Temperature
1	ECB33-PGB2N4E32-I	ECK33-B2N4E32-I	4GB LPDDR4	32GB eMMC	-40℃ ~85℃

2.2.Model Coding

The explanation of product model coding is shown in the figure below:



Model Code Description

3. Specifications

3.1.Functional Parameters

ECB33-PGB Single Board Computer Functional Parameters Table

Power Input	One DC jack, 12V 5A input
MIPI DSI	1 channel 26-pin 4-lane MIPI DSI display interface, maximum resolution supports 2.5K@60 fps and 4K@45 fps, supports touch screen and backlight adjustment
MIPI CSI	2 channels 22-pin 2-lane MIPI CSI camera interfaces, supporting camera power control
MINI PCIe	1 PCIe 2.1 x1 lane interface, 5 Gbps per lane, supporting MINI PCIe
USB HOST	1 USB 2.0 HOST port
USB OTG	1 USB OTG port
Ethernet	2 10/100/1000 M adaptive RJ45 Ethernet ports
TFcard	1 TF card slot, supporting hot-plug detection
Audio	1 LINEOUT differential output

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Debug	1 UART debug serial port with Type-C interface
GPIO	2 sets of 2.54 mm 2×20-pin standard RPI expansion connectors, providing 3.3 V and 5 V power outputs, with a total of 56 GPIO pins, multiplexed as 2 SPI interfaces, 2 I2S interfaces, 1 SDC interface, 5 I2C interfaces, and 2 UARTs
LOCAL BUS	1 LOCAL BUS interface, supporting 8-bit data-width data transmission
CAN	4 CAN bus interfaces
RS485	8RS485 bus interfaces
Button	1 RESET button 1 PWRON button 1 FEL button
Indicator	1 power indicator LED 1 run indicator LED 1 user indicator LED 1 debug indicator LED 1 wireless network indicator LED
RTC	1.25 mm 1×2-pin RTC battery holder
TP	4 power test points (TP), 14 GPADC channels, 1 LRADC channel, 1 CK32K clock, 1 CK24M clock, 2 LINEOUTL audio outputs, 1 AP-NMI, and 8 GPIO pins

3.2.Environmental Characteristics

ECB33-PGB2N4E32-I Test Baseboard Environmental Characteristics Table

Operating Temperature	Industrial grade: -40℃ ~ 85℃ (with good heat dissipation conditions)
Storage Temperature	-40℃ ~ 85℃
Operating Humidity	5–95% humidity, non-condensing
Storage Humidity	60℃ @ 95% humidity, non-condensing

4. Interface Description

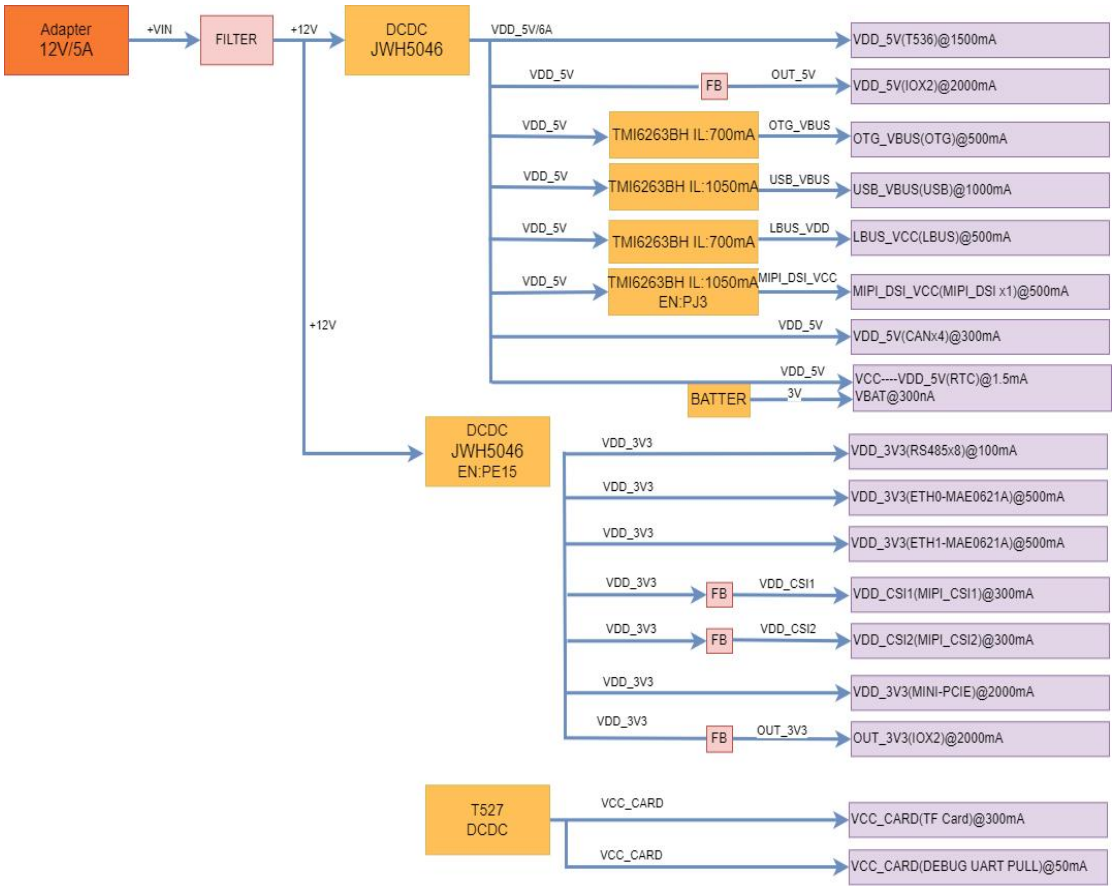
4.1.Power

4.1.1. Power Tree

The baseboard power tree block diagram is as follows:

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Baseboard Power Tree Block Diagram

4.1.2. Power Design

The power supply uses a 12V DC input and features reverse-connection protection and a TVS surge-protection circuit.

Two DCDC chips step the voltage down to 5V and 3.3V respectively to power the interfaces and the core board; each rail is designed to support a maximum current of 6A. For detailed power routing, refer to the baseboard power tree diagram.

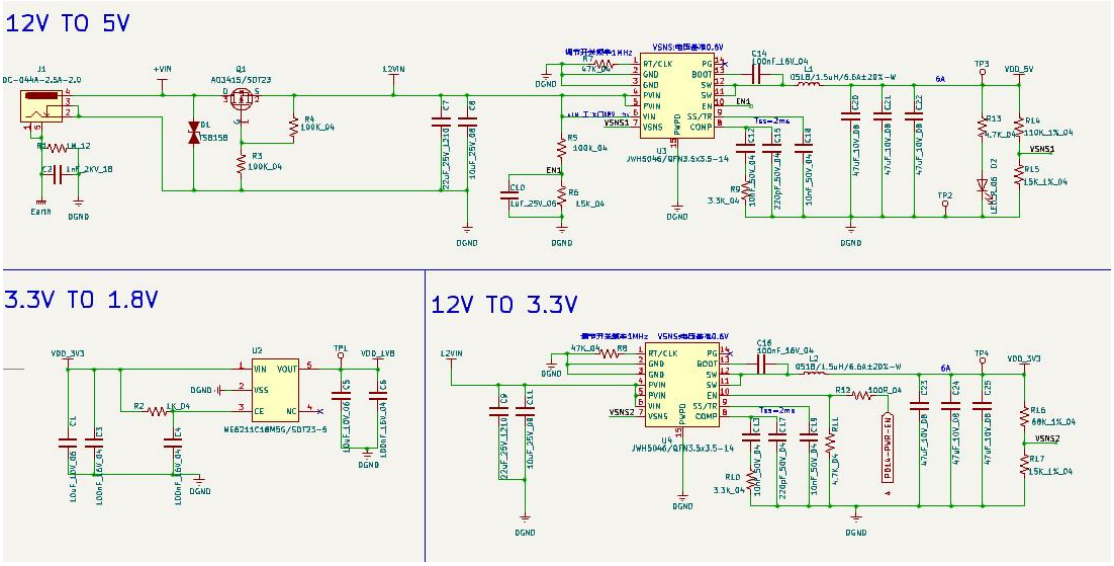
Since the TF card and serial debug circuits must power up before the other interfaces, they are supplied by the core board's VCC_CARD output.

The 3.3V power-enable signal is controlled by a processor IO pin. Choose an IO that powers up relatively late—recommended are IOs under processor PD, PE, PH, PJ, or PK—to prevent back-leakage from other baseboard interfaces powering up too early.

The USB, OTG, LOCAL BUS, and MIPI DSI interfaces powered by the 5V rail each connect to a TMI6263BH load-switch chip, providing current limiting and downstream power control via the enable pin.

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Reference schematic

Power input interface is located at the lower left corner of the baseboard, using a DC2.0 barrel connector, as shown in the power interface diagram.

Users can select a 12V power adapter of appropriate wattage according to their requirements; for detailed power distribution, refer to the baseboard power tree diagram. A 12V 5A power adapter is recommended.



Power interface diagram

4.1.3. Power consumption

Power consumption parameters table

Operating conditions	Power supply voltage (V)	Average current (A)	Power consumption（W）
Uboot state, kernel not booted	12	0.14	1.68
After system startup, no application running	12	0.26	3.12
Software reload test	12	0.40	4.80
freeze mode sleep state	12	0.15	1.8
standby mode sleep state	12	/	/

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mem mode sleep state	12	0.04	0.48
poweroff state power consumption	12	0.04	0.48

4.2.Debug Interface

The debug interface uses the CH340X chip to convert UART signals to USB signals and employs a Type-C connector for user convenience, eliminating the need for a serial c onverter chip. When a signal is applied to the baseboard's Type-C debug interface, the yel low UART LED above the connector lights up steadily. The debug interface is located at the lower right of the baseboard, as shown in the figure below.



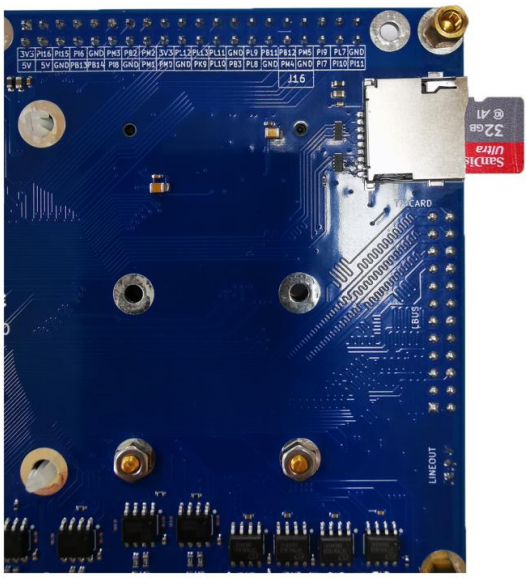
Debug interface diagram

4.3.TF Card Interface

The TF card slot is located on the upper right of the back side of the baseboard. Us ers can purchase a TF card of 16GB or larger, download the corresponding program from the Chengdu Eibot official website, and write it to the card.Alternatively, programs can b e written directly via OTG.When inserting the SD card, pay attention to the orientation, a s shown in the figure below. To eject, lightly press the SD card inward, and it will pop out.

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TF card interface diagram

4.4.Buttons and Indicators

Button Function Table

Button Name	Function	Remarks
RESET	Hardware reset signal	
PWRON	Power-on enable signal	
FEL	Forced programming signal	

Indicator Function Table

Indicator Name	Function	Default State	Remarks
PWR	Power indicator LED	Red, steady on	
RUN	Run indicator LED	Green, blinking	
USER	User indicator LED	Green, blinking	User can customize the corresponding PG9 IO pin
UART	Debug serial indicator LED	Yellow, steady on	
D8	Network indicator LED	Green, off	PCIe interface network indicator, user-customizable

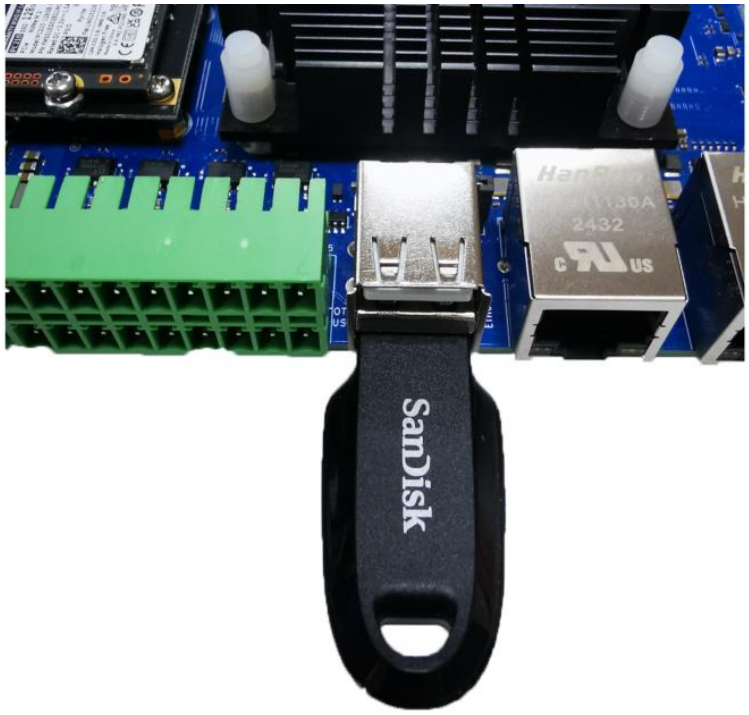
4.5.USB2.0 Interface

This product provides one USB2.0 port, located at the bottom center of the baseboard' s front side, as shown in the USB2.0 interface diagram below. Users can connect external devices such as a mouse, keyboard, or USB flash drive, or attach multiple devices via a

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USB hub. Note that the USB2.0 interface supports HOST mode only and supplies up to 1000 mA of output current. In the dual-row USB connector, the lower port is the USB2.0 interface.



USB2.0 interface diagram

4.6.USB_OTG Interface

The product provides one USB_OTG port, located at the bottom front of the baseboard, as shown in the USB_OTG interface diagram. In the dual-row USB connector, the upper port is the OTG interface. Users can write firmware directly through this interface.

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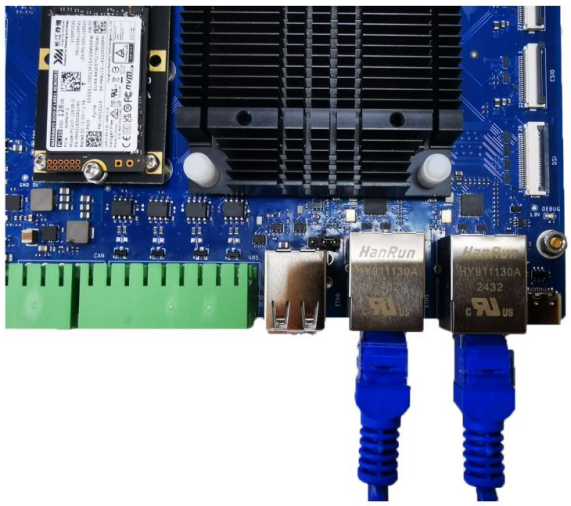


USB_OTG interface diagram

The USB_OTG interface supports both Host and Device modes. Users select the OTG mode via the jumper. When the jumper shorts the right two pins, or when no jumper is fitted, the port operates in Device mode.When the jumper shorts the left two pins, the port operates in Host mode and can supply up to 700 mA of output current.

4.7.Network Interface

Two RJ45 Ethernet ports are located at the lower right of the baseboard's front side, as shown in the figure below:

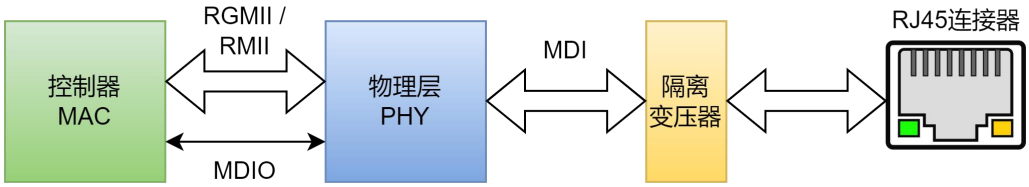


Ethernet interface diagram

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Both Ethernet ports support 10M/100M/1000M adaptive Ethernet controllers. The RJ45 Ethernet interface mainly consists of an Ethernet controller MAC (Media Access Control), an Ethernet physical layer PHY (Physical Layer), Ethernet transformers, and RJ45 connec tors, as shown in the figure below.



RJ45 Ethernet Composition

The baseboard uses the MAE0621A as the physical layer chip, designed with referenc e to the “MAE0621A Design Guide V1.1.” A 25 MHz passive crystal is adopted for the clock source. RJ45 uses a connector with an integrated transformer, so there is no need to design a separate transformer circuit. Note: In PCB layout, the copper area under the RJ 45 connector should be hollowed out to avoid interference with the transformer signals.

The default PHY address for ETH0 is 001 (binary), corresponding to PHYAD[2:0] bei ng configured as PHYAD0, PHYAD1, and PHYAD2 = 001. RXDLY and TXDLY are both set to 1 (enabled), and PLLOFF is set to 0 (disabled).

The default PHY address for ETH1 is 010 (binary), corresponding to PHYAD[2:0] bei ng configured as PHYAD0, PHYAD1, and PHYAD2 = 010. RXDLY and TXDLY are both set to 1 (enabled), and PLLOFF is set to 0 (disabled).

Some functions of the PHY chip require hardware configuration. The specific pins an d settings are shown in the table below:

PHY Pin Configuration Table

PIN NAME	PIN NO.	I/O	DESCRIPTION
PHYAD0	22	O/LI/PU	PHYAD[2:0]. Sampled on reset. The PHY address selects MII management PHY address.
PHYAD1	27	O/LI/PD	
PHYAD2	26	O/LI/PD	
PLLOFF	23	O/LI/PD	ALDPS Mode PLL Off Configuration. Pull up to stop PLL when entering ALDPS mode.
TXDLY	24	O/LI/PD	RGMII Transmit Clock Timing Control. Pull up to add 2ns delay to TXC for TXD latching.
RXDLY	25	O/LI/PU	RGMII Receive Clock Timing Control.

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			Pull up to add 2ns delay to RXC for RXD latching.
CFG_EXT	32	O/LI/PD	RGMII and SMI I/O Pad Power Source Mode Configuration. When pulling down CFG_EXT, CFG_LDO[1:0] represent LDO output voltage setting for IO pad: 2'b00: Reserved; 2'b01: 2.5V from internal LDO; 2'b10: 1.8V from internal LDO; 2'b11: 1.5V from internal LDO. When pulling up CFG_EXT, CFG_LDO[1:0] represent the input voltage of IO pad is selected from external power: 2'b00: 3.3V from external power; 2'b01: 2.5V from external power; 2'b10: 1.8V from external power; 2'b11: 1.5V from external power.
CFG_LDO0	33	O/LI/PU	
CFG_LDO1	34	O/LI/PD	

LED Status Indicator Table

Connection Status	LED Status	Transmission Status	LED Status
10M connection	Both LEDs off	10M transmission	Both LEDs off
100M connection	Yellow LED on	100M transmission	Yellow LED blinking
1000M connection	Green LED on	1000M transmission	Green LED blinking

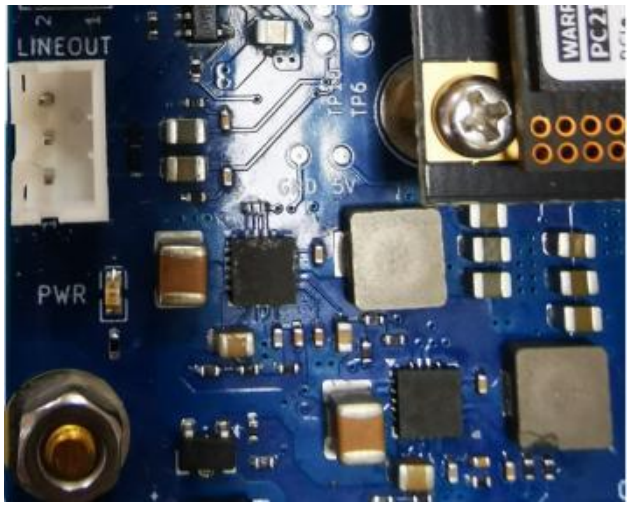
4.8.Audio Interface

A 1 × 3-pin, 2.0 mm-pitch connector provides the LINEOUTLP and LINEOUTLN si gnals. Users can hook up an external power-amplifier stage; note that each output is alrea dy AC-coupled with a 47 µF series capacitor.

4.8 Audio Interface The audio interface uses a 1×3-pin, 2.0 mm-pitch connector, provi ding LINEOUTLP and LINEOUTLN audio signals. Users can attach an external power am plifier; note that each output is AC-coupled with a 47 µF coupling capacitor. One audio DAC channel: 16-bit and 20-bit sampling resolution; 8 kHz to 192 kHz sampling rate. Su pports dynamic-range controller adjustment of DAC playback; 128×20-bit FIFO for DAC d ata transfer; programmable FIFO threshold; supports interrupt and DMA transfers. As show n below.

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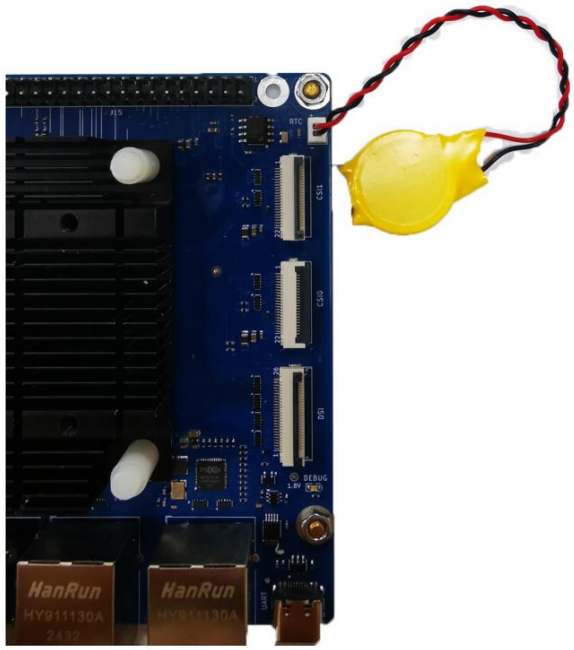
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Audio Interface Diagram

4.9.RTC

The baseboard uses a dedicated RTC chip to provide clock data. The chip features au tomatic power-fail detection and power-switching circuitry. The main power is supplied by a +5 V source, and the backup power by a +3 V battery. The battery voltage must rema in between 2.0 V and 3.5 V for normal operation. In battery-powered mode, the oscillator' s consumption is less than 500 nA. A CR2032 battery is recommended. The battery interf ace uses a 1×2-pin, 1.25 mm-pitch connector located at the upper right of the front side of the baseboard, as shown below.



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RTC Battery Interface Diagram

4.10.MIPI CSI interface

The MIPI CSI camera interface is located on the front right side of the base board. There are two interfaces: MIPI CSI0 and MIPI CSI1. Both use a 22-pin 0.5 mm FPC flex cable for connection. As shown in the figure below, this interface is compatible with the CSI interface of the Raspberry Pi 5. You can purchase a Raspberry Pi 5 camera via e-commerce platforms to use it. Alternatively, you can buy the cameras for Raspberry Pi 4B and 3B+ and use an adapter cable to convert from 15-pin to 22-pin.



MIPI CSI CSI interface Diagram

The parallel CSI interface supports a maximum pixel clock of 148.5MHz and is compatible with BT.601, BT.665, BT.1120, and the Digital Camera Protocol. Each interface uses 2 lanes, supporting BT.656 up to 720P@30fps resolution, and BT.1120 up to 1080P@30fps resolution. When connecting, pay attention to the pin numbers to prevent reverse insertion. Refer to the pin number labels next to the connector, which must correspond to the pins on the camera side. The detailed pin definitions are listed in the table below.

MIPI CSI0 Interface Definition Table

Pin Number	Pin Definition	Function Description	Pin Voltage Level
1	GND	GND	0V
2	MCSIC-D0N	CSI differential signal	1V8
3	MCSIC-D0P	CSI differential signal	1V8
4	GND	GND	0V
5	MCSIC-D1N	CSI differential signal	1V8

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6	MCSIC-D1P	CSI differential signal	1V8
7	GND	GND	0V
8	MCSIC-CKN	CSI differential clock signal	1V8
9	MCSIC-CKP	CSI differential clock signal	1V8
10	GND	GND	0V
11	/	NC	/
12	/	NC	/
13	GND	GND	0V
14	/	NC	/
15	/	NC	/
16	GND	GND	0V
17	CSI0_PWR_EN	Power enable signal	3V3
18	NC	/	/
19	GND	GND	0V
20	TWI1-SCK	I2C clock signal	3V3
21	TWI1-SDA	I2Cdata signal	3V3
22	VDD_CSI0	3.3Vpower supply	3V3

MIPI CSI1 Interface Definition Table

Pin Number	Pin Definition	Function Description	Pin Voltage Level
1	GND	GND	0V
2	MCSID-D0N	CSI differential signal	1V8
3	MCSID-D0P	CSI differential signal	1V8
4	GND	GND	0V
5	MCSID-D1N	CSI differential signal	1V8
6	MCSID-D1P	CSI differential signal	1V8
7	GND	GND	0V
8	MCSID-CKN	CSI differential clock signal	1V8
9	MCSID-CKP	CSI differential clock signal	1V8
10	GND	GND	0V
11	/	NC	/
12	/	NC	/
13	GND	GND	0V
14	/	NC	/
15	/	NC	/
16	GND	GND	0V
17	CSI1_PWR_EN	Power enable signal	3V3
18	NC	/	/

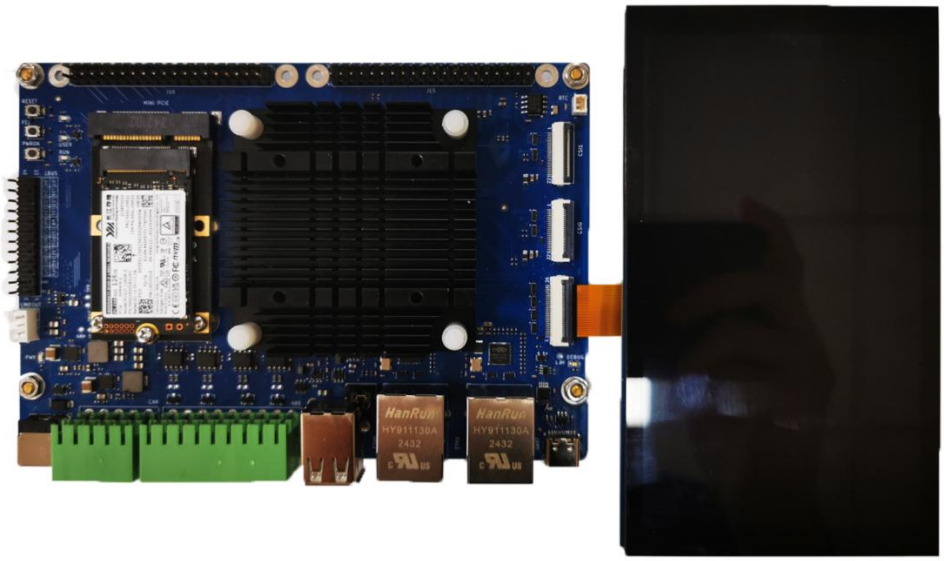
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19	GND	GND	0V
20	TWI0-SCK	I2C clock signal	3V3
21	TWI0-SDA	I2C data signal	3V3
22	VDD_CSI1	3.3V power supply	3V3

4.11.MIPI DSI interface

A single MIPI DSI display interface is located at the bottom right of the front side o f the baseboard, as shown in the figure below. The DSI display interface uses a 4-lane M IPI DSI and supports up to 2.5K@60fps and 4K@45fps.



MIPI DSI Display Interface Diagram

The DSI display interface uses a 26-pin 0.5mm pitch FPC connector. A 26-pin 0.5m m FPC flexible flat cable can be used to connect to the display. When connecting, pay at tention to the pin numbers to prevent reverse insertion. Refer to the pin number labels ne xt to the connector, which must correspond to the pins on the display side. The detailed pin definitions are listed in the table below. It is recommended to use the EBYTE ECA11 -5LM1xxxC series MIPI dedicated display panel. MIPI DS

MIPI DSI Interface Definition Table

Pin Number	Pin Definition	Function Description	Pin Voltage Level
1	GND	GND	0V
2	DSI_LCD_RESET	LCD reset signal	1V8
3	GND	GND	0V
4	DSI-D3N	DSI differential signal	1V8
5	DSI-D3P	DSI differential signal	1V8

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6	GND	GND	0V
7	DSI-D2N	DSI differential signal	1V8
8	DSI-D2P	DSI differential signal	1V8
9	GND	GND	0V
10	DSI-D0N	DSI differential signal	1V8
11	DSI-D0P	DSI differential signal	1V8
12	GND	GND	0V
13	DSI-CKN	DSI differential clock signal	1V8
14	DSI-CKP	DSI differential clock signal	1V8
15	GND	GND	0V
16	DSI-D1N	DSI differential signal	1V8
17	DSI-D1P	DSI differential signal	1V8
18	GND	GND	0V
19	DSI-LCD-ID	LCD detection pin	/
20	DSI-BL-CTR	Backlight control signal	3V3
21	DSI-TP-RST	Touch screen reset signal	3V3
22	TWI4-SDA	I2C data signal	3V3
23	TWI4-SCK	I2C clock signal	3V3
24	DSI-TP-INT	Touch screen interrupt signal	3V3
25	MIPI_DSI_VCC	5V power supply	5V
26	MIPI_DSI_VCC	5V power supply	5V

4.12.MINI PCIe interface

One MINI PCIe interface is located on the left side of the front of the baseboard, as shown in the figure below. The interface transmits PCIe signals and supports PCIe 2.1. Users can expand storage modules, network cards, wireless communication modules, USB 3.0 expansion cards, serial port cards, graphics cards, etc. via the MINI PCIe interface. D esigned with mounting holes for full-size and half-size cards, it supports the installation of both full-size and half-size network cards.

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MINI PCIe Interface Diagram

The MINI PCIe interface definition is listed in the table below:

MINI PCIe Interface Definition Table

Pin Number	Pin Definition	Function Description
1	NC	/
2	VDD_3V3	3.3V power supply
3	NC	/
4	GND	GND
5	NC	/
6	NC	/
7	NC	/
8	NC	/
9	GND	GND
10	NC	/
11	PCIE21-REFCLKN	PCIe_CLKN differential signal
12	NC	/
13	PCIE21-REFCLKP	PCIe_CLKN differential signal
14	NC	/
15	GND	GND
16	NC	/
17	NC	/
18	GND	GND
19	NC	/
20	NC	/
21	GND	GND
22	PCIE-PERSTN	PCIe reset signal
23	PCIE21-RXN	PCIe_RX_DN differential signal
24	VDD_3V3	3.3V power supply
25	PCIE21-RXP	PCIe_RX_DP differential signal
26	GND	GND

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27	GND	GND
28	NC	/
29	GND	GND
30	NC	/
31	PCIE21-TXN	PCIe_TX_DN differential signal
32	NC	/
33	PCIE21-TXP	PCIe_TX_DP differential signal
34	GND	GND
35	GND	GND
36	NC	/
37	GND	GND
38	NC	/
39	VDD_3V3	3.3V power supply
40	GND	GND
41	VDD_3V3	3.3V power supply
42	VDD_3V3	3.3V power supply
43	GND	GND
44	NC	/
45	NC	/
46	NC	/
47	NC	/
48	NC	/
49	NC	/
50	GND	GND
51	NC	/
52	VDD_3V3	3.3V power supply

4.13.LOCAL BUS interface

One LOCAL BUS interface uses a 2x12Pin 2.54 pitch header and is located on the l eft side of the front, as shown in the figure below.

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LOCAL BUS Interface Diagram

LOCAL BUS interface uses a 2x12Pin 2.54 pitch header and is located on the left side of the front, as shown in the figure below. Bus Interface Diagram The LOCAL BUS interface supports 8-bit wide data transmission; address and data multiplexed access; parity check; synchronous read/write of 128 × 8 FIFO (AHB clock domain); read/write of 16 × 8 buffer (local bus clock domain); up to 400MHz AHB clock and up to 100MHz local bus clock.

The LOCAL BUS interface definition is listed in the table below:

LOCAL BUS Interface Definition Table

Pin Number	Pin Definition	Function Description
1	VDD_LBUS	5V Power Supply
2	VDD_LBUS	5V Power Supply
3	GND	GND
4	GND	GND
5	LBUS-RESET	Local Bus Reset Signal
6	LBUS-DP0	Local Bus Parity Signal
7	LBUS-DRQ	Local Bus Asynchronous Request
8	LBUS-BURST2	Local Bus Burst Command
9	LBUS-LBE	Local Bus Byte Enable
10	LBUS-BURST1	Local Bus Burst Command
11	LBUS-ALE	Local Bus Address Lock Enable
12	LBUS-BURST0	Local Bus Burst Command
13	LBUS-CS0	Local Bus Chip Select
14	LBUS-LCLK	Local Bus Clock Signal

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15	LBUS-WR	Local Bus Write Signal
16	LBUS-READY	Local Bus Ready Signal
17	LBUS-LD1	Local Bus Data Signal
18	LBUS-LD0	Local Bus Data Signal
19	LBUS-LD3	Local Bus Data Signal
20	LBUS-LD2	Local Bus Data Signal
21	LBUS-LD5	Local Bus Data Signal
22	LBUS-LD4	Local Bus Data Signal
23	LBUS-LD7	Local Bus Data Signal
24	LBUS-LD6	Local Bus Data Signal

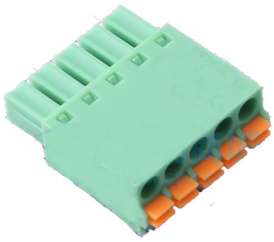
4.14.CAN Bus Interface

Provides 4 channels of CAN bus interfaces, utilizing a single 2x5 pin 3.81 mm Phoe nix connector located at the lower left of the front panel. As shown in the figure below:



CAN Bus Interface Diagram

Users may purchase matching terminal blocks for connection; recommended model: K F2EDGKN-3.81-5P, as shown in the figure below.



CAN Interface Terminal Block KF2EDGKN-3.81-5P Diagram

The evaluation board has a built-in CAN transceiver chip with a 120Ω termination re sistor. The CAN bus interface uses differential signaling and complies with “ISO 11898” a

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nd “SAE J2284-1 to SAE J2284-5” standards. It supports CAN 2.0A and 2.0B protocol sp ecifications and is compatible with the AUTOSAR automotive open system architecture. It also supports the SAE J1939 standard with up to 64 dedicated receive buffers and up to 32 dedicated transmit buffers. The interface can be directly used in automotive applicatio ns and industrial control systems.

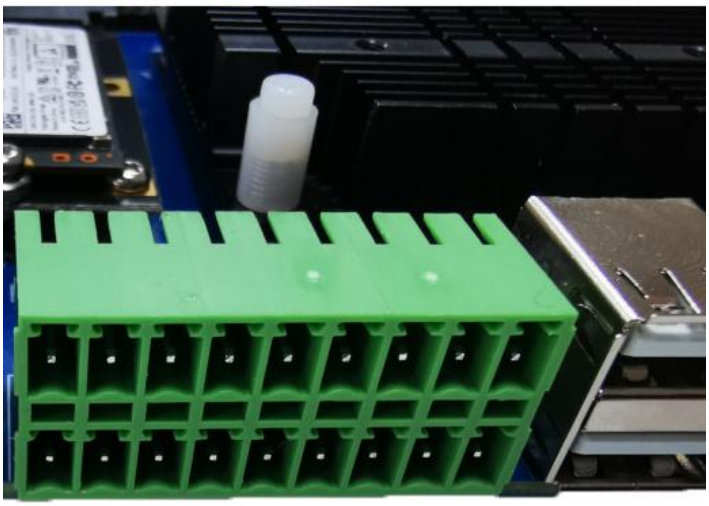
See the table below for detailed definitions of the CAN bus interface pins.

CAN Bus Interface Pin Definition Table

Pin Number	Pin Definition	Pin Number	Pin Definition
1	CAN2H	2	CAN3H
3	CAN2L	4	CAN3L
5	GND	6	GND
7	CAN0H	8	CAN1H
9	CAN0L	10	CAN1L

4.15.RS485 Interface

Provides 8 channels of RS485 bus interfaces, utilizing a single 2x9 pin 3.81 mm Phoe nix connector located at the bottom front panel. As shown in the figure below:



RS485 Bus Interface Diagram

Users may purchase a matching terminal block; recommended model: KF2EDGKN-3.8 1-9P, as shown in the figure below:

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RS485 Interface Terminal Block KF2EDGKN-3.81-9P Diagram

Each 485 interface supports 1/8 unit load, allowing up to 256 devices to connect to t he bus. The bus port has ESD protection capability (HBM) exceeding 15 kV, a voltage tol erance of ±15 V, operates in half-duplex mode, and is low power consumption. It complies with the TIA/EIA-485 standard. Detailed definitions are provided in the table below:

RS485 Interface Pin Definition Table

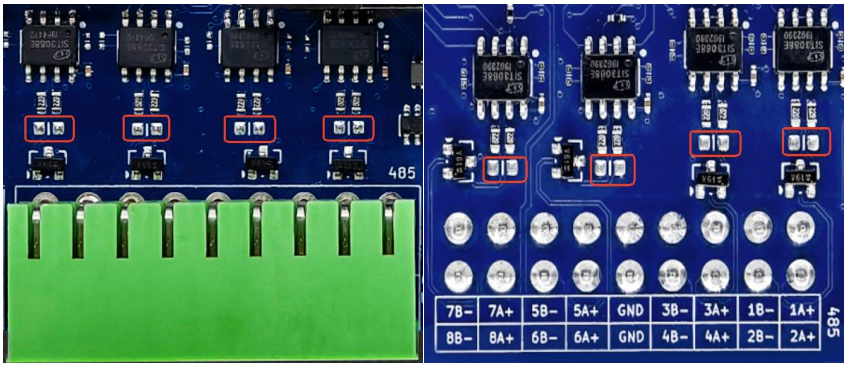
Pin Number	Pin Definition	Pin Number	Pin Definition
1	RS485_1A	2	RS485_2A
3	RS485_1B	4	RS485_2B
5	RS485_3A	6	RS485_4A
7	RS485_3B	8	RS485_4B
9	GND	10	GND
11	RS485_5A	12	RS485_6A
13	RS485_5B	14	RS485_6B
15	RS485_7A	16	RS485_8A
17	RS485_7B	18	RS485_8B

Longer transmission cables lead to greater current through the termination resistor, cau sing significant voltage drop. As a result, the differential voltage at the receiver end decre ases, which negatively affects data integrity. On an RS-485 bus, higher load levels reduce the differential voltage output by the transceiver. Since the RS-485 receiver detects signals based on the voltage difference between the A and B lines, and this threshold is ±200 m V, communication fails when the voltage drops below this level.

Therefore, the evaluation board does not come with pre-soldered termination resistors by default, but it does provide reserved solder pads for 0603 packaged resistors. If users operate under conditions with long transmission distances and high communication speed where signal integrity is critical, they may manually solder a 120 Ω termination resistor to enhance signal quality.

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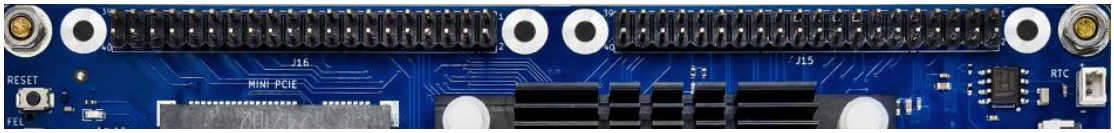
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RS485 Bus Termination Resistor Location Diagram

4.16.Raspberry Pi Expansion Interfaces

Two standard Raspberry Pi 2x20 Pin 2.54 mm expansion headers are designed and pos itioned at the upper front section of the baseboard, as shown in the figure below.



Raspberry Pi Expansion Interface Diagram

he IO interface supports multiplexing functions, including up to 2 SPI interfaces, 2 I2 S interfaces, 1 SDC interface, 3 CAN interfaces (TTL level), 7 I2C interfaces, and 6 UA RT interfaces. Users may configure the interface according to specific needs. Additionally, each expansion header provides 3.3V and 5V power outputs, each supporting up to 1000 mA of current. Detailed pin definitions are provided in the table below.

J15 Raspberry Pi Expansion Header Pin Definition Table

Pin Number	Pin Definition	Pin Voltage Level	Pin Number	Pin Definition	Pin Voltage Level
1	3V3	3V3	2	5V	5V
3	PI5/TWI5-SDA	3V3	4	5V	5V
5	PI4/TWI5-SCK	3V3	6	GND	0V
7	PG10/I2S1-MCLK	3V3	8	PB4/UART8-TX	3V3
9	GND	0V	10	PB5/UART8-RX	3V3
11	PG0/SDC1-CLK	3V3	12	PG11/I2S1-BCLK	3V3
13	PG1/SDC1-CMD	3V3	14	GND	0V
15	PG2/SDC1-D0	3V3	16	PG3/SDC1-D1	3V3
17	3V3	3V3	18	PG4/SDC1-D2	3V3
19	PC2/SPI0-MOSI	1V8	20	GND	0V
21	PC4/SPI0-MISO	1V8	22	PG5/SDC1-D3	3V3
23	PC12/SPI0-CLK	1V8	24	PC3/SPI0-CS0	1V8
25	GND	0V	26	PC7/SPI0-CS1	1V8
27	PH7/TWI6-SDA	3V3	28	PH6/TWI6-SCK	3V3

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29	PD12/UART8-RTS	3V3	30	GND	0V
31	PD13/UART8-CTS	3V3	32	PD18/PWM1-8	3V3
33	PH4/PWM1-4	3V3	34	GND	0V
35	PG12/I2S1-LRCK	3V3	36	PL6	3V3
37	PI12	3V3	38	PG14/I2S1-DIN0	3V3
39	GND	0V	40	PG13/I2S1-DOUT0	3V3

J16 Raspberry Pi Expansion Header Pin Definition Table

Pin Number	Pin Definition	Pin Voltage Level	Pin Number	Pin Definition	Pin Voltage Level
1	3V3	3V3	2	5V	5V
3	PI16/TWI2-SDA	3V3	4	5V	5V
5	PI15/TWI2-SCK	3V3	6	GND	0V
7	PI6/I2S0-MCLK	3V3	8	PB13/UART7-TX	3V3
9	GND	0V	10	PB14/UART7-RX	3V3
11	PM3	1V8	12	PI8/I2S0-BCLK	3V3
13	PB2	3V3	14	GND	0V
15	PM2	1V8	16	PM1/S-TWI0-SDA	1V8
17	3V3	3V3	18	PM0/S-TWI0-SCK	1V8
19	PL12/S-SPI0-MOSI	3V3	20	GND	0V
21	PL13/S-SPI0-MISO	3V3	22	PK9	3V3
23	PL11/S-SPI0-CLK	3V3	24	PL10/S-SPI0-CS0	3V3
25	GND	0V	26	PB3	3V3
27	PL9/S-TWI1-SDA	3V3	28	PL8/S-TWI1-SCK	3V3
29	PB11/UART7-RTS	3V3	30	GND	0V
31	PB12/UART7-CTS	3V3	32	PM4/S-PWM0-2	1V8
33	PM5/S-PWM0-3	1V8	34	GND	0V
35	PI9/I2S0-LRCK	3V3	36	PI7/I2S0-DIN2	3V3
37	PL7	3V3	38	PI10/I2S0-DIN1	3V3
39	GND	0V	40	PI11/I2S0-DOUT1	3V3

4.17.TP Test Points

Some GPIO and ADC interfaces on the baseboard are unused and not routed to expansion headers. Instead, they are exposed as TP test points. If needed, users can refer to the table below to utilize corresponding TP point functions.

GPADC supports 12/10-bit resolution with a maximum sampling rate of 2 MHz, and an input signal range of 0 to 1.8 V. LRADC supports 6-bit resolution with a maximum sampling rate of 2 kHz, and an input signal range of 0 to 1.35 V.

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TP Point Definition Table

TP Point Number	TP Point Definition	TP Point Number	TP Point Definition
TP5	GPADC2-3	TP19	GPADC1-8
TP6	GPADC2-2	TP20	GPADC2-8
TP7	GPADC1-3/TP-Y2	TP21	GPADC2-9
TP8	GPADC1-2/TP-Y1	TP22	GPADC3-0
TP9	LINEOUTLP	TP23	AP-NMI
TP10	LINEOUTLN	TP24	PD10
TP11	CK32K-OUT	TP25	PD11
TP12	CK24M-OUT	TP26	PE15
TP13	LRADC0	TP27	PD19
TP14	GPADC1-9	TP28	PA0
TP15	GPADC2-7	TP29	PA1
TP16	GPADC1-7	TP30	PD15
TP17	GPADC2-1	TP31	PK8
TP18	GPADC2-6	TP32	GPADC2-5

5. Software Resources

The ECB33-PGB single-board computer runs an operating system based on the Linux 5.15 kernel. Upon delivery, it includes all embedded Linux development essentials: the cr oss-compilation toolchain Buildroot source code, U-boot source code, Linux kernel and dri ver module sources, as well as various development and debugging tools compatible with Windows and Linux desktop environments.

Operating System:

1. Linux file system built with Buildroot
2. Linux file system ported from Debian

System Source Code:

1. U-boot 2018
2. Kernel 5.15
3. BuildRoot 2022.05
4. Debian 11

Development Environment & Tools:

1. USB flashing tool: PhoenixSuit
2. SD card flashing tool: PhoenixCard

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System software resources are listed in the table below:

System Software Resource Table

Category	Name	Description	Source Code
SPL	spl-pub	Boot0, U-Boot Loader	<SDK>/brandy/brandy-2.0/spl-pub/
BOOT	u-boot 2018.07	Boot Program	<SDK>/brandy/brandy-2.0/u-boot-2018/
Kernel	Kernel 5.15.147	Linux Kernel	<SDK>/kernel/linux-5.15/
Bsp	BSP	Allwinner-related Kernel Drivers and Device Tree	<SDK>/bsp/
Device Driver	Audio	Built-in Audio Driver	bsp/drivers/sound/platform/*
	AWlink	CAN Driver	bsp/awlink
	GMAC	Built-in MAC Driver	bsp/gmac
	STMMAC	Built-in MAC Driver	Bsp/stmmac
	GPADC	GPADC Driver	bsp/gpadc
	GPIO	GPIO Driver	bsp/pinctrl/*
	drm	Display-related Driver	bsp/drm/panel/*
	LRADC	Key Module Driver	bsp/lradc/*
	MMC	MMC Driver	bsp/mmc/*
	SPI	SPI Driver	bsp/spi/*
	TWI	I2C Driver	bsp/twi/*
	UART	Serial Port Driver	bsp/uart/*
	VIN	Dedicated Camera Driver	bsp/vin/modules/sensor/*
	PCIe	PCI Driver	bsp/pci/*
	IR	Infrared Driver	bsp/ir-rx/* bsp/ir-tx/*
操作系统	Buildroot 202205	Buildroot Version 202205	<SDK>/buildroot/buildroot-202205
	Debian	Debian 11	<SDK>/debian/compressed_files/
开发工具	PhoenixSuit	USB Flashing Tool	/tools/PhoenixSuit
	PhoenixCard	SD Card Flashing Tool	/tools/PhoenixCard

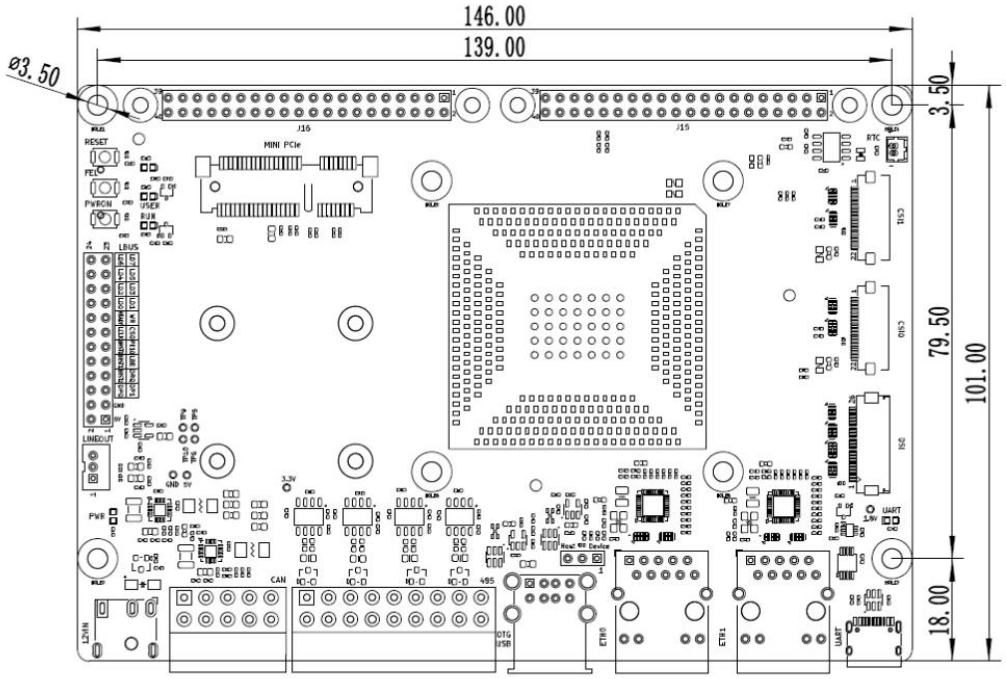
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6. Mechanical Dimensions

Units: mm; Tolerance: ±0.1 mm.

Front view dimensions are illustrated in the figure below:



Baseboard Front Mechanical Dimension Diagram

7. Reference Documents

- T536_Datasheet_V0.91.pdf
- ECK33-B_ProductManual_EN_V1.0.pdf
- MAE0621A Design Guide V1.1.pdf

8. Revision Notes

Revision Notes Table

Version	Revision Details	Revision Date	Compiled By	Proofread By	Approved By
V1.0	Initial release	25-6-26	WJ	LJQ	WFX
V1.1	Supplement to Section 4.16: Raspberry Pi Expansion Interface Pin-Level Description	25-8-21	WJ	LJQ	WFX

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