Product Manual
ECB32-PGB Single board computer



Chengdu Ebyte Electronic Technology Co.,Ltd.

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1.Introduction

1.1. Brief Introduction

ECB32-PGB is a single board based on EBYTE ECK32-T527B series core board. The core board is in 381Pin LGA package and can be soldered to the backplane by SMT. The baseboard design makes full use of the core board interfaces, leading to include MIPI DSI display interface, MIPI CSI camera interface, HDMI display interface, DP display interface, USB2.0, USB OTG, debugging interfaces, Ethernet interfaces, audio interfaces, MINI PCIE interfaces, and a wealth of extended GPIO interfaces. The design grade of single board is higher than common development boards, which can not only be used for core board function verification, but also can be directly used in industrial scenarios in batch.

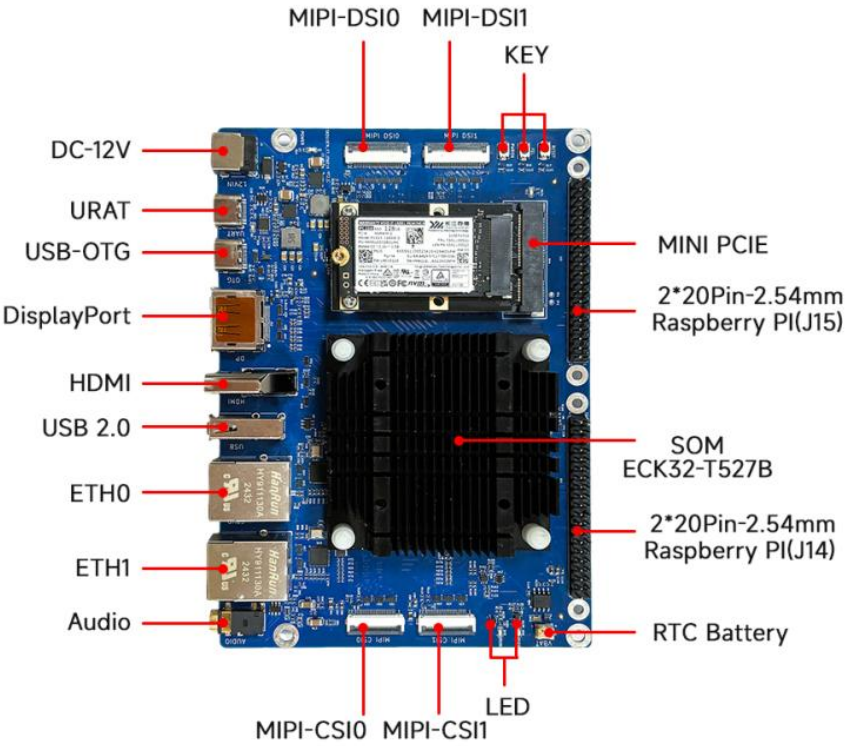
EVERBUILT provides stable reference design and perfect software development environment, including hardware design documents, software development manuals, and open source schematics, package files and PCB design files. It can effectively help users to verify the core board functions, improve development efficiency, shorten the development cycle, optimize the design quality, and accelerate product development and time-to-market.

ECB32-PGB series of single-board computer contains two specific product models. They have the same baseboard, two models are mounted two different types of core boards, customers can choose the appropriate model according to their needs. For details of product selection, please refer to the Product Selection section.

The functional diagram of the single board machine is as follows:

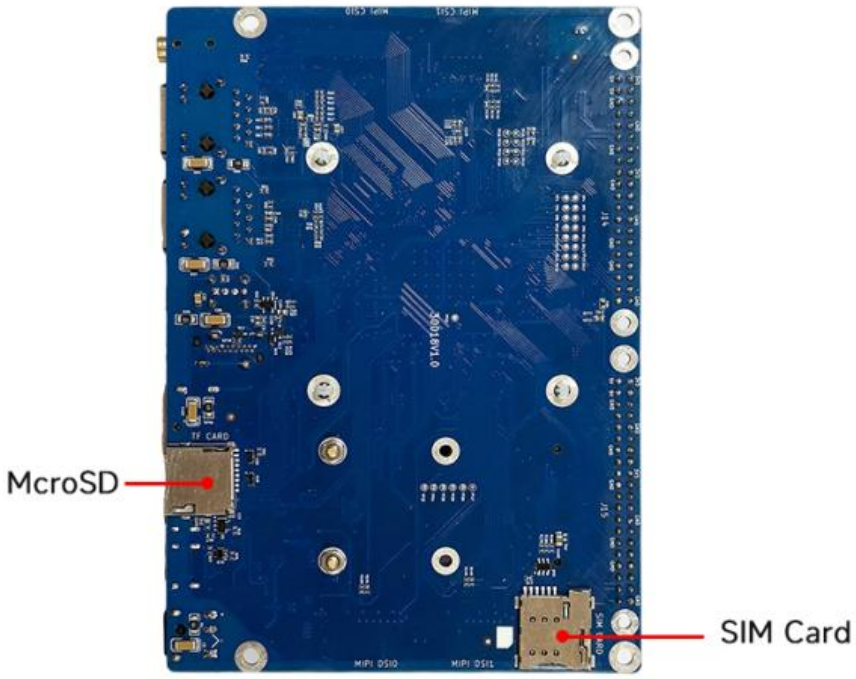
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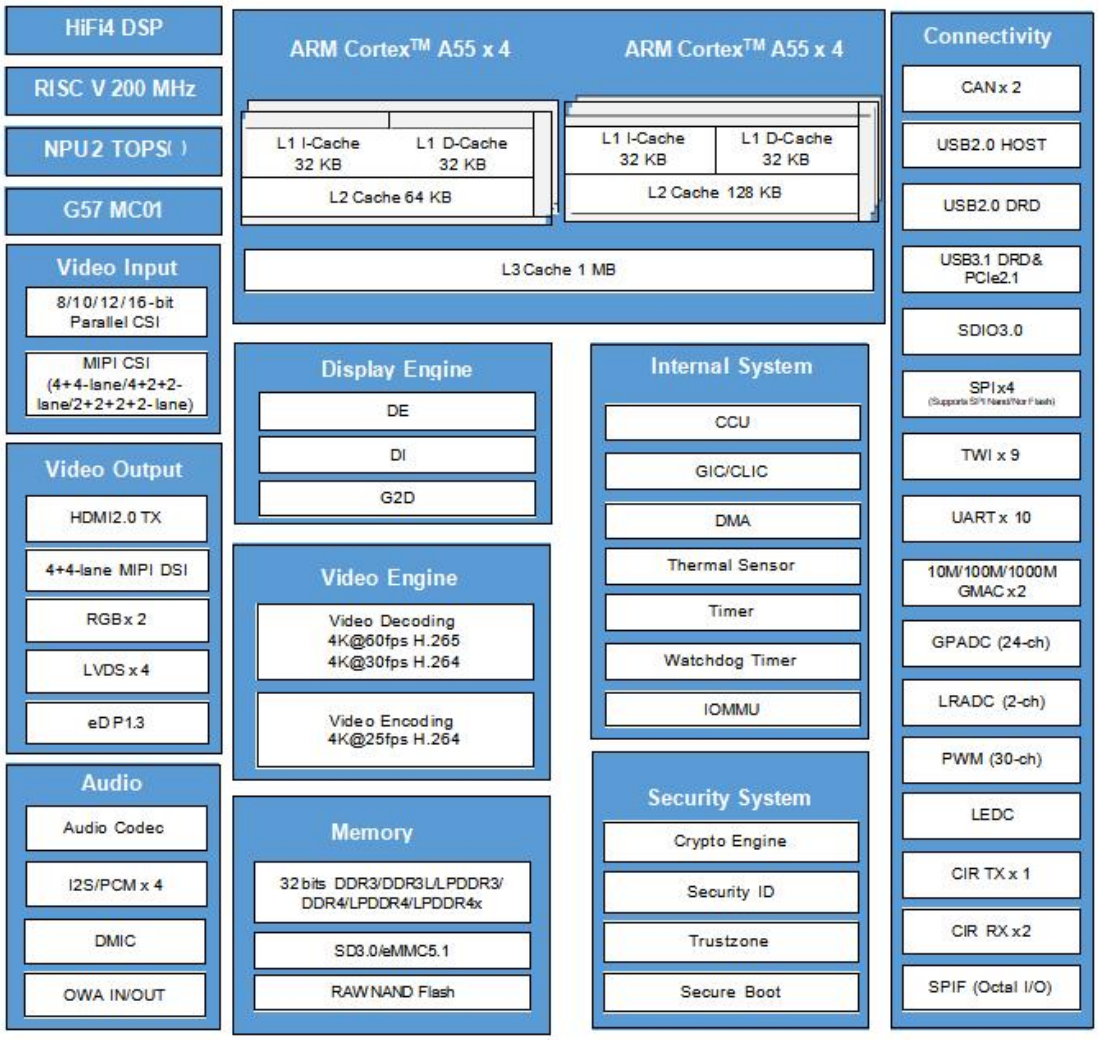
single-board functional description diagram

1.2. Allwinner T527 Chip Introduction

Allwinner T527 series are SOC products with high performance octa-core Cortex-A55 AI platform for commercial, industrial and automotive applications. The chip family integ rates an octa-core Cortex-A55 CPU, HiFi4 DSP, 2 TOPS NPU, ARM G57 MC1 GPU, 32 -bit DDR3/DDR3L/DD4/LPDDR3/LPDDR4/LPDDR4X DRAM, high-speed interfaces (PCIe2. 1 and USB3.1), and automotive interface (CAN), Multiple video output interfaces (2*RGB/ 2*Dual-LVDS/2*MIPI-DSI/HDMI/eDP) and video input interface (MIPI CSI). The chip fam ily supports 4K@60fps H.265 decoder, 4K@30fps H.264 decoder, 4K@25fps H.264 encod er, DI and AWonder systems, providing users with a smooth experience and professional AI visuals.

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T527 System Function Block Diagram

1.3. ECK32-T527B Series Core Board Introduction

ECK32-T527B series core board is carefully designed based on Allwinner's T527 series processor, adopting the new LGA interface form of high-performance, low-power, high-reliability, fully localized industrial-grade embedded core board. It can be widely used in content sharing and self-service terminals, intelligent manufacturing, and other electronic commercial and industrial equipment. For details, please refer to ECK32-T527B Core Board Product Manual V1.0.

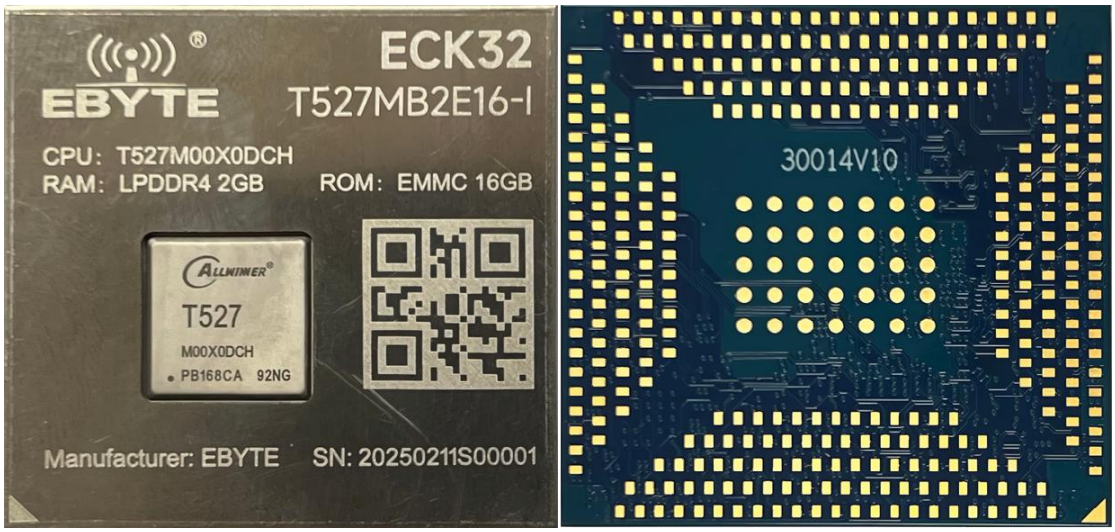
ECK32-T527B series core boards contain 4 specific product models, all of which are designed with fully localized industrial-grade devices. They mainly have some differences in NPU support, DRAM memory capacity, eMMC storage capacity, operating temperature environment, etc. Customers can choose the right model by themselves according to their n

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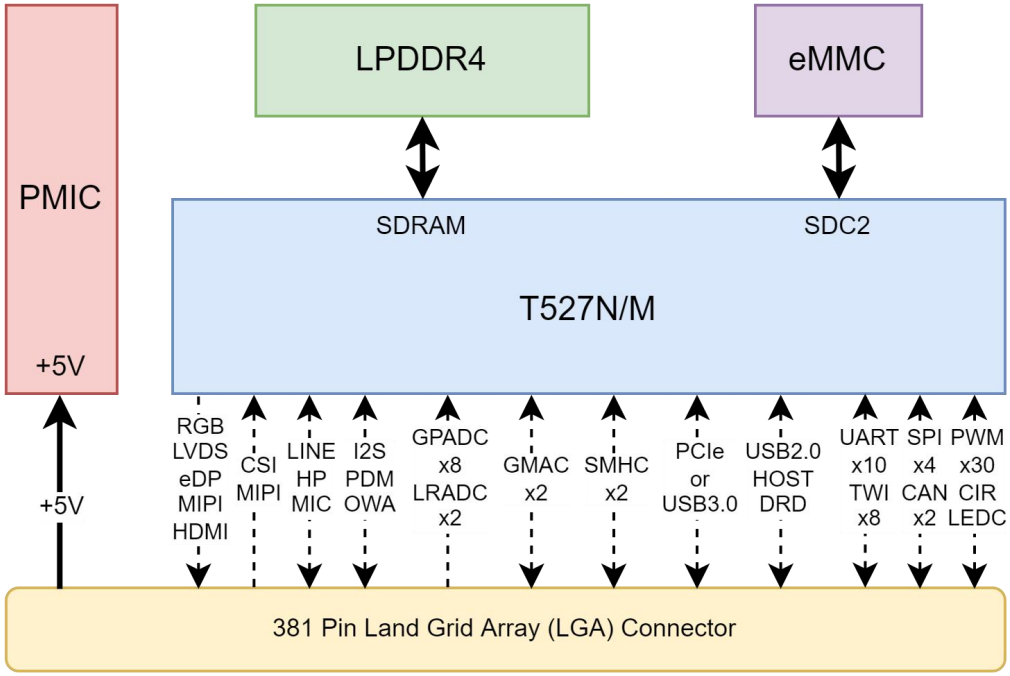
eeds. For details of product selection, please refer to the product selection chapter of ECK 32-T527B Core Board Product Manual V1.0.

The front physical drawing of ECK32-T527B series core board (no device on the bot tom side of the product) is as follows:



Front view of ECK32-T527B series core boards

ECK32-T527B series core board function block diagram is as follows:



1.4. Typical applications

- Industrial control baseboards;
- automotive electronics;

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- industrial all-in-one;
- Smart Cities;
- Tablet PCs;
- IoT gateway;
- Advertising All-in-One;
- Robotics.

2. Product Selection

2.1. Model Configuration

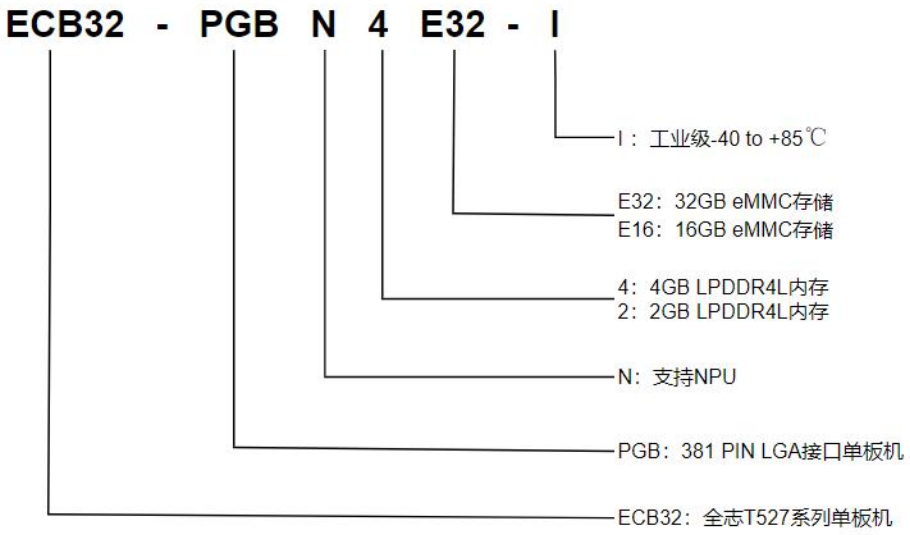
ECB32-PGB series of single-board computer selection and configuration table is shown in the following table:

Product Selection and Configuration Table

No	Model	Core Board Model	RAM	Memory	Operating temperature
1	ECB32-PGBN4E32-I	ECK32-T527BN4E32-I	4GB LPDDR4	32GB eMMC	Chinese industrial grade -40℃ ~ 85℃
2	ECB32-PGB2E16-I	ECK32-T527B2E16-I	2GB LPDDR4	16GB eMMC	Chinese industrial grade -40℃ ~ 85℃

2.2. Model code

The description of the product model code is shown below:



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3.Specification parameters

3.1. Functional parameters

ECB32-PGB Single Board Function Parameter Table

Power Input	1 channel DC socket, 12V_5A input;
HDMI	1 channel HDMI display interface, maximum resolution support 4K@60fps;
DisplayPort	1 channel 4lane DP HD display interface, the maximum resolution support 2.5K@60fps and 4K@30fps;.
DSI	2-way 26Pin 4lane MIPI DSI display interface, maximum resolution support 2.5K@60fps and 4K@45fps, support touch screen and backlight adjustment；
CSI	2-way 22Pin 4lane MIPI CSI camera interface, support camera power and flash control;
MINI PCIE	1 channel PCIE2.1x1 lane, 5Gbps/lane, support MINI PCIE interface;
USB HOST	1 lane USB2.0 HOST;
USB OTG	1 lane USB OTG, Type-C interface;
Network Port	2-way 10/100/1000M adaptive RJ45 Ethernet port;
TF card	1 TF card slot, support plug detection;
Audio	1 channel 3.5MM audio interface, support headphone output and microphone input;
Debugging	1 way UART debugging serial port, Type-C interface;
GPIO	2 groups of 2.54mm2x20Pin standard RPI expansion interface, multiplexing 4-way I2C, 2-way I2S, 2-way SPI, 1-way SDC, 3-way UART, 2-way CAN;
Pushbuttons	1 RESET button; 1 PWRON button; 1 FEL button;;
Indicator Lights	1 power indicator; 1 run indicator; 1 user indicator; 1 debugging indicator; 1 x 4G network indicator;
Watchdog	Support on-chip watchdog function;
RTC	1-way 1.25mm 1x2Pin RTC battery holder;
TP Point	27 GPIOs, 2 GPADCs;

3.2. Environmental characteristics

ECB20-PG6Y28C-I Test Chassis Environmental Characteristics Table

Working Temperature	Industrial Grade: -40℃ ~ 85℃ (environment with good heat dissipation conditions);
Storage	-40℃ ~ 85℃;

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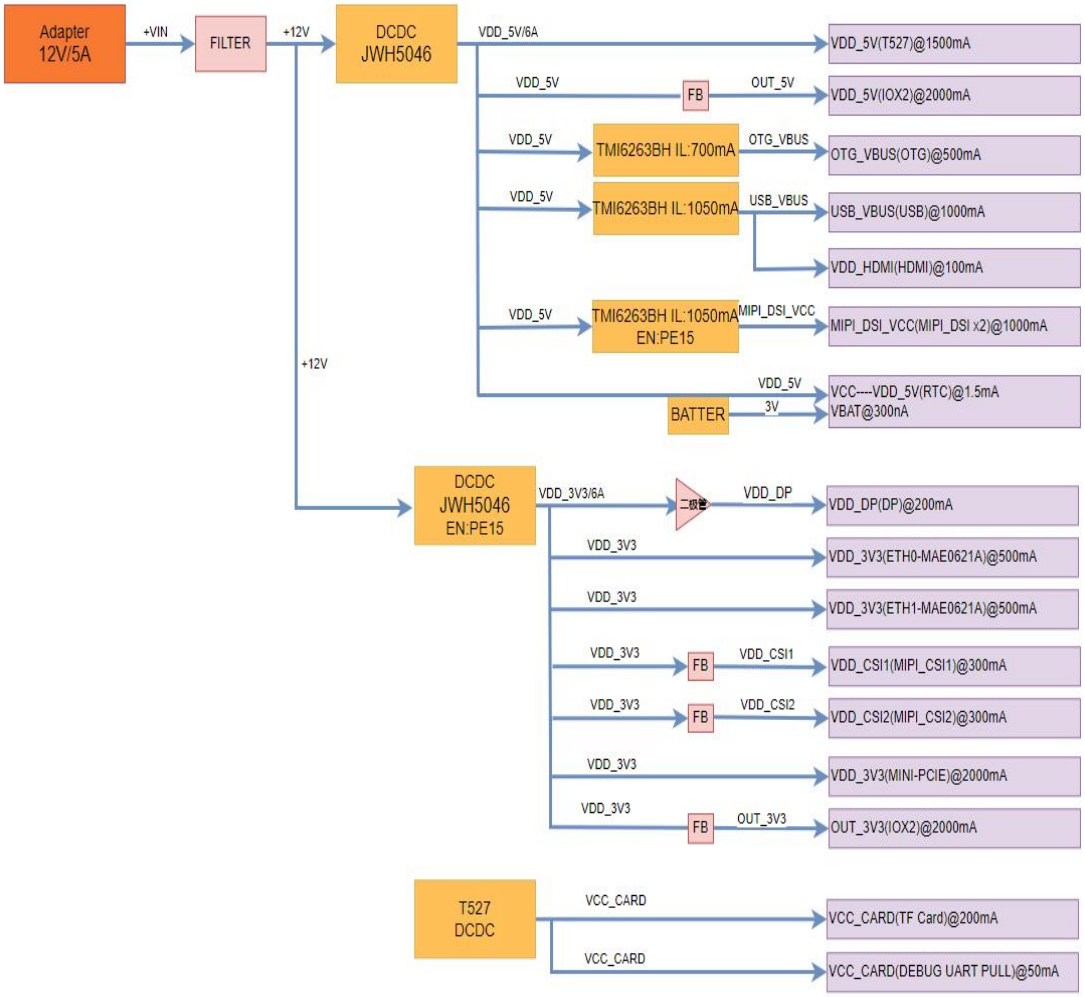
temperature	
Operating humidity	5 ~ 95% humidity, non-condensing;
Storage humidity	60℃@95% humidity, non-condensing;

4. Interface Description

4.1. Power supply

4.1.1. Power tree

The test baseboard power supply tree block diagram is shown below:

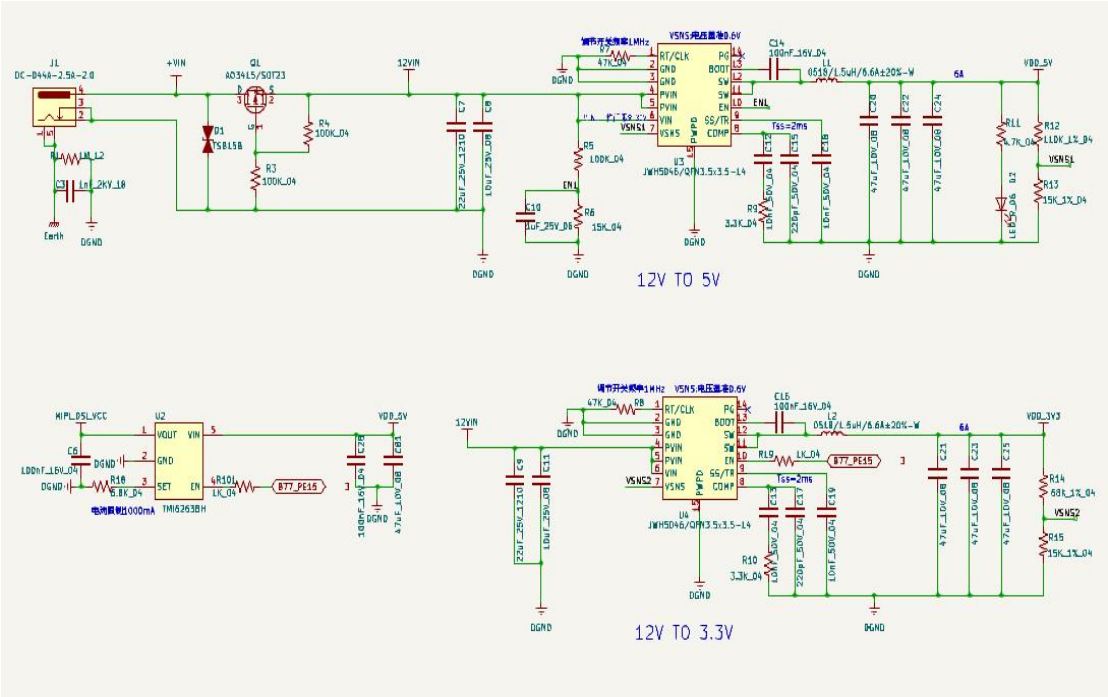


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4.1.2. Power supply design

The power supply adopts 12V DC input and is designed with anti-reverse and TVS anti-surge circuits. Using two DCDC chips were reduced to 5V and 3.3V for each interface and the core board, each power supply is designed to support a maximum current of 6A, detailed power supply to see the bottom of the power tree block diagram.

Due to the TF card and serial debugging circuits need to be more than other interfaces to power up first, so the core board output power supply VCC_CARD power supply. 3.3V power enable signal using the processor's IO port control, pay attention to the selection of the IO port of the evening power, recommended the use of the processor PE, PD, PI, PJ, PK under the IO as a controlled power supply control signals, to prevent the other interfaces of the baseboard too soon! After power-on through the IO port reverse leakage to the core board. 5V power supply USB, OTG, HDMI, MIPI DSI interfaces are connected to the TMI6263BH load switch chip, current limiting at the same time can be enabled through the enable pin to make the back-end power supply controlled.



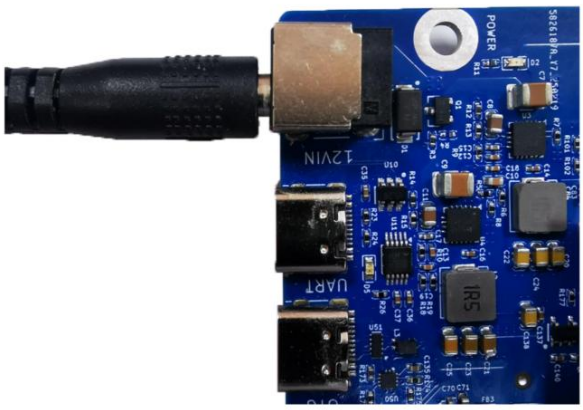
Chassis Power Circuit Reference Diagram

The power input connector is located in the lower left corner of the bottom board, adopting DC2.0 round head connector, as shown in the power connector diagram. Users ca

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n choose the corresponding power of 12V power adapter according to the use of demand for power supply, the detailed power allocation can refer to the power tree diagram of the baseboard, we recommend using 12V 5A power adapter.



Power Interface Diagram

4.1.3. Power supply power consumption

Power Consumption Parameter Table

Working conditions	Supply Voltage(V)	Average current(A)	Power consumption （W）
No-load	12.00	0.19	2.28
Normal	12.00	0.29	3.48
CPU blowfish	12.00	0.53	6.36
CPU cryptohash	12.00	0.51	6.12
CPU zlib	12.00	0.65	7.80
GPU drawing	12.00	0.53	6.36
Stress	12.00	0.78	9.36
Freeze	12.00	0.14	1.68
Mem	12.00	0.07	0.84

4.2. Debugging Interface

The debugging interface converts UART signals to USB signals through the CH340X chip, and the TYPE-C interface is designed to be convenient for users without the need for a serial converter chip. When the TYPE-C debugging interface on the bottom board is connected to the signal, the yellow LED on the top of the interface D5 is always on. The TYPE-C debugging interface is located at the bottom left of the baseboard, as shown in the figure below.

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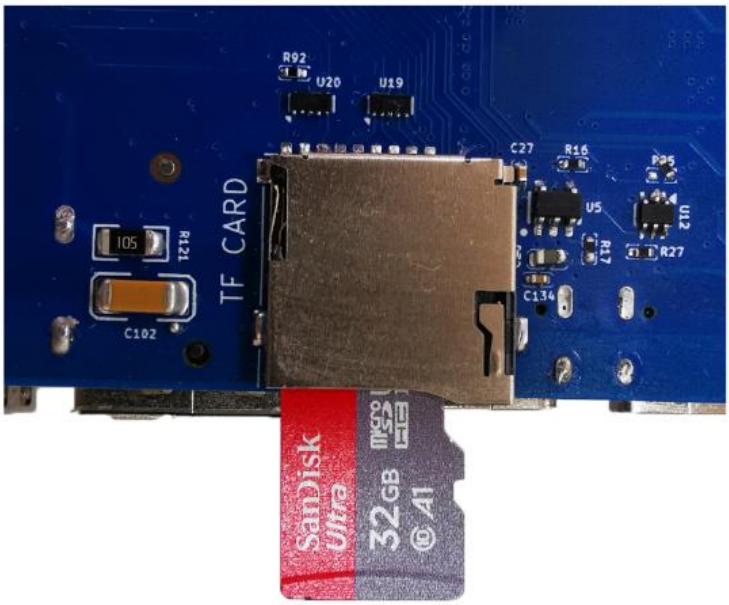
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Debugging Interface Diagram

4.3. TF card interface

The TF card slot is located at the bottom of the back panel. Users can purchase a TF card of 16G or above, download the relevant program from the official website of Chengdu YibaoTek and then burn it into the card. In addition, you can also burn the program directly through OTG. When inserting the SD card, pay attention to the direction as shown in the picture below, and when pulling it out, press the SD card inward gently to eject it.



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4.4. Keys and Indicators

Button Menu

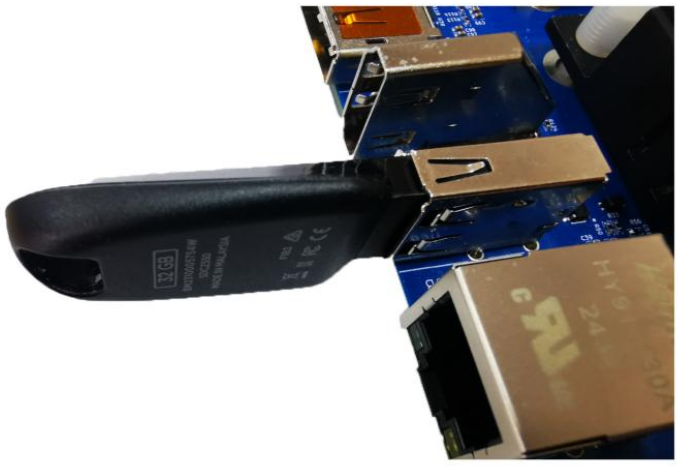
Button Name	Function	Remark
RESET	Hardware reset signal	
PWRON	Power on enable signal	
FEL	Force burn signal	

Indicator light menu

Indicator Name	Function	Default Status	Remarks
PWR	Power indicator	Red, Always On	
RUN	Running Indicator	Green, Blinking	
USER	User Indicator	Green, Blinking	User-definable
D5	Debugging serial port indicator	Yellow, Always On	Corresponds to PL11 IO port
D22	4G network indicator	Green, Off	

4.5. USB 2.0 interface

This product provides one way USB2.0 interface, located in the bottom of the front of the baseboard, as shown in the following USB2.0 interface diagram, users can use the USB interface to connect to the mouse, keyboard, USB flash disk and other devices, but also can be connected to the external USB HUB after connecting multiple devices. Note t hat the USB2.0 interface only supports HOST mode and 1000mA current output.



USB2.0 Interface Diagram

4.6. USB_OTG Interface

Designed to provide a USB_OTG interface, located in the bottom left of the front of

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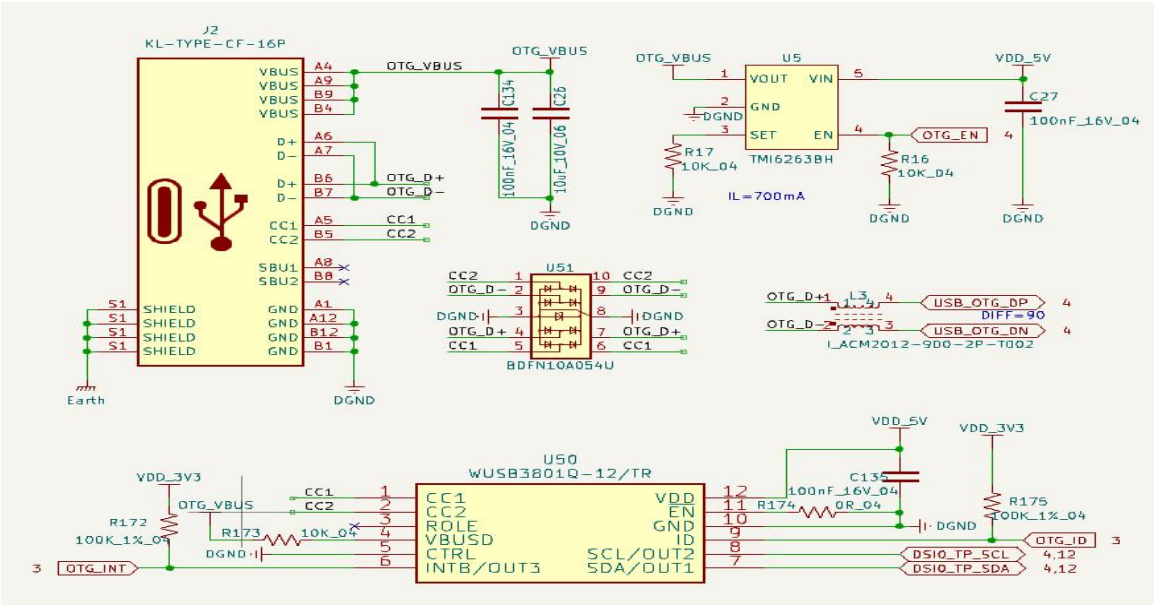
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the board as shown in the following USB_OTG interface diagram, using TYPE-C interfa ce to facilitate the use of the user, support for OTG and HOST mode. Users can burn pr ograms directly through this interface.



USB_OTG Interface Diagram

OTG interface design TPYE-C power configuration detection circuit, using TYPE-C c onfiguration chip WUSB3801Q-12 to detect the CC pin configuration of the external devic e, through the CC pin voltage level comparison to detect the different connections of the topology and settings under the CC connection status, and output detection information to the processor, so as to control the OTG circuit load switch whether to output power. The circuit design refers to the following figure.



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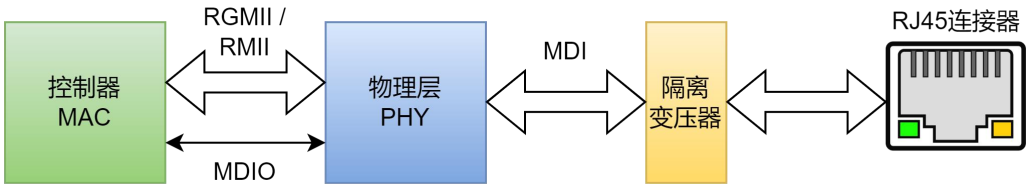
4.7. Network interface

Design the two RJ45 Ethernet interfaces to be located on the lower right side of the front of the backplane, as shown below:



Ethernet interface diagram

Both Ethernet supports 10M/100M/1000M adaptive Ethernet controller.RJ45 Ethernet interface mainly consists of Ethernet controller MAC (Media Access Control), Ethernet physical layer interface PHY (Physical Layer), Ethernet transformer, RJ45 connector components, as shown in the following figure.



MAE0621A is used as the physical layer chip, and the design refers to MAE0621A Design Guide V1.1. 25MHz passive crystal is used to provide the clock. The 25MHz passive crystal is used to provide the clock program, the RJ45 connector with its own transformer, so there is no need to design a separate transformer circuit, it should be noted that the PCB Layout PCB Layout RJ45 connector below the copper to do hollow processing, to avoid interference signals affecting the transformer.

ETH0 PHY design default address is 001 (binary), that is, PHYAD[2:0] corresponding to PHYAD0, PHYAD1, PHYAD2 were configured as 001. RXDLY and TXDLY are configured as 1 (valid), PLLOFF is configured as 0 (invalid).

The default address of the PHY design of ETH1 is 010 (binary), i.e. PHYAD[2:0] corresponding to PHYAD0, PHYAD1, PHYAD2 are configured as 010. both RXDLY and T

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XDLY are configured as 1 (valid) and PLLOFF is configured as 0 (invalid).

PHY chip part of the function needs to be configured by the hardware to do the corr esponding configuration, the specific pins and configuration of the following table:

PHY Pinout Table

PIN NAME	PIN NO.	I/O	DESCRIPTION
PHYAD0	22	O/LI/PU	PHYAD[2:0]. Sampled on reset. The PHY address selects MII management PHY address.
PHYAD1	27	O/LI/PD	
PHYAD2	26	O/LI/PD	
PLLOFF	23	O/LI/PD	ALDPS Mode PLL Off Configuration. Pull up to stop PLL when entering ALDPS mode.
TXDLY	24	O/LI/PD	RGMII Transmit Clock Timing Control. Pull up to add 2ns delay to TXC for TXD latching.
RXDLY	25	O/LI/PU	RGMII Receive Clock Timing Control. Pull up to add 2ns delay to RXC for RXD latching.
CFG_EXT	32	O/LI/PD	RGMII and SMI I/O Pad Power Source Mode Configuration. When pulling down CFG_EXT, CFG_LDO[1:0] represent LDO output voltage setting for IO pad: 2'b00: Reserved; 2'b01: 2.5V from internal LDO; 2'b10: 1.8V from internal LDO; 2'b11: 1.5V from internal LDO. When pulling up CFG_EXT, CFG_LDO[1:0] represent the input voltage of IO pad is selected from external power: 2'b00: 3.3V from external power; 2'b01: 2.5V from external power; 2'b10: 1.8V from external power; 2'b11: 1.5V from external power.
CFG_LDO0	33	O/LI/PU	
CFG_LDO1	34	O/LI/PD	

LED Status Indicator

Connection Status	LED status	Transmission Status	LED status
10M connection	Two lights are not on	10M Transmission	Two lights are not lit
100M connection	Yellow LED on	100M Transmission	Yellow LED blinking
1000M connection	Green LED on	1000M Transmission	Green LED blinking

4.8. Audio Interface

The audio interface is a 3.5mm, CTIA four-segment headphone jack that supports mic rophone in and headphone out, as shown below.

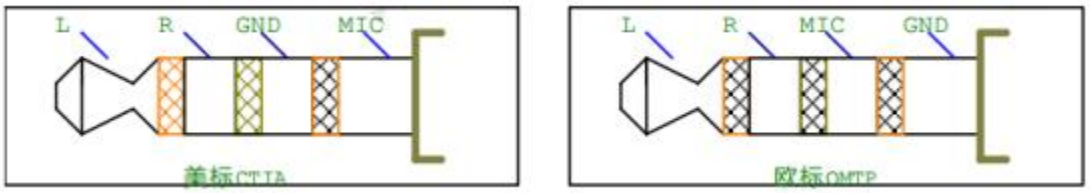
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Audio Interface Diagram

Note that different standards of headset interface structure and wiring order is differen t, need to be based on the actual use of the interface wiring, specific reference to the cor responding headset interface manual, this product adopts the American Standard CTIA four -segment headset, the American Standard and the European standard interface differences a re shown in the figure below.



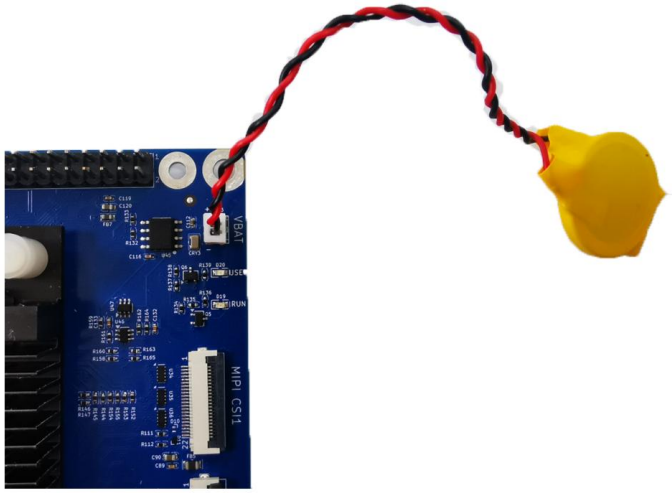
Comparison chart of the structural definition of a four-segment headset

4.9. RTC

The baseboard uses a separate RTC chip to provide clock data, the chip has an auto matic power-down detection and power switching circuit, the main power supply using +5 V power supply, the backup power supply using +3V battery power supply, the battery vo ltage must be maintained at 2.0V to 3.5V in order to work properly, the battery power su pply mode, the oscillator operates with a consumption of less than 500nA, the battery is r ecommended to use the CR2032 battery. The interface uses a 1x2Pin 1.25mm pitch conne ctor located on the upper right side of the front of the backplane, as shown below.

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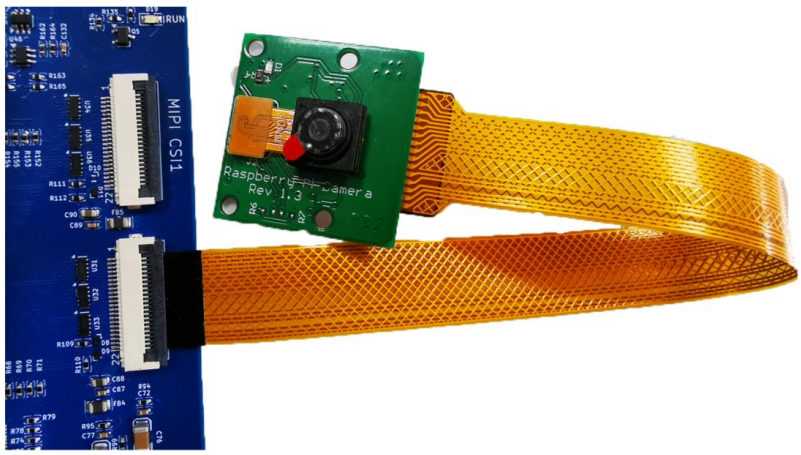
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RTC Battery Interface Diagram

4.10. MIPI CSI Interface

MIPI CSI camera interface is located on the right side of the front of the bottom bo ard, there are two interfaces, MIPI CSI0 and MIPI CSI1, both using 22Pin0.5mm FPC sof t cable connection, as shown in the figure below, the interface is compatible with Raspber ry Pi 5's CSI interface, you can buy the Raspberry Pi 5's camera through the e-commerce platform can be used. You can also buy Raspberry Pi 4B and 3B + corresponding camer a through the adapter cable will be 15Pin to 22Pin can be used.



MIPI CSI Camera Interface Diagram

The parallel CSI interfaces support a maximum pixel clock of 148.5 MHz and are B T.1120 compliant. Each interface utilizes 4 lanes, each with a maximum rate of 2.0 Gbps, and is compliant with MIPI-CSI2 V1.1 and MIPI DPHY V1.1 specifications. The MIPI CSI interface of this product supports a maximum video capture resolution of 4 megapixel

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s @ 30 frames/second.

When connecting, pay attention to the pin numbering to avoid inserting the pins in reverse, refer to the pin number identification next to the connector, which should correspond to the pins on the camera side, the detailed pin definitions are listed in the table below.

MIPI CSI0 Interface Definition Form

Pin No.	Pin Definition	Function Description	Pin Levels
1	GND	GND	0V
2	MIPI_CSIA_D0N	CSI Differential Signaling	1V8
3	MIPI_CSIA_D0P	CSI Differential Signal	1V8
4	GND	GND	0V
5	MIPI_CSIA_D1N	CSI Differential Signal	1V8
6	MIPI_CSIA_D1P	CSI Differential Signal	1V8
7	GND	GND	0V
8	MIPI_CSIA_CKN	CSI Differential Clock Signals	1V8
9	MIPI_CSIA_CKP	CSI Differential Clock Signal	1V8
10	GND	GND	0V
11	MIPI_CSIB_D0N	CSI Differential Signal	1V8
12	MIPI_CSIB_D0P	CSI Differential Signal	1V8
13	GND	GND	0V
14	MIPI_CSIB_D1N	CSI Differential Signal	1V8
15	MIPI_CSIB_D1P	CSI Differential Signal	1V8
16	GND	GND	0V
17	MIPI_CSI0_PWR_EN	Power Enable Signal	3V3
18	NC	/GND	/
19	GND	GND	0V
20	CSI0_I2C3_SCL	I2C Clock Signal	3V3
21	CSI0_I2C3_SDA	I2C data signal	3V3
22	VDD_CSI0	3.3V power supply	3V3

MIPI CSI1 Interface Definition Form

Pin No.	Pin Definition	Function Description	Pin Levels
1	GND	GND	0V
2	MIPI_CSIC_D0N	CSI Differential Signaling	1V8
3	MIPI_CSIC_D0P	CSI Differential Signal	1V8
4	GND	GND	0V
5	MIPI_CSIC_D1N	CSI Differential Signal	1V8
6	MIPI_CSIC_D1P	CSI Differential Signal	1V8
7	GND	GND	0V

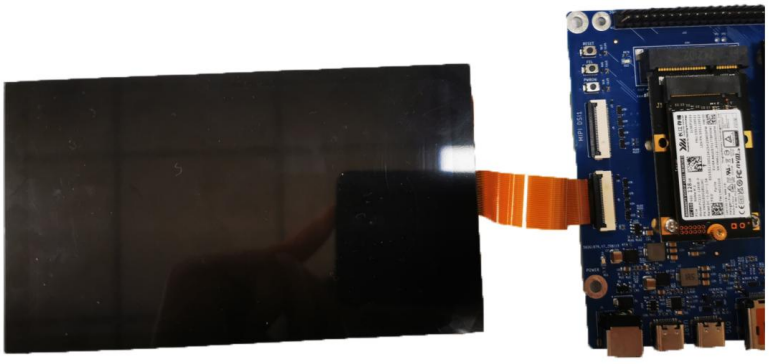
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8	MIPI_CSIC_CKN	CSI Differential Clock Signal	1V8
9	MIPI_CSIC_CKP	CSI Differential Clock Signal	1V8
10	GND	GND	0V
11	MIPI_CSID_D0N	CSI Differential Signal	1V8
12	MIPI_CSID_D0P	CSI Differential Signal	1V8
13	GND	GND	0V
14	MIPI_CSID_D1N	CSI Differential Signaling	1V8
15	MIPI_CSID_D1P	CSI Differential Signal	1V8
16	GND	GND	0V
17	MIPI_CSI1_PWR_EN	Power Enable Signal	3V3
18	NC	/GND	/
19	GND	GND	0V
20	CSI1_I2C4_SCL	I2C Clock Signal	3V3
21	CSI1_I2C4_SDA	I2C data signal	3V3
22	VDD_CSI1	3.3V power supply	3V3

4.11. MIPI DSI interface

Design two MIPI DSI display interfaces, MIPI DSI0 and MIPI DSI1, located on the left side of the front of the backplane, as shown below. Each DSI display interface adopts 4-lane MIPI DSI and supports up to 2.5K@60fps and 4K@45fps.



The DSI display interface uses a 26Pin 0.5mm pitch FPC connector, and can be connected to the display using a 26Pin 0.5mm FPC flexible cable. When connecting, pay attention to the serial number of the pins to prevent inserting the opposite, refer to the serial number of the pins next to the connector, which should correspond to the pins on the side of the display, and the detailed pin definitions are shown in the table below. We recommend using EVERBUILT ECA11-5LM1xxxC series for MIPI.

MIPI DSI0 Interface Definition Form

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Pin No.	Pin Definition	Function Description	Pin Levels
1	GND	GND	0V
2	DSI0_LCD_RESET	LCD screen reset signal	1V8
3	GND	GND	0V
4	MIPI_DSI0_D3N	DSI Differential Signal	1V8
5	MIPI_DSI0_D3P	DSI Differential Signal	1V8
6	GND	GND	0V
7	MIPI_DSI0_D2N	DSI Differential Signal	1V8
8	MIPI_DSI0_D2P	DSI Differential Signal	1V8
9	GND	GND	0V
10	MIPI_DSI0_D0N	DSI Differential Signaling	1V8
11	MIPI_DSI0_D0P	DSI Differential Signal	1V8
12	GND	GND	0V
13	MIPI_DSI0_CLKN	DSI Differential Clock Signal	1V8
14	MIPI_DSI0_CLKP	DSI Differential Clock Signal	1V8
15	GND	GND	0V
16	MIPI_DSI0_D1N	DSI Differential Signal	1V8
17	MIPI_DSI0_D1P	DSI Differential Signal	1V8
18	GND	GND	0V
19	DSI0_LCD_ID	LCD Detection Pins	/
20	DSI0_BL_CTR	Backlight Control Signal	3V3
21	DSI0_TP_RST	Touch panel reset signal	3V3
22	DSI0_TP_SDA	I2C data signal	3V3
23	DSI0_TP_SCL	I2C Clock Signal	3V3
24	DSI0_TP_INT	Touch panel interrupt signal	3V3
25	MIPI_DSI_VCC	5V Power Supply	5V
26	MIPI_DSI_VCC	5V Power Supply	5V

MIPI DSI1 Interface Definition Form

Pin No.	Pin Definition	Function Description	Pin Levels
1	GND	GND	0V
2	DSI1_LCD_RESET	LCD screen reset signal	1V8
3	GND	GND	0V
4	MIPI_DSI1_D3N	DSI Differential Signal	1V8
5	MIPI_DSI1_D3P	DSI Differential Signal	1V8
6	GND	GND	0V
7	MIPI_DSI1_D2N	DSI Differential Signal	1V8
8	MIPI_DSI1_D2P	DSI Differential Signal	1V8
9	GND	GND	0V
10	MIPI_DSI1_D0N	DSI Differential Signal	1V8
11	MIPI_DSI1_D0P	DSI Differential Signal	1V8
12	GND	GND	0V

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13	MIPI_DSI1_CLKN	DSI Differential Clock Signal	1V8
14	MIPI_DSI1_CLKP	DSI Differential Clock Signal	1V8
15	GND	GND	0V
16	MIPI_DSI1_D1N	DSI Differential Signal	1V8
17	MIPI_DSI1_D1P	DSI Differential Signal	1V8
18	GND	GND	0V
19	DSI1_LCD_ID	LCD Detect Pin	/
20	DSI1_BL_CTR	Backlight Control Signal	3V3
21	DSI1_TP_RST	Touch panel reset signal	3V3
22	DSI1_TP_SDA	I2C data signal	3V3
23	DSI1_TP_SCL	I2C Clock Signal	3V3
24	DSI1_TP_INT	Touch panel interrupt signal	3V3
25	MIPI_DSI_VCC	5V Power Supply	5V
26	MIPI_DSI_VCC	5V Power Supply	5V

4.12. DP interface

Designed for 1 channel DisplayPort display interface with standard DP connector, loca ted on the bottom front of the chassis, as shown in the picture below. The interface supp orts 2.5K@60fps and 4K@30fps resolution. 1, 2, and 4 lanes transmission with a maximu m transmission rate of 2.7 Gbit/s. Color depth: 8bit and 10bit per lane.



DP Monitor Interface Diagram

4.13. HDMI interface

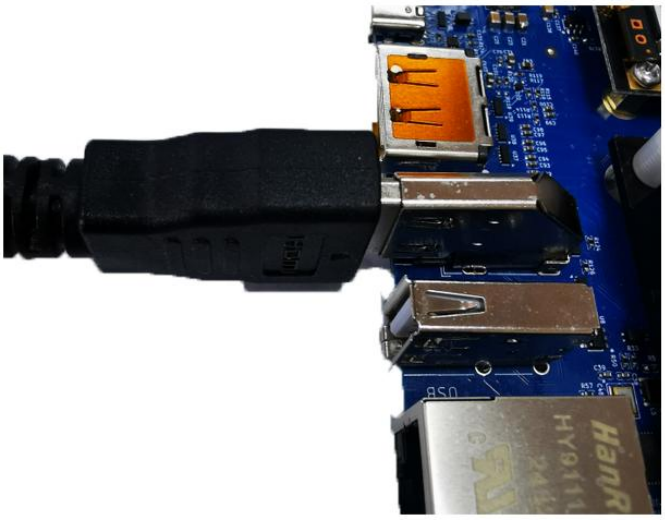
Design 1 channel HDMI display interface, located at the bottom of the front side of the baseboard, as shown in the picture below. Support HDMI 2.0 and HDCP1.4 protocol.

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Maximum support 4K@60fps 2D display or 4K@30fps 3D display.

ECK32-T527B series core board HDMI I2C and CEC pins built-in Levelshift circuit, for 5V voltage pin, support for direct connection to the device side does not require external level conversion chip. Single-board machine HDMI interface 5V power supply pin has been connected Schottky diode series, to avoid power leakage after the device side of the shutdown.



HDMI Display Interface Diagram

4.14. MINI PCIE interface

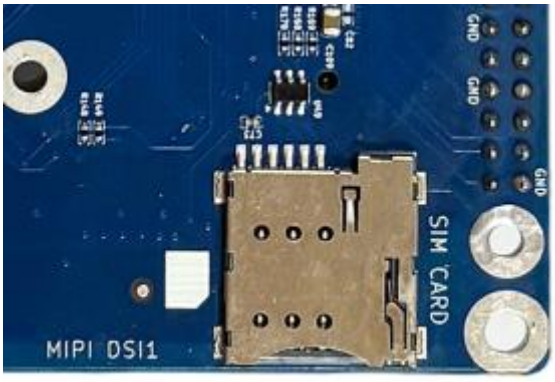
Design 1 channel MINI PCIE interface, located in the left side of the front of the bottom board, as shown in the following figure. The interface accesses PCIE and USB signals and supports PCIe2.1 and USB2.0. Users can connect external Wi-Fi, Bluetooth and 4G communication modules etc. through the MINI PCIE interface. Designed with full-size and half-size mounting holes to support full-size and half-size NIC installation.

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MINI PCIE interface diagram



SIM Card Interface Diagrams

The MINI PCIE interface is defined in the table below:

MINI PCIE Interface Definition Form

Pin No.	Pin Definition	Functional Description
1	NC	/
2	VDD_3V3	3.3V power supply
3	NC	/
4	GND	GND
5	NC	/
6	NC	/
7	NC	/
8	SIM_VDD	SIM card power supply
9	GND	GND
10	SIM_DATA	SIM card data signal
11	PCIE_CLKN	PCIE_CLKN differential signal

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12	SIM_CLK	SIM card clock signal
13	PCIE_CLKP	PCIE_CLKN differential signal
14	SIM_RST	SIM card reset signal
15	GND	GND
16	NC	/
17	NC	/
18	GND	GND
19	NC	/
20	NC	/
21	GND	GND
22	PCIE0_PERSTN	PCIE reset signal
23	PCIE_RX0_DN	PCIE_RX0_DN differential signal
24	VDD_3V3	3.3V power supply
25	PCIE_RX0_DP	PCIE_RX0_DP differential signal
26	GND	GND
27	GND	GND
28	NC	/
29	GND	GND
30	NC	/
31	PCIE_TX0_DN	PCIE_TX0_DN differential signaling
32	NC	/PCIE_TX0_DP Differential Signal
33	PCIE_TX0_DP	PCIE_TX0_DP Differential Signal
34	GND	GND
35	GND	GND
36	PCIE_USB_DN	USB_DN differential signal
37	GND	GND
38	PCIE_USB_DP	USB_DP differential signal
39	VDD_3V3	3.3V power supply
40	GND	GND
41	VDD_3V3	3.3V Power Supply
42	VDD_3V3	3.3V power supply
43	GND	GND
44	NC	/
45	NC	/
46	NC	/
47	NC	/
48	NC	/
49	NC	/
50	GND	GND
51	NC	/
52	VDD_3V3	3.3V power supply

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4.15. Raspberry Pi Extended Interface

Design two Raspberry Pi 2x20Pin 2.54mm standard expansion connectors located on t he top front of the backplane as shown below.



Raspberry Pi Extended Interface Diagram

IO interfaces provide multiplexing functions including 2 sets of SPI interfaces, 2 sets of I2S interfaces, 1 set of SDC interfaces, 2 sets of CAN interfaces, 4 sets of I2C interfa ces, 3 sets of UART interfaces, which can be configured and utilized by users according t o their needs. In addition, the 3.3V and 5V power supply provided by each expansion int erface supports 1000mA current output, providing detailed definitions in the following tabl e.

J14 Raspberry Pi Expansion Interface Pin Definition Table

Pin No.	Pin Definition	Pin No.	Pin Definition
1	3V3	2	5V
3	PM5/S_I2C2_SDA	4	5V
5	PM4/S_I2C2_SCL	6	GND
7	PG10/I2S1_MCLK	8	PG6/UART1_TX
9	GND	10	PG7/UART1_RX
11	PG0/SDC1_CLK	12	PG11/I2S1_BCLK
13	PG1/SDC1_CMD	14	GND
15	PG2/SDC1_D0	16	PG3/SDC1_D1
17	3V3	18	PG4/SDC1_D2
19	PE13/SPI2_MOSI	20	GND
21	PE14/SPI2_MISO	22	PG5/SDC1_D3
23	PE12/SPI2_CLK	24	PE11/SPI2_CS0
25	GND	26	B6_PL12
27	PM3/S_I2C1_SDA	28	PM2/S_I2C1_SCL
29	PL5/S_CAN_RX0	30	GND
31	PL4/S_CAN_TX0	32	PM0/S-PWM2
33	PM1/S-PWM3	34	GND
35	PG12/I2S1_LRCK	36	PG8/UART1_RTS
37	PG9/UART1_CTS	38	PG14/I2S1_DIN0
39	GND	40	PG13/I2S1_DOUT0

J15 Raspberry Pi Expansion Interface Pin Definition Table

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Pin No.	Pin Definition	Pin No.	Pin Definition
1	3V3	2	5V
3	CSI1_I2C4_SDA	4	5V
5	CSI1_I2C4_SCL	6	GND
7	PE5/I2S2_MCLK	8	PI6/UART6_TX
9	GND	10	PI7/UART6_RX
11	B31_PI8	12	PE6/I2S2_BCLK
13	PD20/UART2_TX	14	GND
15	PD21/UART2_RX	16	PB3/CAN_RX0
17	3V3	18	PB2/CAN_TX0
19	PI4/SPI1_MOSI	20	GND
21	PI5/SPI1_MISO	22	B32_PI12
23	PI3/SPI1_CLK	24	PI2/SPI1_CS0
25	GND	26	B12_PI0
27	PJ27/I2C5_SDA	28	PJ26/I2C5_SCL
29	B13_PI1	30	GND
31	B14_PI11	32	PB11/PWM_2
33	PB12/PWM_3	34	GND
35	PE7/I2S2_LRCK	36	B52_PI14
37	B34_PI9	38	PE9/I2S2_DIN0
39	GND	40	PE8/I2S2_DOUT0

4.16. TP test points

Some of the GPIO interfaces on the bottom board are not used, and they are not led out to the expansion interface, but are led out as TP points, if the user has the demand, he can use the related TP point function according to the definition in the following tabl e.

TP point definition table

TP point number	TP point definition	TP point number	TP point definition
TP1	C87_PH19	TP2	C88_PH12
TP3	B1_PE1	TP4	B2_PE2
TP5	B3_PE4	TP6	B23_PE3
TP7	B58_PJ23	TP8	B43_PJ21
TP9	B26_PJ22	TP10	B5_PJ20
TP11	B27_PL2	TP12	B44_PL13
TP13	B73_PJ17	TP14	B59_PL3
TP15	B62_PJ19	TP16	B61_PJ18
TP17	B65_PL9	TP18	B64_PL8
TP19	A64_PL7	TP20	A80_PL6

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TP21	B9_PJ16	TP22	A79_PE10
TP23	CK24M_OUT	TP24	GPADC9
TP25	CK32K_OUT	TP26	GPADC7
TP27	WREQIN	TP28	PC4_1V8
TP29	C4_PB1	TP30	C9_PB8
TP31	PC2_1V8	TP32	PC12_1V8

5. Software resource

ECB32-T527B single board equipped with an operating system based on the Linux 5. 15 version of the kernel, the single board shipped with embedded Linux system developm ent needs of the cross-compiler tool chain Buildroot source code, U-boot source code, Lin ux kernel and the source code of the driver module, as well as for the desktop environme nt and Linux Windows desktop environment and a variety of development and debugging tools. Desktop environment for Windows and Linux, as well as a variety of development and debugging tools.

The operating system:

1.Linux file system built by Buildroot

2.Debian port of the Linux file system

System source code:

1.U-boot 2018

2.Kernel 5.15

3.BuildRoot 2022.05

4.Debian 11

Development environment and tools:

1.USB burning tool: PhoenixSuit

2.SD card burning tool: PhoenixCard

System software resources see the following table:

System Software Resource Sheet

Categorie	Name	Description	Source code
SPL	spl-pub	Boot0, boot uboot	<SDK>/brandy/brandy-2.0/spl-pub/
BOOT	u-boot 2018.07	Boot Programs	<SDK>/brandy/brandy-2.0/u-boot-2018/

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Kernel	Kernel 5.15.147	Linux kernel	<SDK>/kernel/linux-5.15/
Bsp	BSP	Driver and device tree in the kernel for logging-related parts, etc.	<SDK>/bsp/
Device Driver	Audio	Built-in audio driver	bsp/drivers/sound/platform/*
	AWlink	CAN driver	bsp/awlink
	GMAC	Built-in MAC driver	bsp/gmac
	STMMAC	Built-in MAC driver	Bsp/stmmac
	GPADC	GPADC driver	bsp/gpadc
	GPIO	GPIO Driver	bsp/pinctrl/*
	drm	Display Screen Driver	bsp/drm/panel/*
	LRADC	Key Module Driver	bsp/lradc/*
	MMC	MMC Driver	bsp/mmc/*
	SPI	SPI Driver	bsp/spi/*
	TWI	I2C Driver	bsp/twi/*
	UART	Serial Driver	bsp/uart/*
	VIN	Specific Camera Driver	bsp/vin/modules/sensor/*
	Pcie	PCI Driver	bsp/pci/*
	IR	Infrared Driver	bsp/ir-rx/* bsp/ir-tx/*
Operating Systems	Buildroot 202205	Version 202205 Buildroot	<SDK>/buildroot/buildroot-202205
	Debian	Debian 11	<SDK>/debian/compressed_files/
Development Tools	PhoenixSuit	USB burning tool	/tools/PhoenixSuit
	PhoenixCard	SD Card Burning Tool	/tools/PhoenixCard

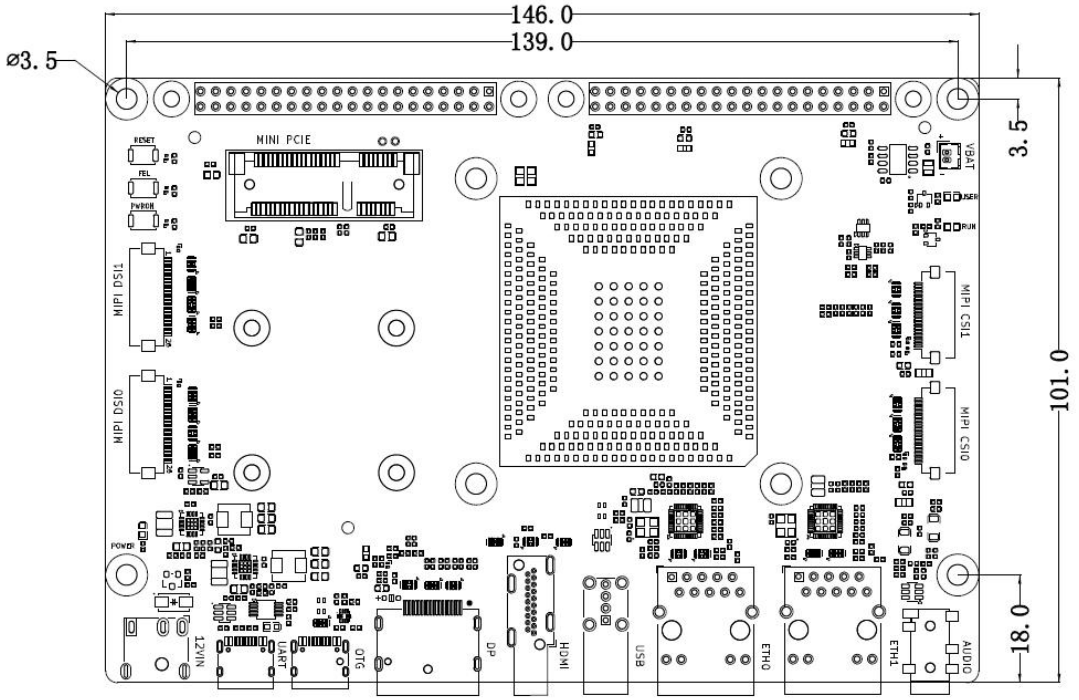
6. Structural Dimension

Unit mm; error ±0.1mm.

The front dimensions are shown in the figure below:

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Dimensional drawing of the front structure of the base plate

7. Revision history

Revised Explanatory Notes

Version	Revision content	Date	Preparation	Proofreading	Approval
V1.0	first draft	25-3-28	WJ	LJQ	WFX

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