Product manual
ECB30-PGT13IC-I Motherboard



Chengdu Ebyte Electronic Technology Co.,Ltd.

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1. Product Overview

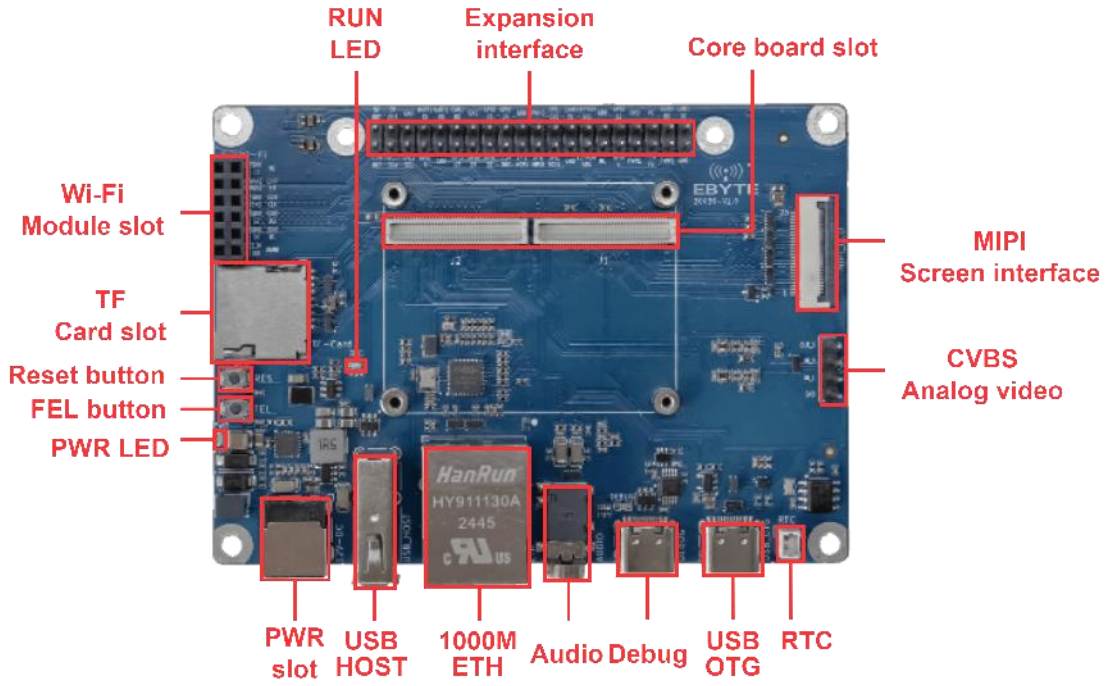
1.1.Product Introduction

Ebyte launched the motherboard ECB30-PGT13IC-I based on the ECK30-T13IC series core board. The core board and motherboard are combined through BTB connectors. The motherboard has rich peripheral interfaces. The design grade is higher than that of ordinary development boards and can be used in batches in industrial scenarios.

Ebyte provides a stable reference design and a perfect software development environment, which can effectively help users verify core board functions, improve development efficiency, shorten development cycle, optimize design quality, and speed up product development and time to market.

Please refer to ECB30-PGT13IC _ User _ Guide _ CN _ V1.0. pdf for a quick start-up manual

The functional diagram of the motherboard is as follows:



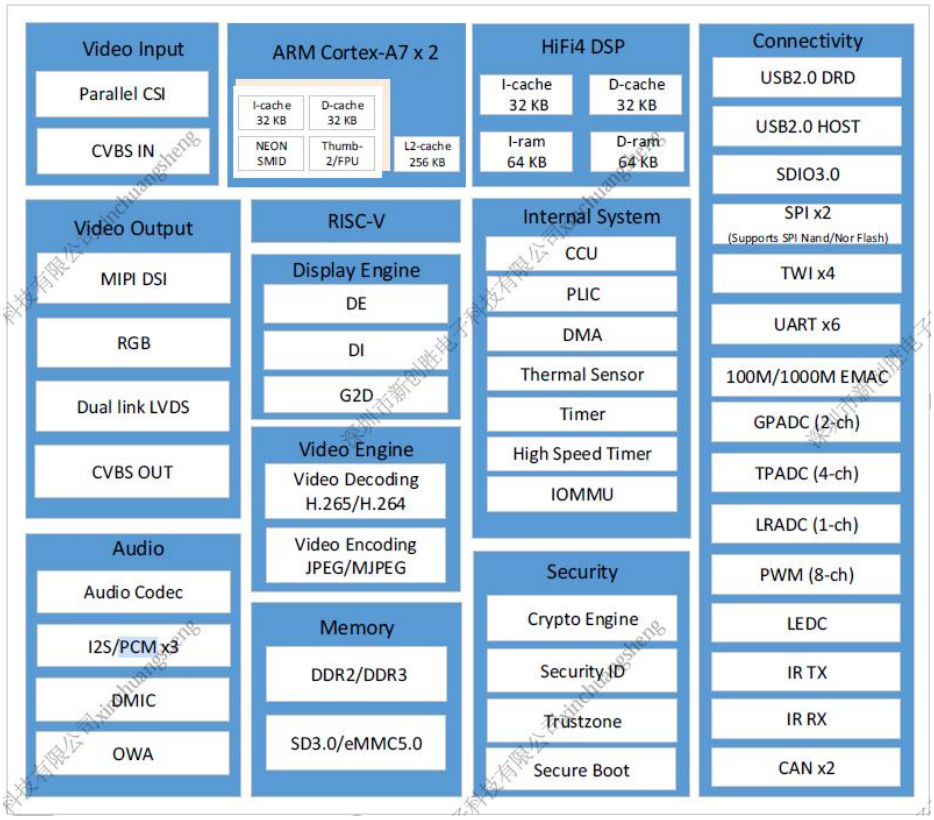
Motherboard function description diagram

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1.2. Introduction to T113-I chip

Allwinner Technology T113-i processor is a multi-core heterogeneous industrial-grade processor based on dual-core ARM Cortex-A7 + RISC-V + HiFi4 DSP. Supports H.265, H.264, MPEG-1/2/4, JPEG, VC1 and other full format 1080P @ 60FPS video decoding, JPEG/MJPEG 1080P @ 60FPS video encoding, has rich multimedia interface MIPI-DSI/RGB/LVDS/CVBS/Parallel CSI, and supports 1080P @ 60FPS display. Integrated ADC/DAC and I2S/PCM/DMIC/OWA audio interfaces can work seamlessly with the CPU to accelerate multimedia algorithm applications and improve user experience. The processor also supports Gigabit Ethernet interface, 2 CAN interfaces, 2 USB2.0 interfaces, 6 UART and other functional interfaces. Furthermore, the T113-i can be connected with other different peripherals such as WiFi and Bluetooth via SDIO and UART. The functional block diagram of the T113-i processor is shown in the following figure:



T113-iProcessor system functional block diagram

1.3.Introduction to ECK30-T13IC series core board

ECK30-T13IC series core board adopts 8-layer board design, sunken gold and lead-fre

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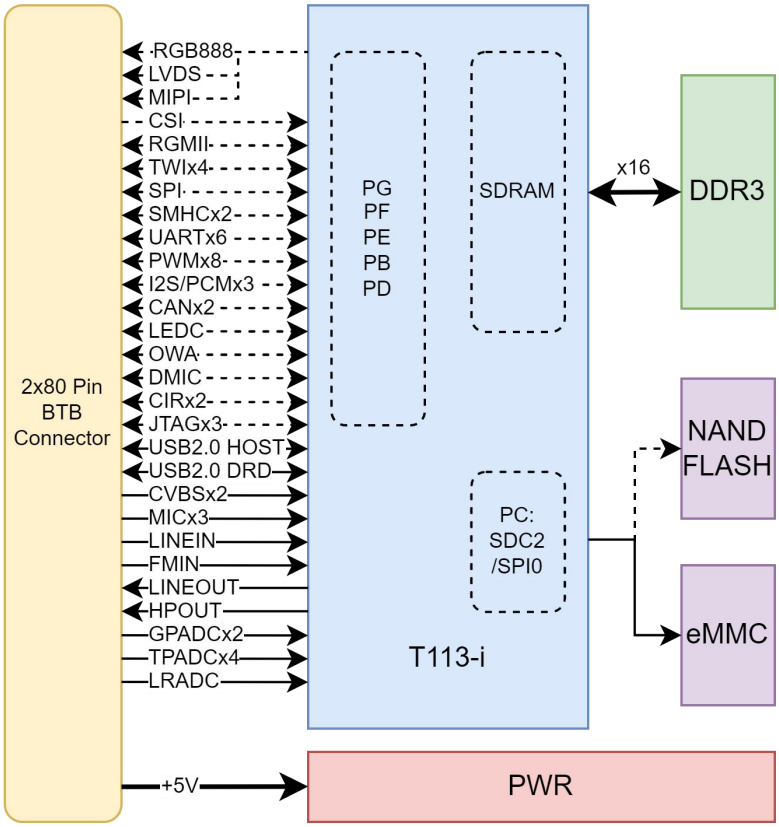
e process. The core board integrates Allwinner T113-i CPU, ROM, RAM, power supply, c rystal oscillator and other devices. Among them, the RAM can be selected in 256MB, 512 MB, and 1GB capacity; ROM optional 256MB, 8GB capacity. All devices are domestic in dustrial grade, stable and reliable. The core plate size is: 45 × 35 × 3. 6 mm, and the si gnal and power source are extracted through the stamp hole for up to 160Pin. Ideal for h igh-volume applications in industrial control, HMI, IoT and more。

ECK30-T13IC5E8-IThe physical diagram of the core board is as follows:



Physical drawing of core board

The functional block diagram of ECK30-T13IC series core board is as follows:



Functional block diagram

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1.4.Typical Applications

- Industrial Control Motherboard;
- Automotive Electronics;
- Industrial all-in-one machine;
- Smart cities;
- Tablets;
- IoT Gateway;
- Advertising All-in-One;
- Robots.

2. Specifications

2.1.Functional parameters

ECB30-PGT13IC-I motherboard function parameter table

Power input	1 DC socket, 12V _ 1A input;
show	1 channel 4-LANE MIPI display interface, maximum support 1920 * 1080 @ 60Hz;
USB HOST	1 USB2.0 TYPE _ A interface;
USB OTG	1 USB2.0 TYPE _ C OTG interface;
Network port	1-way 10/100/1000 adaptive Ethernet RJ45 interface with indicator light;
TF	1 TF card slot for booting the system or expanding storage;
Audio	1 headphone output and microphone input, 3.5 mm interface;
BOOT	Automatically select the startup mode;
Commissioning	1-channel UART debugging and printing serial port (UART0), Type-C lead out;
UART	4 channels, extended pin row lead out, reused with other functions;
CAN	2 channels, extended pin row lead out, reused with other functions;
SPI	1 channel, extended pin row to lead out, reuse with other functions;
GPIO	26 channels, extended pin row lead out, reused with other functions;
I2C	4 channels, extended pin row lead out, reused with other functions;
key	1 reset button; 1 download button;
Indicator lamp	1 x power lamp; 1 running light; 1 debugging light;
Watchdog	Support on-chip watchdog function;
RTC	1 RTC clock chip, 1 2P 1.27 mm plug-in battery holder;
Power output	Two 3.3 V @ 1A power outputs, extended pin lead out; 2 5V @ 1A power supply outputs, extended pins lead out;

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2.2.Environmental Characteristics

ECB30-PGT13IC-I Motherboard Environmental characteristic table

Operating temperature	-40℃ ~ 85℃;
Storage temperature	-40℃ ~ 85℃;
Operating humidity	5 ~ 95% humidity, non-condensation;
Storage humidity	60 ℃ @ 95% humidity, non-condensing;

3. Interface definition

3.1.Core Board Pin Definition

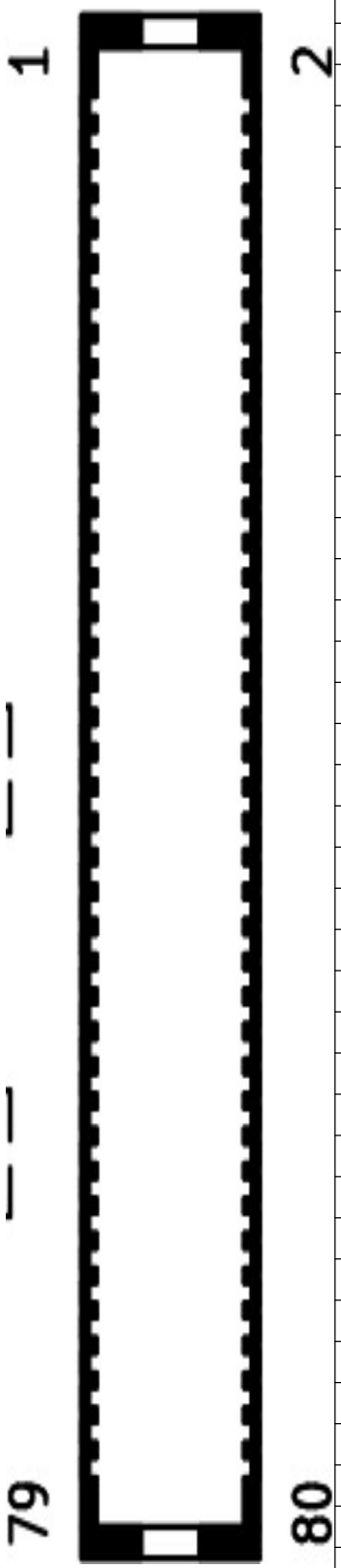
The ECK30-T13IC series core board leads out signals and power supplies a total of 160PIN through the BTB connector. These signal pins contain rich peripheral resources. From connector J1 and connector J2, respectively. Please refer to ECK30-T13IC _ Pin _ List _ V1.0. xlsx for detailed definitions. The backplane BTB interface I/O allocation pins are defined as follows:

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BTB J1 interface pin definition table

Pin Name	Pin		Pin	Pin Name
DGND	J1-1		J1-2	DGND
PB0 _ J16	J1-3		J1-4	PD0 _ W19
PB1 _ J17	J1-5		J1-6	PD1 _ V20
PB2 _ M16	J1-7		J1-8	PD2 _ V19
PB3 _ M15	J1-9		J1-10	PD3 _ U20
PB4 _ K16	J1-11		J1-12	PD4 _ U19
PB5 _ K15	J1-13		J1-14	PD5 _ U18
PB6 _ K17	J1-15		J1-16	DGND
DGND	J1-17		J1-18	PD6 _ T19
PB7 _ J15	J1-19		J1-20	PD7 _ T18
PB8 _ G15	J1-21		J1-22	PD8 _ R20
PB9 _ G16	J1-23		J1-24	PD9 _ R19
PB10 _ F17	J1-25		J1-26	PD10 _ T17
PB11 _ F15	J1-27		J1-28	PD11 _ R17
PB12 _ F16	J1-29		J1-30	DGND
DGND	J1-31		J1-32	PD12 _ P19
FMINR _ C17	J1-33		J1-34	PD13 _ P18
FMINL _ B17	J1-35		J1-36	PD14 _ N17
LINEINR _ C16	J1-37		J1-38	PD15 _ N16
LINEINL _ B16	J1-39		J1-40	PD16 _ N20
AUD _ AGND	J1-41		J1-42	PD17 _ N19
MBIAS _ E16	J1-43		J1-44	DGND
MIC _ DET _ A17	J1-45		J1-46	PD18 _ M19
MICIN1P _ D20	J1-47		J1-48	PD19 _ M18
MICIN1N _ D19	J1-49		J1-50	PD20 _ W18
MICIN3P _ D17	J1-51		J1-52	PD21 _ V18
MICIN3N _ D16	J1-53		J1-54	DGND
MICIN2P _ E15	J1-55		J1-56	DGND
MICIN2N _ D15	J1-57		J1-58	LRADC _ B12
AUD _ AGND	J1-59		J1-60	GPADC0 _ C13
LINEOUTLP _ B15	J1-61		J1-62	GPADC1 _ B13
LINEOUTLN _ C15	J1-63		J1-64	DGND
LINEOUTRP _ B14	J1-65		J1-66	TP _ X1 _ C12
LINEOUTRN _ C14	J1-67		J1-68	TP _ X2 _ A11
AUD _ AGND	J1-69		J1-70	TP _ Y1 _ B11
HP _ DET _ A13	J1-71		J1-72	TP _ Y2 _ C11
HBIAS _ E17	J1-73		J1-74	DGND
HPOUTR _ D13	J1-75		J1-76	TVIN0 _ B9
HPOUTFB _ E13	J1-77		J1-78	TVIN1 _ C9
HPOUTL _ F13	J1-79		J1-80	TVOUT0 _ E19

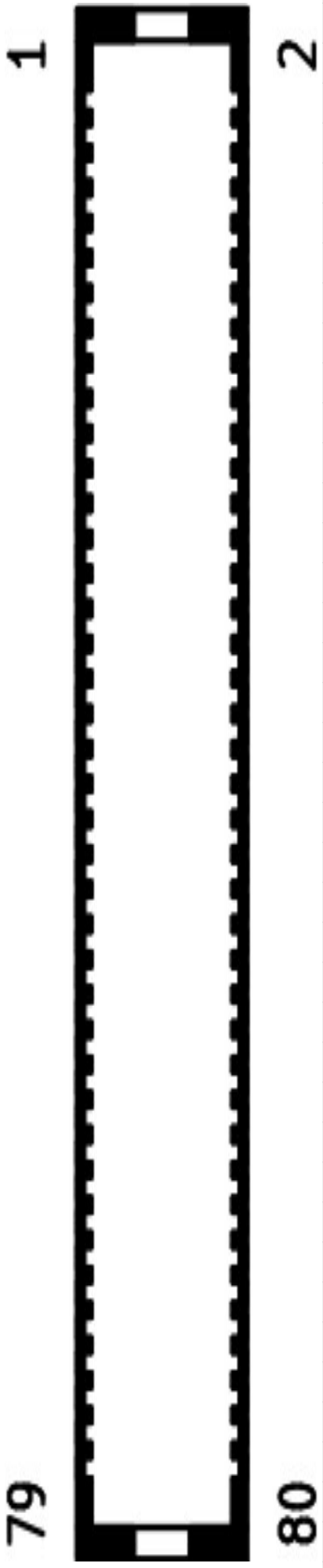


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BTB J2 interface pin definition table

Pin Name	Pin		Pin	Pin Name
DGND	J2-1		J2-2	DGND
REFCLK _ OUT _ J2	J2-3		J2-4	USB1 _ DP _ A8
FEL _ A18	J2-5		J2-6	USB1 _ DM _ B8
NMI _ N3	J2-7		J2-8	DGND
RESET _ KEY	J2-9		J2-10	DGND
DGND	J2-11		J2-12	USB0 _ DP _ B7
PG0 _ B2	J2-13		J2-14	USB0 _ DM _ C7
PG1 _ B3	J2-15		J2-16	DGND
PG2 _ A3	J2-17		J2-18	DGND
PG3 _ C3	J2-19		J2-20	PF0 _ C2
PG4 _ A4	J2-21		J2-22	PF1 _ C1
PG5 _ B4	J2-23		J2-24	PF2 _ D2
DGND	J2-25		J2-26	PF3 _ D1
PG6 _ B5	J2-27		J2-28	PF6 _ D3
PG7 _ C5	J2-29		J2-30	PF5 _ E2
PG8 _ A6	J2-31		J2-32	PF4 _ E3
PG9 _ B6	J2-33		J2-34	DGND
PG10 _ C6	J2-35		J2-36	DGND
PG11 _ D4	J2-37		J2-38	PE17 _ M6
DGND	J2-39		J2-40	PE12 _ R5
PG12 _ D5	J2-41		J2-42	PE14 _ N4
PG13 _ D6	J2-43		J2-44	PE15 _ N5
PG14 _ E6	J2-45		J2-46	PE16 _ N6
PG15 _ F6	J2-47		J2-48	PE11_N1
PG16_F7	J2-49		J2-50	DGND
PG17_E7	J2-51		J2-52	PE10_P3
PG18_D7	J2-53		J2-54	PE9_P2
DGND	J2-55		J2-56	PE8_R3
DGND	J2-57		J2-58	PE6_R1
VDD_3V3_SOM	J2-59		J2-60	PE7_R2
DGND	J2-61		J2-62	PE13_R4
VDD_1V8_SOM	J2-63		J2-64	DGND
DGND	J2-65		J2-66	PE4_T2
DGND	J2-67		J2-68	PE5_T3
V5_IN	J2-69		J2-70	PE1_U1
V5_IN	J2-71		J2-72	PE2_U2
V5_IN	J2-73		J2-74	PE0_V1
V5_IN	J2-75		J2-76	PE3_U3
V5_IN	J2-77		J2-78	DGND
V5_IN	J2-79		J2-80	DGND



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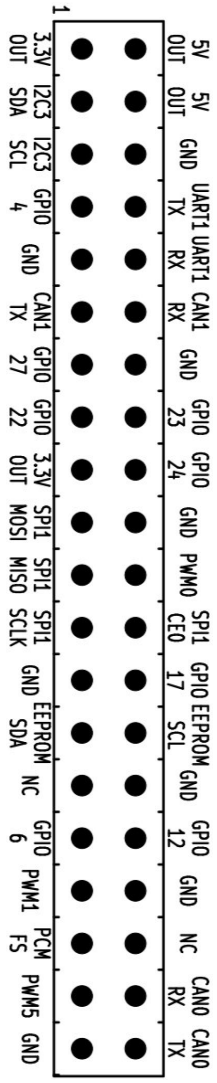
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3.2.Extended interface pin definition

The ECB30-PGT13IC-I motherboard is designed with a 2.54 mm pitch compatible Raspberry Pi expansion interface. The pin definitions are shown in the following table:

Extension interface pin definition table

function	Pin number
3.3 V _ OUT	1
I2C3_SDA	3
I2C3_SCL	5
PB7	7
GND	9
CAN1_TX0	11
PD14	13
PG14	15
3.3 V _ OUT	17
SPI1_MOSI	19
SPI1_MISO	21
SPI1_SCLK	23
GND	25
EEPROM _ SDA	27
NC	29
PB0	31
PWM1	33
PCM _ FS	35
PWM5	37
GND	39



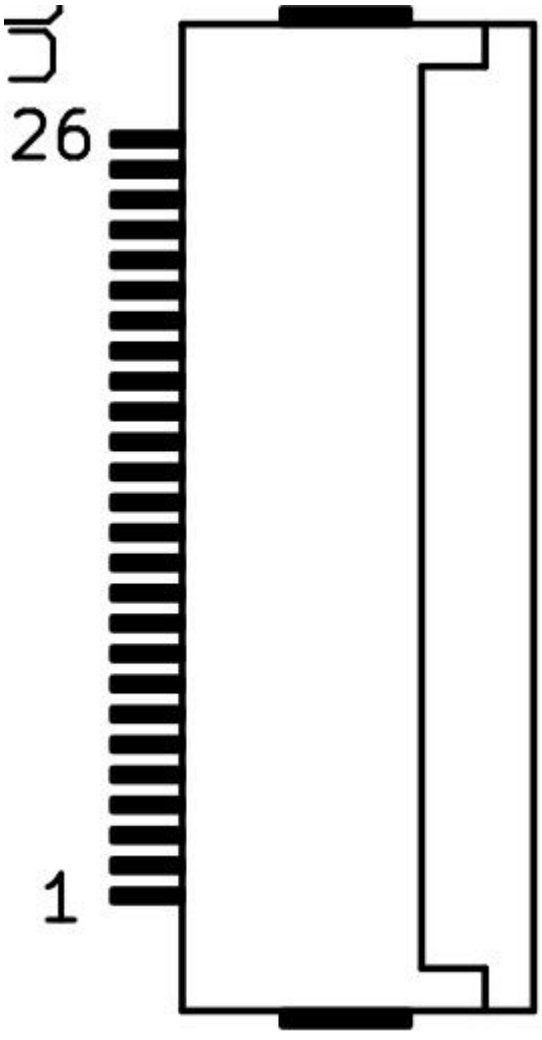
Pin number	function
2	5V_OUT
4	5V_OUT
6	DGND
8	UART1_TX
10	UART1_RX
12	PCM _ CLK CAN1_RX
14	GND
16	PG15
18	PG11
20	GND
22	PD16
24	SPI1_CE0
26	PE10
28	EEPROM _ SCL
30	GND
32	PWM0
34	GND
36	NC
38	PCM _ DIN CAN0_RX
40	PCM _ DOUT CAN0_TX

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3.3.LCD Interface Definition

The ECB30-PGT13IC-I motherboard offers 1 MIPI video output and supports 1920x10 80 @ 60fps display. The interface adopts a 26Pin flip-top type with a pitch of 0.5 mm to be connected to the FPC seat. Can be connected to Ebyte ECA11-5LM1019C touch scree n module for use. When wiring, pay attention to the interface screen 1 corresponding to 2 6. The LCD interface definition is shown in the following table:



LCD interface pin definition table

Pin number	function	Level	Type
26	5V_IN	5V	PWR _ I
25	5V_IN	5V	PWR _ I
24	TP _ INT	3.3 V	DI
23	TP_I2C_SCL	3.3 V	I/O
22	TP_I2C_SDA	3.3 V	I/O
21	TP RST	3.3 V	DI
20	LCD _ BL _ PWM	3.3 V	DO
19	LCD _ ID	1.8 V	DI
18	DGND	GND	PWR
17	MIPI_DSI_D1P	1.8 V	DO
16	MIPI_DSI_D1N	1.8 V	DO
15	DGND	GND	PWR
14	MIPI _ DSI _ CLKP	1.8 V	DO
13	MIPI _ DSI _ CLKN	1.8 V	DO
12	DGND	GND	PWR
11	MIPI_DSI_D0P	1.8 V	DO
10	MIPI_DSI_D0N	1.8 V	DO
9	DGND	GND	PWR
8	MIPI_DSI_D2P	1.8 V	DO
7	MIPI_DSI_D2N	1.8 V	DO
6	DGND	GND	PWR
5	MIPI_DSI_D3P	1.8 V	DO
4	MIPI_DSI_D3N	1.8 V	DO
3	DGND	GND	PWR
2	MIPI _ DSI _ RESET	1.8 V	DI
1	DGND	GND	PWR

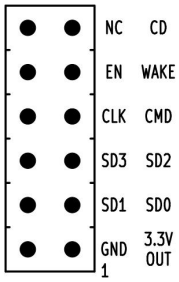
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3.4.Wi-Fi module interface definition

The ECB30-PGT13IC-I motherboard is designed with a 1-channel Wi-Fi module interf ace, using dual-row 2.54-row female leads. The pin definitions are shown in the following table:Wi-Fi module interface pin definition table

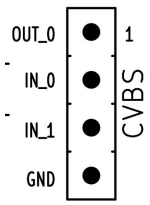
function	Pin number
NC	12
EN	10
SDIO1_CLK	8
SDIO1_SD3	6
SDIO1_SD1	4
GND	2



Pin number	function
11	CD
9	WAKE HOST
7	SDIO1_CMD
5	SDIO1_SD2
3	SDIO1_SD0
1	3.3 V _ OUT

3.5.CVBS analog video interface

The ECB30-PGT13IC-I motherboard is designed with 1-channel TV _ OUT and 2-cha nnel TV _ IN analog video interfaces, using 2.54 rows of pins to lead out. The pin defin itions are shown in the following table:



Analog Video Interface Pin Definition Table

Pin number	function
1	TV_OUT0
2	TV_IN0
3	TV_IN1
4	GND

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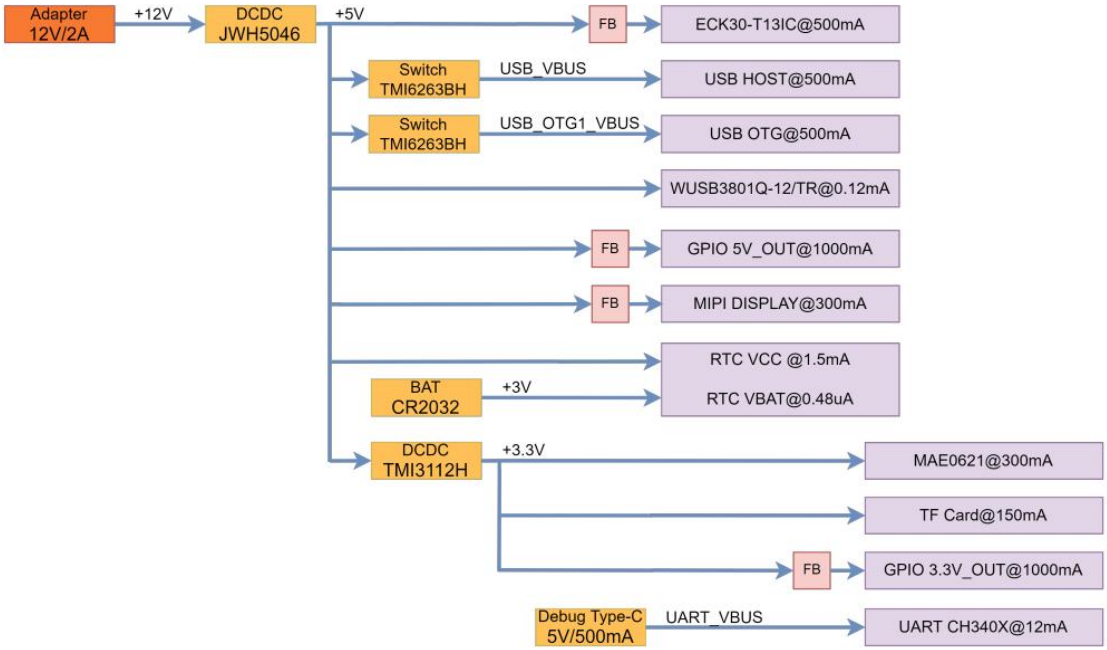
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4. Circuit design

4.1.power supply

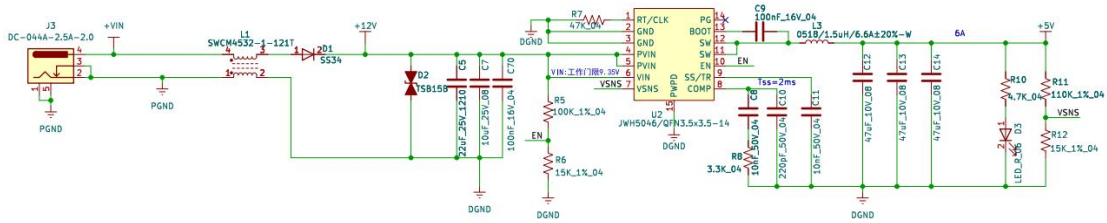
4.1.1. Power Tree

The block diagram of the motherboard power tree is as follows:



Motherboard power tree block diagram

4.1.2. 12V to 5V DCDC reference circuit



12V to 5V power supply reference circuit diagram

The core board needs to provide a voltage of 5V for normal operation, and the full l oad power consumption is close to 0.1 W. Considering that the instantaneous current of th e core board is relatively large when it is powered on, and the performance of the circuit itself will be derated under high temperature conditions, if the power supply power is no t enough, the system will not start normally, so the power supply design must leave a cer tain power margin to ensure the stable and reliable operation of the system.

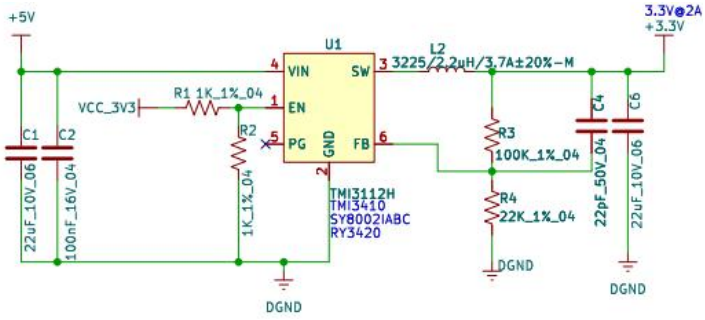
If DC-DC power supply is used to supply power to the core board, the power margi

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n of the power supply should not be too large in power supply design. If the design pow er of the power supply is too large, many power supplies will work in discontinuous PW M mode in order to ensure conversion efficiency, and the ripple of the output power supp ly will increase significantly, which is not conducive to the working stability of the digital signal system. If the LDO is used to supply power to the core board, the power loss an d working temperature rise of the LDO itself should be considered in the design to preve nt the LDO power supply from over-temperature stopping or burning when working in a high-temperature environment or environment with poor heat dissipation.

4.1.3. 5V to 3.3 V DCDC reference circuit



5V to 3.3 V power supply reference circuit diagram

DCDC chip is used to convert 5V to 3.3 V, and the design load capacity is 2A.

Considering the power-on timing problem of some interface circuits in the rear stage, the 3.3 V power domain is designed to be controlled by MCU. The EN pin of the powe r chip is connected to the core board VCC _ 3V3 power supply. When the core board is powered on normally, the chip will work when the EN pin voltage is higher than 1.5 V, and the configuration voltage is 1.65 V. Add R2 and R3.

This design 5V to 3.3 V DCDC chip is also compatible with TMI340, TMI3112H, S Y8002IABC, RY3420.

4.1.4. Layout Recommendations

- The distance between the different power planes is at least 20 mil apart;
- Try to widen the width of the power line and ground wire to meet the required rated c urrent value.
- The width of the feedback signal should not be too narrow, and it is recommended to be more than 10mil;

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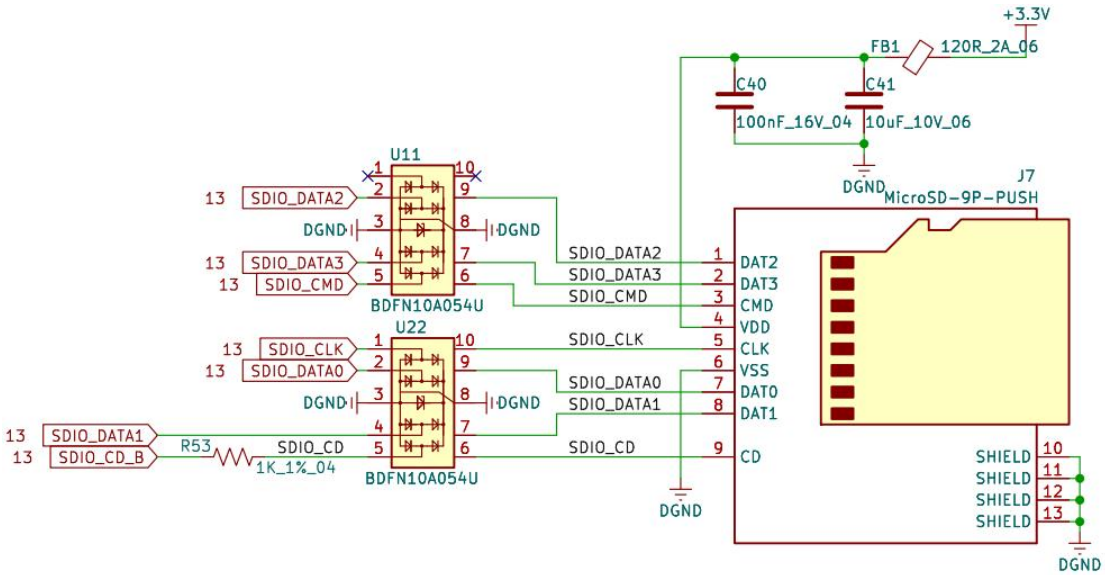
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- It is not recommended to take signal lines in the area below the inductor;
- The path of the current loop is as short as possible, and the inductors and capacitors ar e placed as close as possible to the chip;
- Try to choose a capacitor with small ESR as far as possible as the output capacitor;
- DCDC chips, inductors, capacitors and other main components are recommended to be placed on the top layer to facilitate subsequent debugging. At the same time, reducing vias can effectively reduce parasitic effects and electromagnetic interference;
- The input capacitor is placed through the DCDC input pin to ensure that the input curr ent is filtered by the capacitor before entering the chip;
- The feedback voltage is taken from the output capacitor immediately next to the capacit or;

4.2.BOOT

There is no need to focus on the boot bit configuration when designing the backplan e. If the SD card is inserted and the image has been burned in the card, the board will f irst boot from the SD card. After removing the Micro SD card, the single board PC can be booted from eMMC.

4.3.TF interface design



TF interface reference circuit diagram

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ECK30-T13IC SeriesThe core board leads out 2-way SDC (SD/MM host controller) c ontrollers, including SDC0 and SDC1. The SDC0 complies with the Secure Digital Memor y v3.0 protocol and is typically used to connect SD cards. The SDC1 complies with the Secure Digital I/O v3.0 protocol and is typically used to connect extended functions, such as WiFi modules. SDC2 complies with the Multimedia Card v5.0 protocol and is typicall y used to connect eMMC memory chips. ECK30-T13IC SeriesThe core board uses SDC2 to expand the on-board eMMC memory chip. It is recommended that the backplane use S DC0 to connect the SD card. SDC2 recommends extending other devices or not using the m.

The I/O of the Allwinner T113-I processor can be configured with on-chip pull-up res istors. These pull-up resistors can meet the pull-up requirements when the SD card interfa ce is expanded, and the user design does not require external pull-up resistors. The core b oard has a 33 ohm matching resistor connected in series to the clock signal of SDIO _ C LK (PF2), and the user design does not require an external series resistor. Expand the Mi cro SD card via the SDC0 interface.

4.3.1. Layout Recommendations

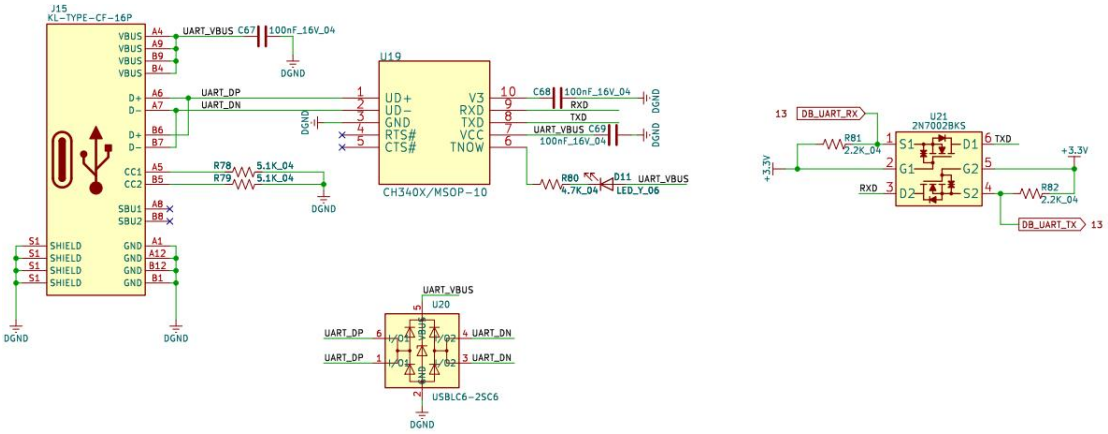
- The interface signal needs to be impedance controlled, using a single-ended impedance of 50Ω;
- The SDIO signal line should be as long as possible, and the error should be less than ± 20 mil;
- If there is sufficient wiring space, the CLK signal will be processed as close as possibl e. If you can't, distance the clock signal from other signals and follow the 3W rule.
- The SDIO _ CD _ B pin is connected in series with a 1K resistor to improve ESD pe rformance.

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4.4.Debugging serial port design

4.4.1. TuneTry UART reference circuit



UART circuit schematic diagram

The motherboard defaults to UART0 as the debugging serial port and uses Type-C le ad out. Users only need a USB Type-C cable to debug when using it.

The CH340X chip is used to convert the USB signal into the debugging serial port s ignal, and the CH340X chip is powered by the 5V voltage on the external Type-C line.

Current backflow should be considered when designing the circuit. A 2N7002BKS dua l NMOS transistor is used to prevent the PC from generating current backflow to the MC U through the RXD or TXD internal diodes of the MCU in the dual power mode.

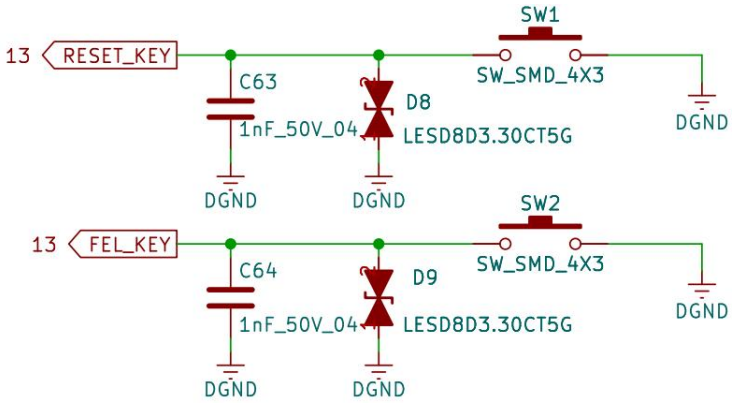
4.4.2. Layout Recommendations

- The TVS is placed near the TYPE-C interface;
- Isolate the signals before and after, and the power plane ensures sufficient distance.

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4.5.Reset and Power buttons



Reference circuit diagram for reset and download keys

The RESET _ KEY signal can be connected to an external key to realize the reset c ontrol of the processor. The RESET _ KEY signal is an input-output bidirectional signal, which can be used as an external reset input to reset the processor, and it is also the out put of the processor memory power reset signal.

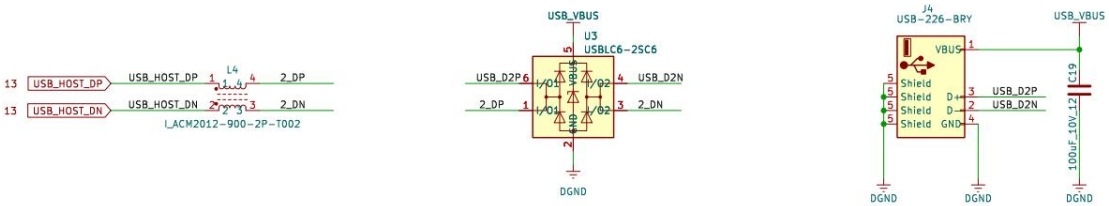
The FEL _ KEY signal is used to burn the image. Press it before powering on, and then release it after powering on, and it will enter the burning image mode.

The RESET _ KEY and FEL _ KEY signals provide a 10K pull-up resistor within th e core board. Therefore, don't connect the pull-up resistor to the bottom plate, directly con nect the button, or drive it through the OD gate. Don't drive these two signals through th e interface of push-pull output either. When connecting the manual input button, a small c apacitor and TVS can be placed to reduce interference and improve ESD performance.

4.6.USB _ HOST interface design

ECK30-T13IC Series. The core board supports 2 USB2.0 interfaces. USB0 supports H OST and Device modes, and USB1 only supports HOST mode.

4.6.1. USB _ HOST interface reference circuit



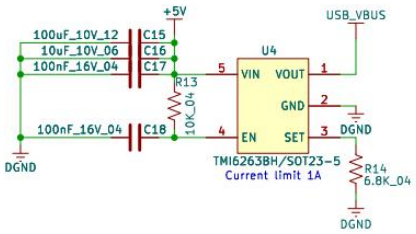
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USB interface reference circuit diagram

The ECB30-PGT13IC-I motherboard is designed with 1-way USB2.0 interface. Place a common-mode inductor and TVS on the USB signal line. It is recommended that the par asitic capacitance of the TVS be less than 2pF.

4.6.2. Power supply current limiting reference circuit



USB power supply current limiting reference circuit diagram

The USB single-channel power supply voltage is 5.0 V ± 10%. The USB on the bac kplane of the motherboard uses USB _ VBUS power supply. Considering that the USB de vice requires a large current when it is just connected, the TMI6263BH chip is used to li mit the current to 1A. The SET pin of the TMI6263BH is the current limiting configurati on pin, Iset = 6.8 k/Rset.

4.6.3. Layout Recommendations

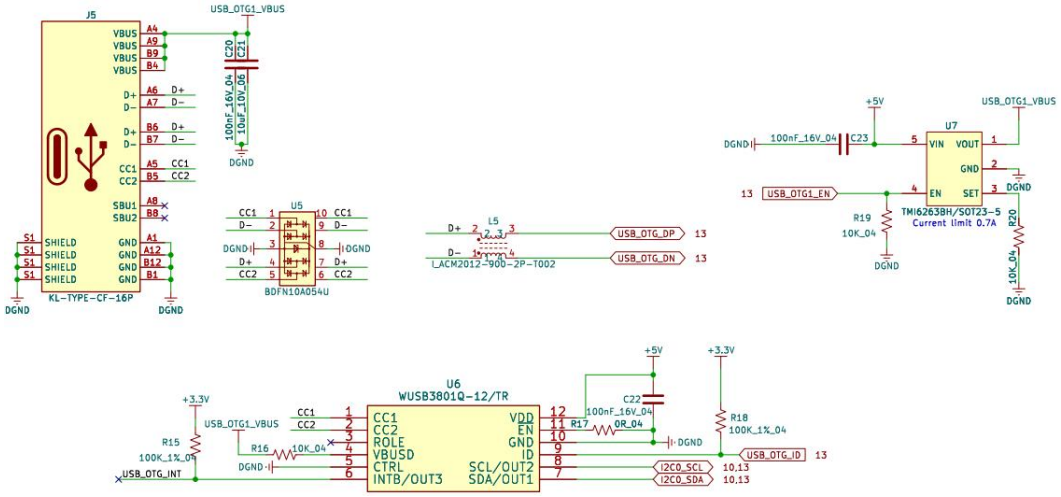
- The USB _ DP/USB _ DN signal takes a differential line, and the differential impedan ce is 90Ω, ensuring that the adjacent layers of the trace have a continuous and comp lete same reference plane;
- The distance between the USB _ DP/USB _ DN signal line and other traces is greater than 10mil, so try to avoid tracing under the device;
- The USB _ DP/USB _ DN signal line traces are as short as possible, the length does not exceed 4000mil, the corner angle of the trace is greater than or equal to 135 deg rees, and the number of trace vias does not exceed 2;
- Try not to change layers of the USB _ DP/USB _ DN signal line. If the layer is chan ged, a GND return via needs to be placed within 50mil from the layer change via;
- The TVS is placed close to the interface.

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4.7.USB _ OTG interface design

4.7.1. OTG reference circuit



USB _ OTG reference circuit diagram

The OTG identification chip WUSB3801Q-12 is used to detect whether the externally inserted Device is Device or Host. When the access Device is Device, the USB current l imiting chipTMI6263BH is enabled, thereby supplying external power. At the same time, t he USB current limiting chip will limit the current to 700mA.

4.7.2. Layout Recommendations

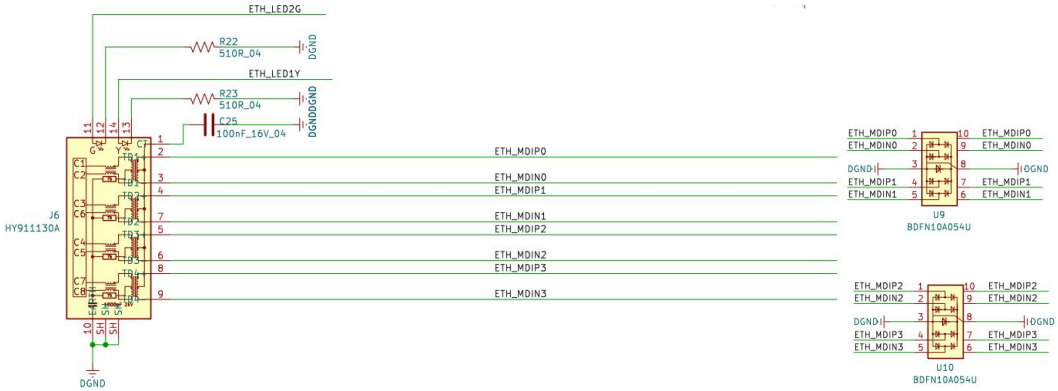
- The OTG _ DN/OTG _ DP signal takes a differential line, and the differential impedan ce is 90Ω, ensuring that the adjacent layers of the trace have a continuous and comp lete same reference plane;
- The VBUS power trace should be wide enough to ensure that it can pass enough curre nt;
- The TVS is placed close to the interface.

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4.8.Network interface design

4.8.1. RJ45 connector reference circuit



Network RJ45 interface reference circuit diagram

A Gigabit RJ45 interface is designed on the backplane. Voltage type PHY is adopted, and the middle tap of the transformer is connected in series with capacitor to ground. The RJ45 LED indication content is shown in the following table:

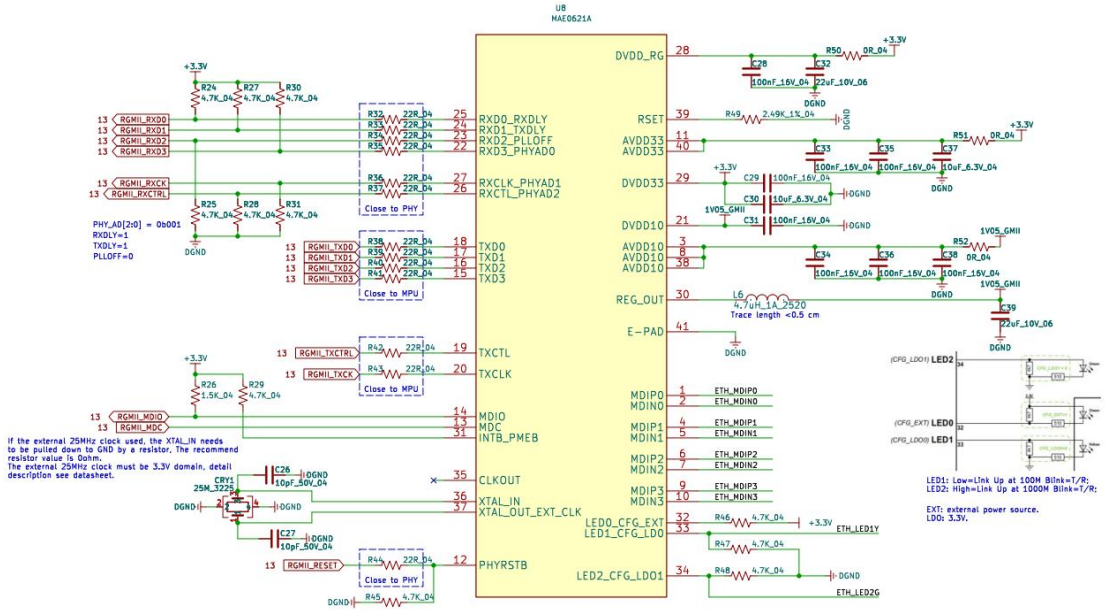
Direct connection LED status indicator

Connection status	LED status	Transmission status	LED status
10M connection	Doesn't light up	10M transmission	Doesn't light up
100M connection	Yellow LED on	100M transmission	Yellow LED flashing
1000M connection	Green LED on	1000M transmission	Green LED flashing

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4.8.2. PHY reference circuit



Network PHY Circuit Reference Circuit Diagram

The ECK30-T13IC series core board supports 1-channel 10M/100M/1000M adaptive E thernet controller. The Ethernet controller supports RGMII and RMII interfaces. The MII i nterface on the core board is reused for the PE/PG pin and only supports the 3.3 V level. There is no Ethernet PHY circuit designed in the core board. Users need to design PHY interface chip circuit on the backplane to use Ethernet functions. The default address of PHY design on the backplane circuit is 001.

4.8.3. Layout Recommendations

- Do not route or lay copper under the network socket to prevent the interference on the ground from coupling to the transformer or routing and affecting the signal quality;
- RGMII differential pairs need to be controlled at equal intervals, with an equal length e rror of ± 10 mil and a differential impedance of 100 Ω ± 10%;
- The length of the signal trace from PHY to the transformer terminal shall not exceed 1 2cm, and try to avoid punching and layer conversion;
- The 2.49 K RESET resistor is placed close to the PHY, no more than 0.5 cm away, an d should be as far away from other signal lines as possible to avoid unnecessary inte rference;
- The 22 ohm matching resistor on the RX data line and clock line is placed close to P

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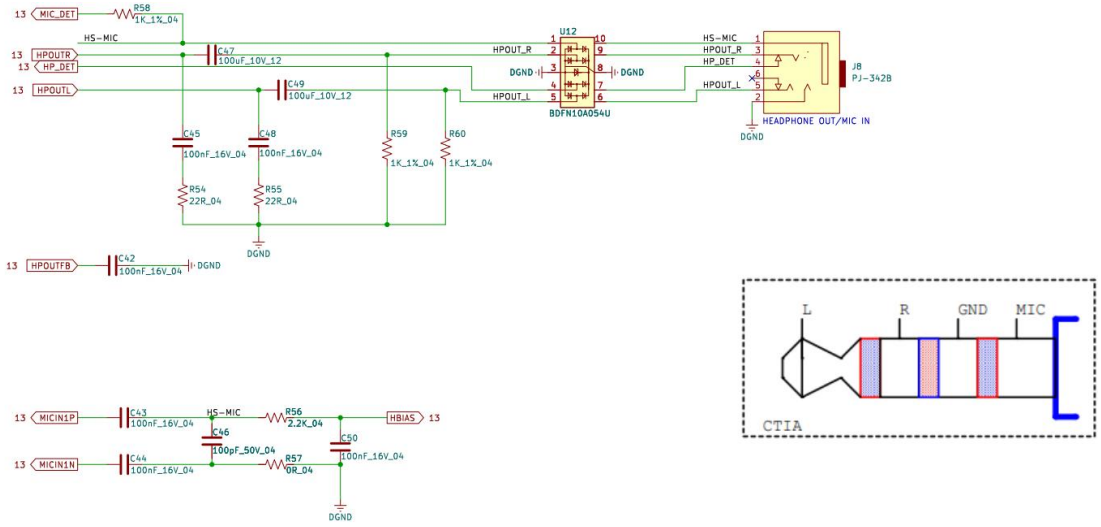
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HY, the 22 ohm matching resistor on the TX data line and clock line is placed close to MCU, and the matching capacitor on the RGMII _ RESET line is placed close to PHY;

- The TVS is placed close to the mesh port seat.

4.9.Audio interface design

4.9.1. Audio interface reference circuit



Audio chip circuit reference diagram

The ECK30-T13IC series core board supports analog audio interface and leads out signals: 1 channel FM _ IN, 1 channel LINE _ IN, 3 channel MIC _ IN, 1 channel LINE _ OUT (two channels), and 1 channel HP _ OUT (two channels). The backplane leads out the HP _ OUT and MIC _ IN signals to realize the headphone microphone function.

The audio interface uses 4 3.5 mm audio sockets, including headphone and microphone functions, and has headphone and microphone detection functions.

4.9.2. Layout Recommendations

- MICIN1N/MICIN1P signal lines are routed according to differential lines;
- The layout of the audio circuit is far away from the interference source. It is recommended to plan an area separately on the PCB for placing analog circuits;
- This design belongs to analog audio signals, and the power supply spacing of 10mil and above is recommended;

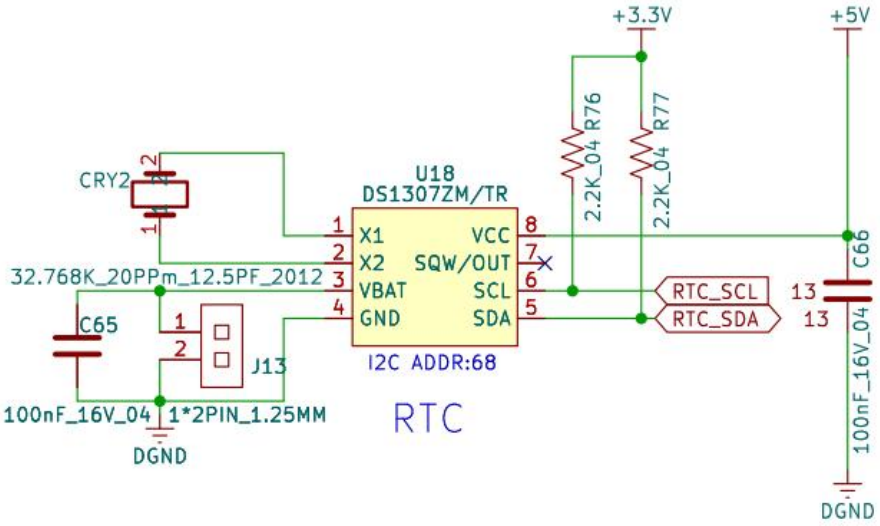
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● Digital ground and analog ground are grounded at a single point.

4.10.RTC battery interface

4.10.1. RTC clock circuit reference circuit



RTC clock circuit schematic diagram

There is no RTC on the ECK20-6Y28C series core board powered by backup batterie s. The backplane uses a separate RTC chip. The chip is equipped with automatic power-of f detection and power switching circuit. The main power supply is powered by + 5V pow er supply, and the backup power supply is powered by + 3V battery. The battery voltage must be kept at 2.0 V to 3.5 V before it can work normally. The battery is recommended Use CR2032.

The chip comes with a 12.5 pF load capacitor and an external 32.768 K crystal oscil lator.

4.10.2. Layout Recommendations

● The crystal oscillator is placed close to the RTC chip.

● The wiring of the battery holder should be appropriately thickened to reduce wiring resi stance and reduce line loss.

4.11.Layout Recommendations

● The USB _ DP/USB _ DN signal takes a differential line, and the differential impedan

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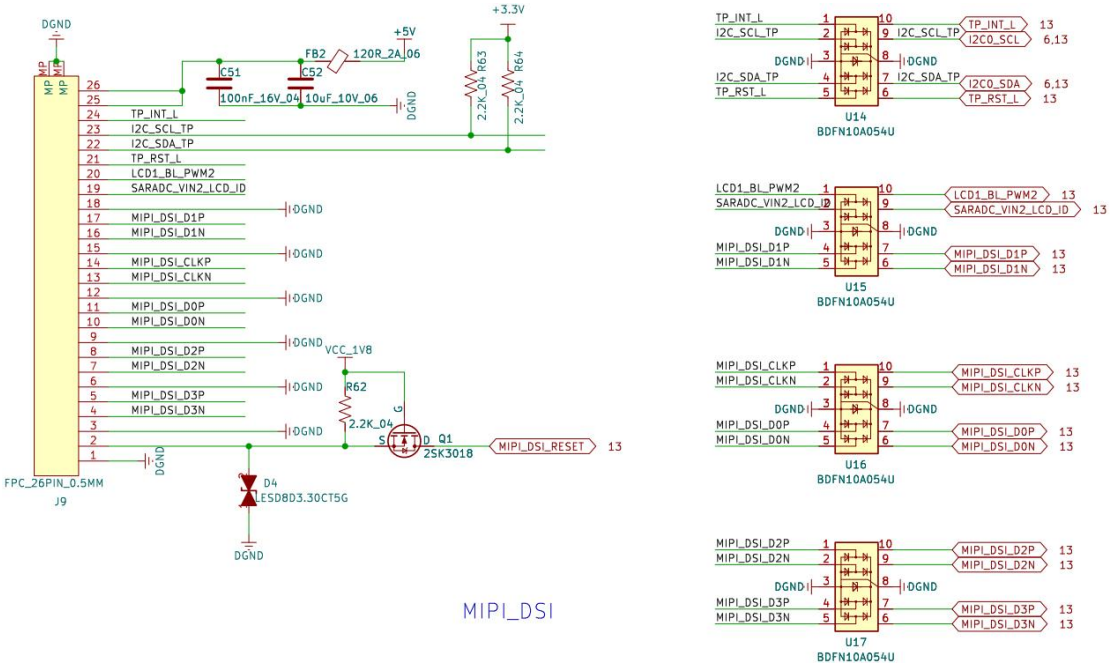
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ce is 90Ω, ensuring that the adjacent layers of the trace have a continuous and comp lete same reference plane;

- The distance between the USB _ DP/USB _ DN signal line and other traces is greater than 10mil, so try to avoid tracing under the device;
- The USB _ DP/USB _ DN signal line traces are as short as possible, the length does not exceed 4000mil, the corner angle of the trace is greater than or equal to 135 deg rees, and the number of trace vias does not exceed 2;
- Try not to change layers of the USB _ DP/USB _ DN signal line. If the layer is chan ged, a GND return via needs to be placed within 50mil from the layer change via;
- The TVS is placed close to the interface.

4.12.Design of MIPI Display Interface

4.12.1. MIPI display interface reference circuit



MIPI Display Interface Reference Circuit Diagram

The backplane is designed with a MIPI touch screen module interface, which can be connected to the Ebyte ECA11-5LM1019C touch screen module. The LCD _ PWM signal is used to adjust the screen backlight, and a TVS is used to prevent the touch screen ba cklight power chip from being damaged by interference.

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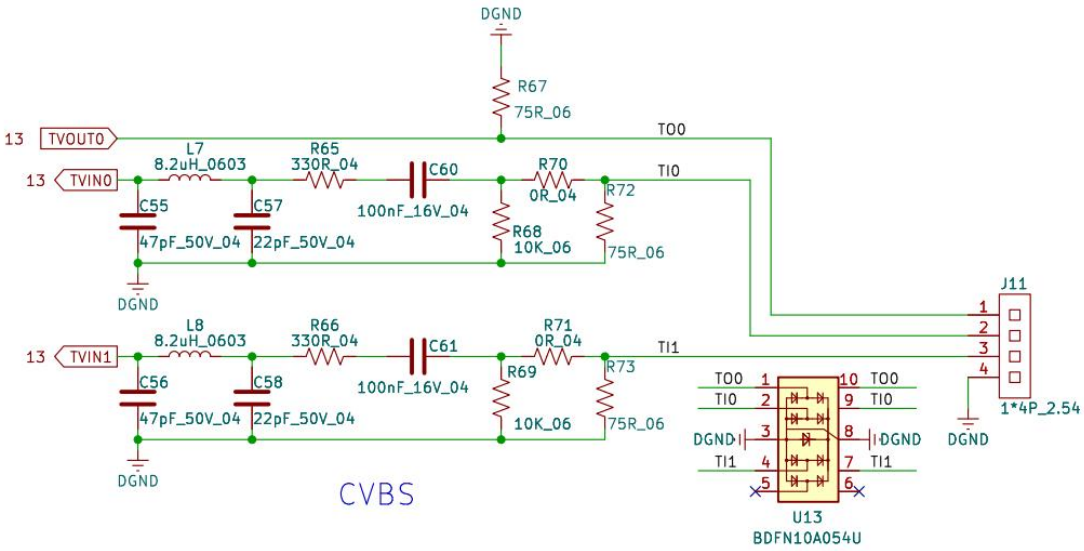
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4.12.2. Layout Recommendations

- RGB signal traces are controlled by equal length, with an error range of ± 20 mil, meeting the 50Ω impedance design;
- The TVS is placed close to the interface.

4.13.CVBS Interface design

4.13.1. CVBS Interface reference circuit



The ECK20-6Y28C series core board has 3 dedicated pins TVOUT0, TVIN0, and TV IN1 for analog video output interfaces. The motherboard leads these two signals out to pins at 1 * 4P 2.54 mm pitch. Signal port plus TVS prevents static interference.

4.13.2. Layout Recommendations

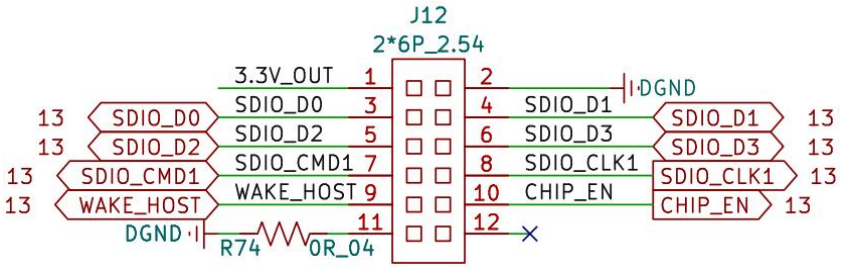
- The video signal line is traced according to the impedance of 37.5 Ω. Note that the corner of the trace cannot be less than 135 degrees;
- The 75Ω resistor is placed close to the interface.

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4.14.Wi-Fi Module Interface Design

4.14.1. Wi-Fi module interface Circuit



The ECK20-6Y28C series core board is designed with a Wi-Fi module interface, whic h uses dual-row 2.54-row bus leads. Wi-Fi module that can be connected to SDIO commu nication mode. The pin 11 signal is a CD signal, which is pulled down on the board to no longer detect whether a module is inserted. WAKE _ HOST is the module wake-up ho st signal.

4.14.2. Layout Recommendations

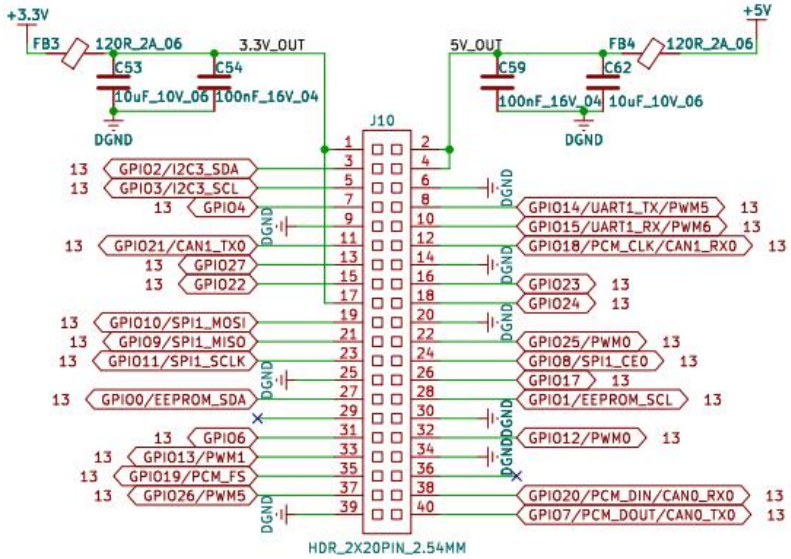
- The interface signal needs to be impedance controlled, using a single-ended impedance of 50Ω;
- The SDIO signal line should be as long as possible, and the error should be less than ± 20 mil;
- If there is sufficient wiring space, the CLK signal will be processed as close as possibl e. If you can't, distance the clock signal from other signals and follow the 3W rule.

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4.15.Extended interface design

4.15.1. GPIO extension interface reference circuit



Schematic diagram of expansion interface circuit

The main version is designed with an expansion interface compatible with Raspberry Pi, which expands a total of 38Pin power supply and signal. The expansion interface has 5V and 3.3 V power outputs, and the recommended load does not exceed 3W. The signal s lead out CSI, I2C, SPI, AUDIO, IO, UART, and CAN. These signals CAN be configure d to realize functional multiplexing.

The CAN signal is TTL level, which needs to be used by users in conjunction with the level conversion chip. The level conversion chip is recommended as Bairui CTM05S.

4.15.2. Layout Recommendations

- Don't put the double rows of needles too close to the edge of the board, leaving a pro per spacing.
- 1. The silk screen printing on the foot needs to be clearly marked, so be careful to pre vent fool.

5. Software Resources

ECK20-6Y28C series core boards and ECB30-PGT13IC-I motherboards do not come with systems by factory default. Users can go to the official website

Or consult sales to download the cross-compilation tool chain, U-boot source code, source

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code of Linux kernel and each driver module required for embedded Linux system development, as well as various development and debugging tools suitable for Windows desktop environment and Linux desktop environment.

Operating system:

Linux file system built by Buildroot

System source code:

U-boot 2018

Kernel 5.4

BuildRoot 2019.02

openwrt

Development environment and tools:

USB burning tool: PhoenixSuit

SD card burning tool: PhoenixCard

The system software resources are shown in the following table:

System software resource table

Category	Name	Description	Source code
SPL	spl-pub	Boot0, boot uboot	< SDK >/brandy/brandy-2. 0/spl-pub/
BOOT	u-boot 2018.07	Bootstrap	< SDK >/brandy/brandy-2. 0/u-boot-2018/
Kernel	Kernel 5.4. 61	Linux kernel	< SDK >/kernel/linux-5. 4/
Device Driver	Audio	Built-in audio driver	sound/soc/sunxi _ v2/*
	AWlink	CAN Drive	drivers/net/can/sunxi _ awlink.c
	GMAC	Built-in MAC driver	drivers/net/ethernet/allwinner/sunxi-gmac.c
	GPADC	GPADC Driver	drivers/input/sensor/sunxi _ gpadc.c
	GPIO	GPIO driver	drivers/pinctrl/sunxi
	LCD	Disp2 display driver	drivers/video/fbdev/sunxi/disp2/disp/lcd/
	LRADC	Key module driver	drivers/input/keyboard/sunxi-keyboard.c
	SMHC	MMC Drive	drivers/mmc/host/sunxi-mmc.c
	SPI	SPI Drive	drivers/spi/spi-sunxi.c
	SPI-NAND	SPI-NAND driver	drivers/mtd/awnand/spinand
	TVD	CVBS input	drivers/media/platform/sunxi - tvd/
	TVE	CVBS Output	drivers/video/fbdev/sunxi/disp2/tv/
	TWI	I2C Driver	drivers/i2c/busses/i2c-sunxi.c
	UART	Serial port driver	drivers/tty/serial/sunxi-uart.c
	VIN	CSI Driver	drivers/media/platform/sunxi-vin/
Operating system	Buildroot 201902	Version 201902 Buildroot	< SDK >/buildroot/buildroot-201902
	Buildroot 202205	Version 202205	< SDK >/buildroot/buildroot-202205

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		Buildroot	
	openwrt	openwrt	< SDK > openwrt/openwrt
Development tools	PhoenixSuit	USB burning tool	/tools/PhoenixSuit
	PhoenixCard	SD card burning tool	/tools/PhoenixCard

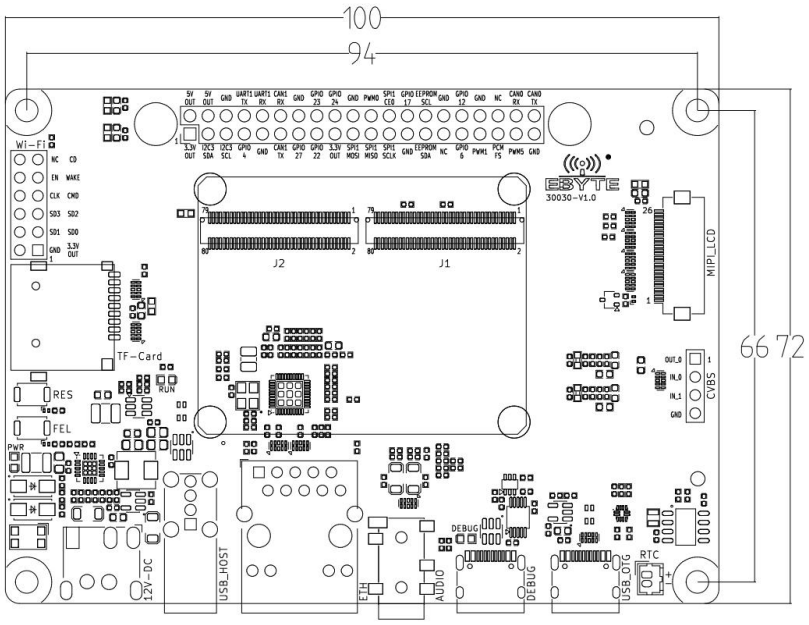
6. Structural dimensions

Unit mm; Error ± 0. 1 mm.

Side thickness:18mm.

The BTB connector closes 3mm high.

The front dimensions are shown below:



Dimensional drawing of front structure of motherboard

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7. Reference Documents

- T113-i _ V1.9. pdf

8. Description of amendments

Revision Description Sheet

version	Modify content	Modification Time	Preparation	proofreading	examine and approve
V1.0	First draft	25-4-23	LJQ	WFX	WFX
-	-	-	-	-	-
-	-	-	-	-	-

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