Product user manual
ECB30-P4T13IA5ME8G-I SBC



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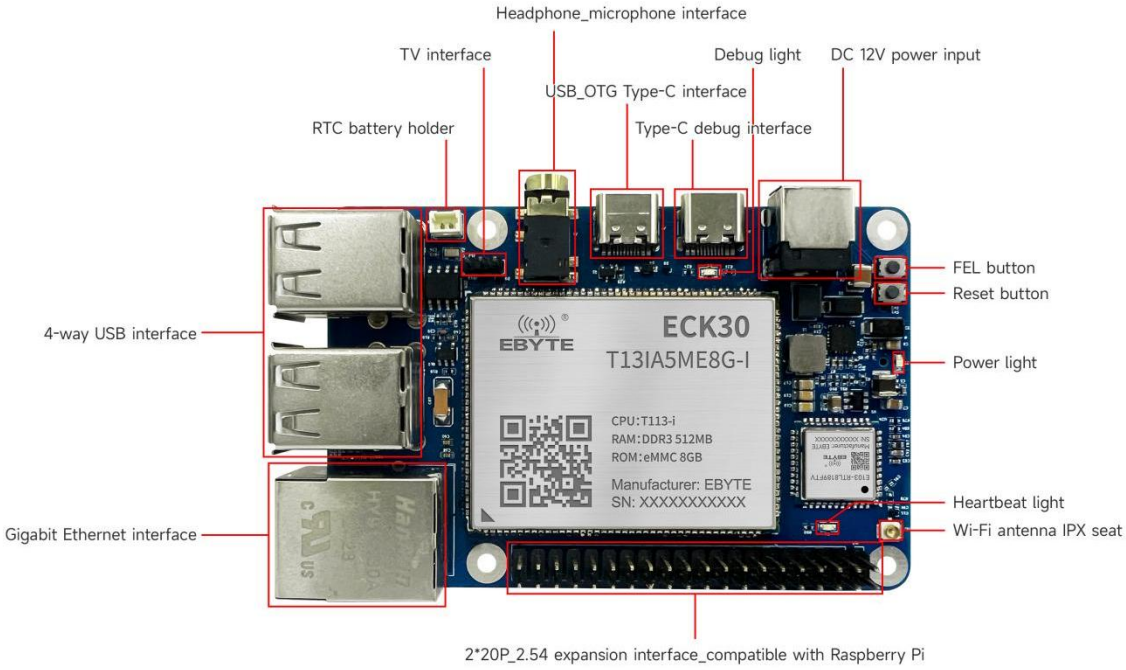
1. Product Overview

1.1. Product Introduction

Based on Allwinner T113-i processor, Ebyte launched a cost-effective single-board computer ECB30-P4T13IA5ME8G-I, which is composed of a core board ECK30-T13IA5ME8G-I and a base plate, and the core board and the base board are combined by stamp hole welding, and the external dimensions are compatible with Raspberry Pi. The design level is higher than that of ordinary development boards, and it can be used in industrial scenarios in batches.

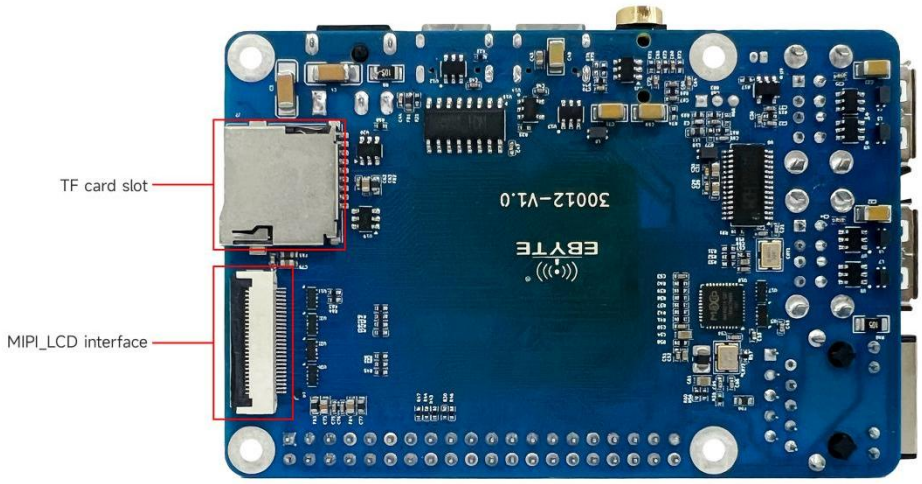
Along with the single board computer, EBT provides a stable reference design and a complete software development environment, which can effectively help users verify the core board functions, improve development efficiency, shorten the development cycle, optimize design quality, and accelerate product development and time to market.

The function diagram of the single board computer is as follows:



Functional description diagram of the front of the single-board computer

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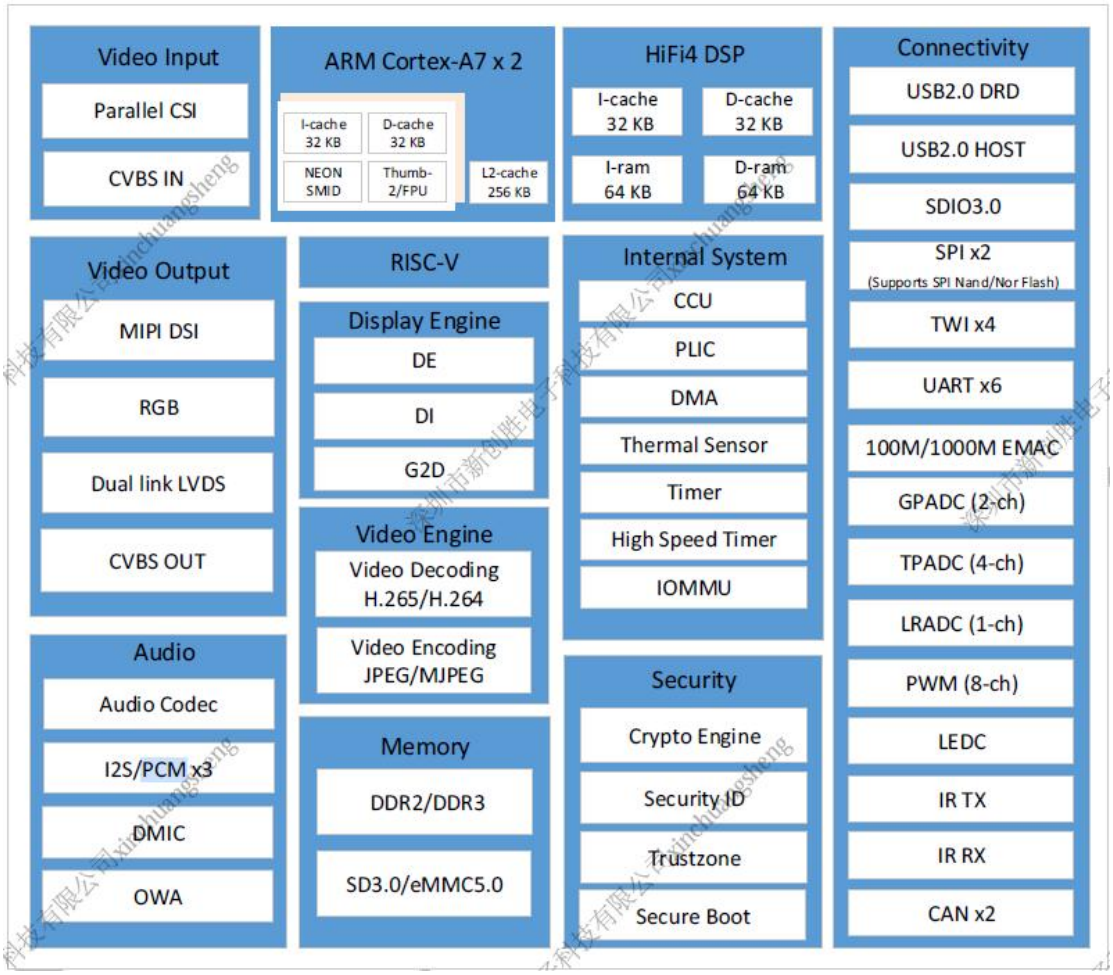


Functional description diagram of the back of the single-board computer

1.2. Introduction to the T113-I chip

Allwinner T113 series processor is a dual-core ARM Cortex-A7 + RISC-V + HiFi4 DSP multi-core heterogeneous industrial-grade processor. It supports H.265, H.264, MPEG-1/2/4, JPEG, VC1 and other full-format 1080P@60FPS video decoding, JPEG/MJPEG 1080P@60FPS video encoding, and has rich multimedia interfaces MIPI-DSI/RGB/LVDS/CVBS/Parallel CSI, and supports 1080P@60FPS display. The integrated ADC/DAC and I2S/PCM/DMIC/OWA audio interfaces work seamlessly with the CPU to accelerate multimedia algorithm applications and improve user experience. The processor also supports Gigabit Ethernet interface, 2 CAN interfaces, 2 USB2.0 interfaces, 6 UART and other functional interfaces. In addition, the T113-i can connect with other different peripherals such as WiFi and Bluetooth via SDIO and UART. The functional block diagram of the T113-i processor is shown in the figure below.

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Block diagram of the T113-i processor system

1.3. ECK30-T13IA5ME8G-I core board introduction

ECK30-T13IA5ME8G-I core board adopts 8-layer board design, immersion gold, lead-free process. The core board integrates Allwinner T113-i CPU, ROM, RAM, power supply, crystal oscillator and other devices. All devices are domestic industrial grade, stable and reliable. The size of the core board is: 45×35×3.6mm, and the signal and power supply are up to 140pin through the stamp hole. It is very suitable for high-volume applications in industrial control, HMI, IoT and other fields.

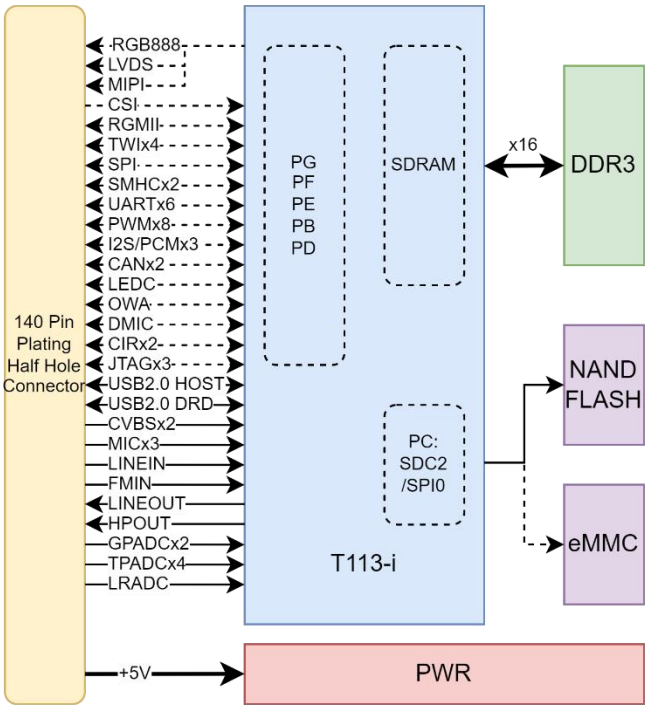
The physical diagram of the ECK30-T13IA5ME8G-I core board (no device on the bottom surface of the product) is as follows:

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Physical drawing

ECK30-T13IA 系列核心板功能框图如下：



Functional block diagram

1.4. Typical Applications

- smart home;
- smart toys;
- smart cities;
- Tablet;
- IoT gateways
- all-in-one advertising machine;

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- industrial all-in-one machine;
- Industrial control motherboards;
- Robot.

2. Specifications

2.1. Functional parameters

ECB30-P4T13IA5ME8G-I Functional parameters of the single board computer

Power input	12V_1A DC input	
processor	Allwinner T113-i processor：Dual Arm Cortex-A7 core，1.2GHz；Darkiron C906 RISC-V(64bit)，1008MHz；HiFi4 DSP，1.2GHz；	
storage	memory	512MB，DDR3；
	FLASH	8GB，eMMC；
display	1 channel 26Pin FPC MIPI display interface, support 4-lane, maximum resolution support 1080P (1920×1080@60fps), support touch screen; 1 CVBS output, support NTSC and PAL; 1 CVBS input, support NTSC and PAL;	
USB HOST	4 channels USB2.0 HOST；	
USB OTG	1 channels USB OTG，Type-C Interface type；	
Ethernet port	1 x 10/100/1000M adaptive RJ45 Ethernet port;	
WiFi	1 channel 2.4G Wi-Fi；	
TF	1 TF card slot, support plugging and unplugging detection;	
audio	1 x 3.5mm audio jack, support headphone output and microphone input;	
debugging	1-way debug serial port, Type-C interface type;	
CAN	2 CAN interfaces, expansion interface lead-out;	
GPIO	28 GPIOs, multiplexed with some functions, and extended interfaces;	
Serial	1 UART communication serial port, TTL level, expansion interface lead-out;	
I2C	2 channels I2C, extended interface lead-out;	
keystroke	1 reset button; 1-way FEL download button;	
Light	1 power indicator; 1 running indicator; 1 debug indicator;	
Watch Dogs	Support on-chip watchdog function;	
RTC	1 x 1.25mm RTC battery holder;	
Power output	2 x 5V 1A power output, extended interface lead-out; 2 x 3.3V 1A power output, extended interface;	

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2.2. Environmental characteristics

ECB30-P4T13IA5ME8G-I Environmental characteristics of a single board computer

Operating temperature	Industrial grade：-40℃ ~ 85℃；
Storage temperature	-40℃ ~ 85℃；
Operating humidity	5~95% humidity, non-condensing;
Storage humidity	60°C@95% humidity, non-condensing;

3. Interface definition

3.1.Core board pin definition

The ECK30-T13IA5ME8G-I core board leads out a total of 118+22PIN signals and power supplies through the stamp holes, and these signal pins contain rich peripheral resources, and most of the signal pins can be freely configured with different functions.

The default I/O assignment pins of the core board are defined as follows:

Core Board Pin Definition Table

Core board pin number	T113-I pin number	Default feature	Level	type
1	Day 2	-	1.8V	TO
2	A18	FEL_KEY	3.3V	OF
3	N3	-	1.8V	I/O
4	M2	RESET_KEY	3.3V	I/O
5	-	DGND	GND	PWR
6	E7	DB_UART_TX	3.3V	I/O
7	D7	DB_UART_RX	3.3V	I/O
8	D6	USB_OTG_ID	3.3V	I/O
9	B6	GPIO0/EEPROM_SAD	3.3V	I/O
10	A6	GPIO1/EEPROM_SCL	3.3V	I/O
11	A3	SDIO_D0	3.3V	I/O
12	B3	SDIO_CMD1	3.3V	I/O
13	B2	SDIO_CLK1	3.3V	I/O
14	C6	CHIP_EN	3.3V	I/O
15	D5	GPIO12/PWM0	3.3V	I/O
16	C5	RTC_SDA	3.3V	I/O

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17	B5	RTC_SCL	3.3V	I/O
18	B4	SDIO_D3	3.3V	I/O
19	A4	SDIO_D2	3.3V	I/O
20	C3	SDIO_D1	3.3V	I/O
21	F7	GPIO26/PWM5	3.3V	I/O
22	D4	GPIO24	3.3V	I/O
23	E6	GPIO22	3.3V	I/O
24	F6	GPIO23	3.3V	I/O
25	-	DGND	GND	PWR
26	D3	SDIO_CD_B	3.3V	I/O
27	C2	SDIO_DATA1	3.3V	I/O
28	C1	SDIO_DATA0	3.3V	I/O
29	D2	SDIO_CLK	3.3V	I/O
30	E2	SDIO_DATA2	3.3V	I/O
31	D1	SDIO_CMD	3.3V	I/O
32	E3	SDIO_DATA3	3.3V	I/O
33	-	DGND	GND	PWR
34	R5	RGMII_TXD3	3.3V	I/O
35	R4	RGMII_RXD2	3.3V	I/O
36	T2	RGMII_TXD0	3.3V	I/O
37	T3	RGMII_TXD1	3.3V	I/O
38	R1	RGMII_TXCTRL	3.3V	I/O
39	R2	RGMII_RESET	3.3V	I/O
40	R3	RGMII_MDC	3.3V	I/O
41	P2	RGMII_MDIO	3.3V	I/O
42	P3	GPIO17	3.3V	I/O
43	N1	RGMII_TXD2	3.3V	I/O
44	N4	RGMII_RXD3	3.3V	I/O
45	N5	RGMII_RXCK	3.3V	I/O
46	N6	GPIO3/I2C3_SCL	3.3V	I/O
47	M6	GPIO2/I2C3_SDA	3.3V	I/O
48	V1	RGMII_RXCTRL	3.3V	I/O
49	U1	RGMII_RXD0	3.3V	I/O
50	U2	RGMII_RXD1	3.3V	I/O
51	U3	RGMII_TXCK	3.3V	I/O
52	-	DGND	GND	PWR
53	G15	GPIO14/UART1_TX/PWM5	3.3V	I/O
54	G16	GPIO15/UART1_RX/PWM6	3.3V	I/O
55	F17	I2C_SCL_TP	3.3V	I/O
56	F15	I2C_SDA_TP	3.3V	I/O
57	F16	RUN_LED	3.3V	I/O
58	M16	GPIO7/SPI1_CE1/CAN0_TX0	3.3V	I/O
59	M15	GPIO20/PCM_DIN/CAN0_RX0	3.3V	I/O

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60	K16	GPIO21/PCM_DOUT/CAN1_TX0	3.3V	I/O
61	K15	GPIO18/PCM_CLK/CAN1_RX0	3.3V	I/O
62	K17	GPIO19/PCM FS	3.3V	I/O
63	Day 15	GPIO4	3.3V	I/O
64	Day 16	GPIO6	3.3V	I/O
65	Day 17	GPIO5	3.3V	I/O
66	-	DGND	GND	PWR
67	W19	MIPI_DSI_D0P	3.3V	I/O
68	V20	MIPI_DSI_D0N	3.3V	I/O
69	V19	MIPI_DSI_D1P	3.3V	I/O
70	U20	MIPI_DSI_D1N	3.3V	I/O
71	-	DGND	GND	PWR
72	U19	MIPI_DSI_CLKP	3.3V	I/O
73	U18	MIPI_DSI_CLKN	3.3V	I/O
74	T19	MIPI_DSI_D2P	3.3V	I/O
75	T18	MIPI_DSI_D2N	3.3V	I/O
76	R20	MIPI_DSI_D3P	3.3V	I/O
77	R19	MIPI_DSI_D3N	3.3V	I/O
78	-	DGND	GND	PWR
79	T17	GPIO8/SPI1_CE0	3.3V	I/O
80	R17	GPIO11/SPI1_SCLK	3.3V	I/O
81	P19	GPIO10/SPI1_MOSI	3.3V	I/O
82	P18	GPIO9/SPI1_MISO	3.3V	I/O
83	N17	GPIO27	3.3V	I/O
84	N16	GPIO16	3.3V	I/O
85	-	DGND	GND	PWR
86	N20	GPIO25/PWM0	3.3V	I/O
87	N19	GPIO13/PWM1	3.3V	I/O
88	M19	LCD1_BL_PWM2	3.3V	I/O
89	M18	MIPI_DSI_RESET	3.3V	I/O
90	V18	TP_INT_L	3.3V	I/O
91	W18	TP_RST_L	3.3V	I/O
92	-	DGND	GND	PWR
93	C17	-	-	TO
94	B17	-	-	TO
95	C16	-	-	TO
96	B16	-	-	TO
97	-	AGND	AGND_AU_DIO	PWR
98	E16	-	-	TO
99	A17	MIC_DET	-	TO
100	D20	MICIN1P	-	TO
101	D19	MICIN1N	-	TO

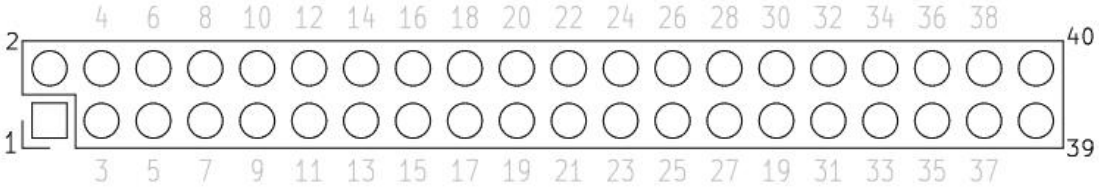
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102	E15	-	-	TO
103	D15	-	-	TO
104	D17	-	-	TO
105	D16	-	-	TO
106	-	AGND	AGND_AU_DIO	PWR
107	B14	-	-	TO
108	C14	-	-	TO
109	B15	-	-	TO
110	C15	-	-	TO
111	E17	HBIAS	-	TO
112	A13	HP_DET	-	TO
113	D13	HPOUTR	-	TO
114	E13	HPOUTFB	-	TO
115	F13	HPOUTL	-	TO
116	-	DGND	GND	PWR
117	E19	-	-	TO
118	C9	-	-	TO
119	B9	-	-	TO
120	-	DGND	GND	PWR
121	B12	-	-	TO
122	C13	SARADC_VIN2_LCD_ID	-	TO
123	B13	-	-	TO
124	C12	-	-	TO
125	A11	-	-	TO
126	B11	-	-	TO
127	C11	-	-	TO
128	-	DGND	GND	PWR
129	A8	USB_HOST_DP	-	I/O
130	B8	USB_HOST_DN	-	I/O
131	-	DGND	GND	PWR
132	B7	USB_OTG_DP	-	I/O
133	C7	USB_OTG_DN	-	I/O
134	-	DGND	GND	PWR
135	-	VOUT	3.3V	PWR
136	-	VOUT	1.8V	PWR
137	-	DGND	GND	PWR
138	-	DGND	GND	PWR
139	-	VOUT	5V	PWR
140	-	VOUT	5V	PWR

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3.2.Extended interface pin definition

ECB30-P4T13IA5ME8G-I HAS RESERVED A 2.54MM 2*20PIN DUAL-PIN PIN CONNECTOR COMPATIBLE WITH RASPBERRY PI, AND SOME IO INTERFACES CAN ALSO BE CONFIGURED FOR OTHER FUNCTIONS, AND THE PINS ARE DEFINED AS SHOWN IN THE FOLLOWING FIGURE:



Extended interface pin definition diagram

Extended interface pin definition table

Pin number	function	Level	type
1	3.3V_OUT	3.3V	PWR_O
2	5V_OUT	5V	PWR_O
3	PE17/I2C2_SDA	3.3V	I/O
4	5V_OUT	5V	PWR_O
5	PE16/I2C2_SCL	3.3V	I/O
6	DGND	GND	PWR
7	PB7/UART3_RX	3.3V	I/O
8	PB8/UART1_TX/PWM5	3.3V	I/O
9	DGND	GND	PWR
10	PB9/UART1_RX/PWM6	3.3V	I/O
11	PE10/UART1_TX/PWM4	3.3V	I/O
12	PB5/PCM_CLK/CAN1_RX0/UART5_RX	3.3V	I/O
13	PD14	3.3V	I/O
14	DGND	GND	PWR
15	PG14	3.3V	I/O
16	PG15	3.3V	I/O
17	3.3V_OUT	3.3V	PWR_O
18	PG11	3.3V	I/O
19	PD12/SPI1_MOSI/I2C0_SCL	3.3V	I/O
20	DGND	GND	PWR
21	PD13/SPI1_MISO	3.3V	I/O
22	PD16/PWM0	3.3V	I/O
23	PD11/SPI1_SCLK/I2C0_SDA/UART3_RX	3.3V	I/O
24	PD10/SPI1_CE/UART3_TX	3.3V	I/O
25	DGND	GND	PWR
26	PB2/CAN0_TX0/UART4_TX	3.3V	I/O

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27	PG9/EEPROM_SDA	3.3V	I/O
28	PG8/EEPROM_SCL/UART3_TX	3.3V	I/O
29	PB1/UART2_RX	3.3V	I/O
30	DGND	GND	PWR
31	PB0/PWM3/UART2_TX	3.3V	I/O
32	PG12/PWM0/UART1_TX	3.3V	I/O
33	PD17/PWM1	3.3V	I/O
34	DGND	GND	PWR
35	PB6/PCM_FS/UART3_TX	3.3V	I/O
36	PD15	3.3V	I/O
37	PG16/PWM5	3.3V	I/O
38	PB3/PCM_DIN/CAN0_RX0/UART4_RX	3.3V	I/O
39	DGND	GND	PWR
40	PB4/PCM_DOUT/CAN1_TX0/UART5_TX	3.3V	I/O

3.3.Analog video interface definition

The ECB30-P4T13IA5ME8G-I provides one CVBS analog video input and one CVBS analog video output. The pin definition is shown in the following diagram:

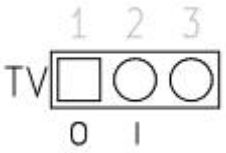


Diagram of the pin definition of an analog video interface

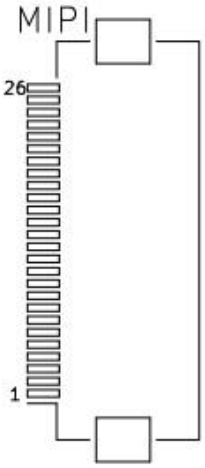
Analog video interface pin definition table

Pin number	function	Level	type
1	TV_OUT	-	TO
2	TV_IN	-	TO
3	DGND	GND	PWR

3.4.MIPI interface definition

ECB30-P4T13IA5ME8G-I provides 1 MIPI video output, supports 1080*1920@60fps display interface, and adopts a 26P clamshell with a pitch of 0.5mm. It can be connected to the ECA11-5P5LCDMIPI1019CT-C MIPI touch screen module. The pin definition is shown in the following diagram:

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MIPI interface pin definition diagram

MIPI interface pin definition table

Pin number	function	Level	type
1	5V_IN	5V	PWR_I
2	5V_IN	5V	PWR_I
3	TP_INT	3.3V	OF
4	TP_I2C_SCL	3.3V	I/O
5	TP_I2C_SDA	3.3V	I/O
6	TP_RST	3.3V	OF
7	LCD_BL_PWM	3.3V	OF
8	LCD_ID	1.8V	OF
9	DGND	GND	PWR
10	MIPI_DSI_D1P	1.8V	OF
11	MIPI_DSI_D1N	1.8V	OF
12	DGND	GND	PWR
13	MIPI_DSI_CLKP	1.8V	OF
14	MIPI_DSI_CLKN	1.8V	OF
15	DGND	GND	PWR
16	MIPI_DSI_D0P	1.8V	OF
17	MIPI_DSI_D0N	1.8V	OF
18	DGND	GND	PWR
19	MIPI_DSI_D2P	1.8V	OF
20	MIPI_DSI_D2N	1.8V	OF
21	DGND	GND	PWR
22	MIPI_DSI_D3P	1.8V	OF
23	MIPI_DSI_D3N	1.8V	OF
24	DGND	GND	PWR
25	MIPI_DSI_RESET	1.8V	OF
26	DGND	GND	PWR

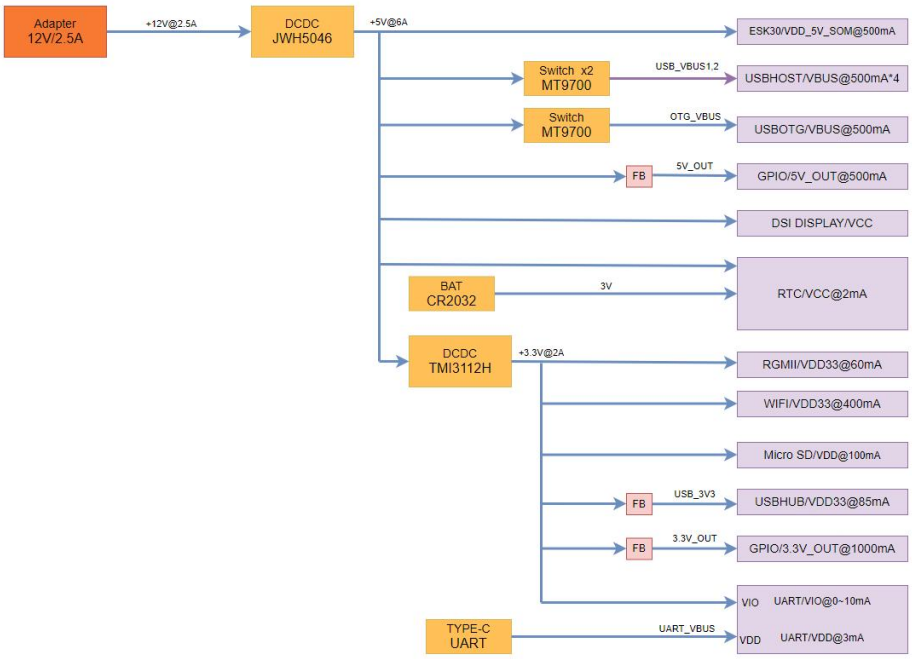
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4. Circuit design

4.1.power supply

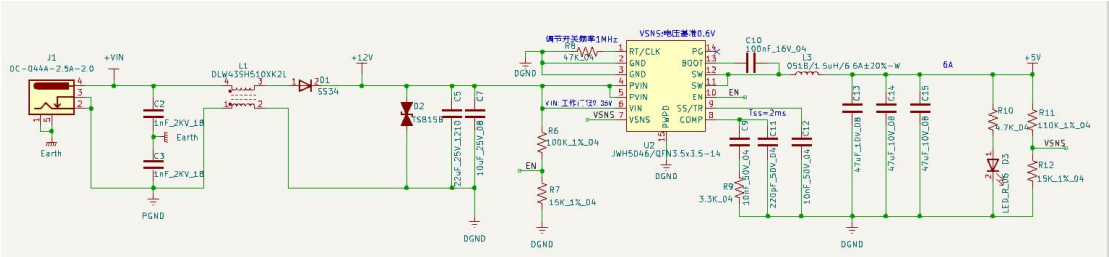
4.1.1. Power tree

The block diagram of the power supply tree of a single board computer is as follows:



Block diagram of the power supply of a single board computer

4.1.2. 12V to 5V DCDC reference circuit



12V to 5V power supply reference circuit diagram

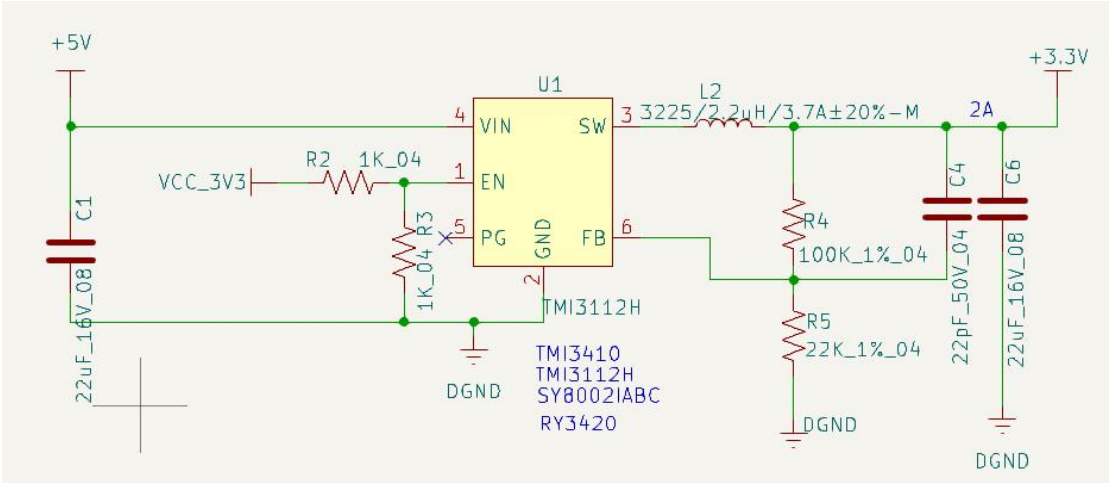
The core board needs to provide a voltage of 5V for normal operation, and the power consumption at full load is close to 1W. Considering that the instantaneous current of the core board is relatively large, and the performance of the circuit itself will be derated under high temperature conditions, if the power supply power is not enough, the system will not be able to

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start normally, so the power supply design should leave a certain power margin to ensure the stable and reliable operation of the system.

If a DC-DC power supply is used to power the core board, the power margin of the power supply should not be too large in the power supply design. If the design power of the power supply is too large, many power supplies will work in discontinuous PWM mode in order to ensure the conversion efficiency, and the output power supply ripple will increase significantly, which is not conducive to the working stability of the digital signal system. If an LDO is used to supply power to the core board, the LDO power loss and operating temperature rise should be considered in the design to prevent the LDO power supply from stopping or burning out when working in a high-temperature environment or an environment with poor heat dissipation.

4.1.3. 5V to 3.3V power supply design



5V to 3.3V power supply reference circuit diagram

The DCDC chip is used to convert 5V to 3.3V, and the design load capacity is 2A.

Considering the power-on timing of some interface circuits in the later stage, the 3.3V power domain is designed to be controlled by the MCU, and the EN pin of the power chip is connected to the core board VCC_3V3 power supply, and the chip will work only after the core board is powered on normally, and the chip will start working when the EN pin voltage is higher than 1.5V, and R2 and R3 will be configured with a voltage of 1.65V.

This design of 5V to 3.3V DCDC chip is also compatible with TMI340, TMI3112H, SY8002IABC, RY3420.

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4.1.4. Layout recommendations

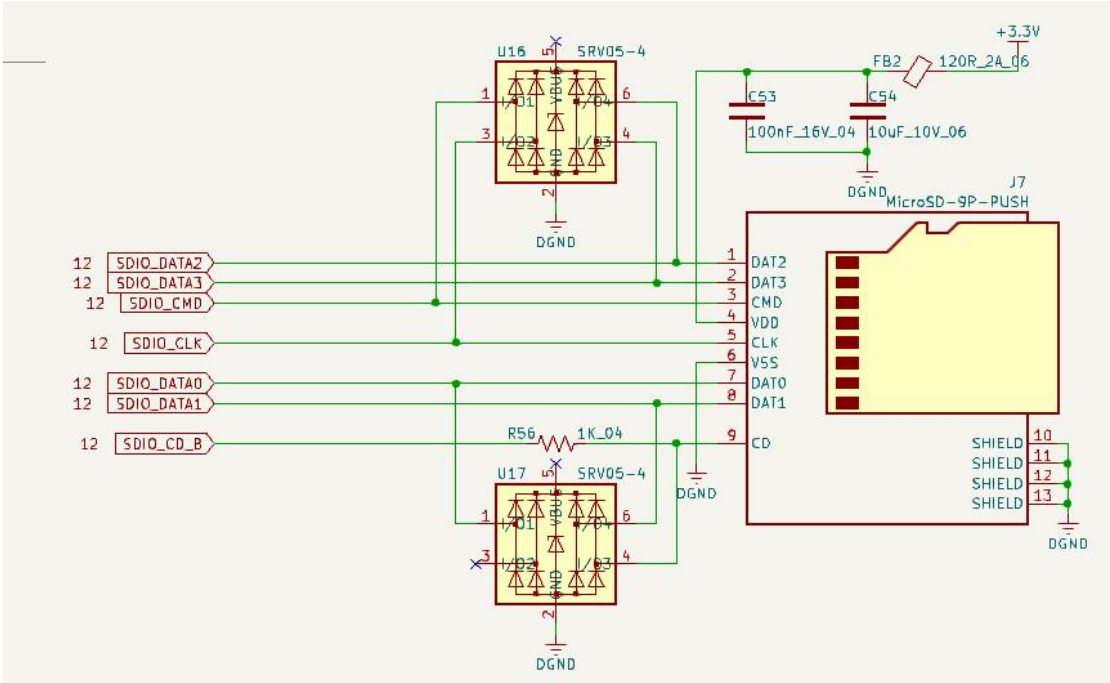
- The distance between different power planes should be at least 20 mils;
- Try to widen the width of the power cord and ground wire, to meet the required rated current value, the width of the feedback signal should not be too narrow, it is recommended to be more than 10mil;
- It is not recommended to take the signal line in the area under the inductor;
- The path of the current loop should be as short as possible, and the inductance and capacitance should be placed as close to the chip as possible;
- The output capacitance should be as small as possible.
- DCDC chips, inductors, capacitors and other main components are recommended to be placed on the top layer to facilitate subsequent debugging, and at the same time, reducing vias can effectively reduce parasitic effects and reduce electromagnetic interference;
- The input capacitor is placed through the DCDC input pin to ensure that the input current enters the chip after being filtered by the capacitor;
- The feedback voltage is taken from the output capacitor and immediately after the capacitor;

4.2.BOOT

There is no need to pay attention to the boot bit configuration when designing the baseplate. If an SD card is inserted and an image has been burned to the card, the board will boot from the SD card first. After removing the Micro SD card, the SBC can be booted from the eMMC.

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4.3.TF interface design



Refer to the circuit diagram for the TF interface

The ECK30-T13IA5ME8G-I core board is equipped with a 3-way SMHC (SD/MM host controller) controller, including SMHC0, SMHC1, SMHC2. SMHC0 conforms to the Secure Digital Memory v3.0 protocol and is usually used to connect SD cards. SMHC1 conforms to the Secure Digital I/O v3.0 protocol and is usually used to connect extended functions, such as WiFi modules. SMHC2 conforms to the Multimedia Card v5.0 protocol and is usually used to connect eMMC memory chips. ECB30-P4T13IA5ME8G-I core uses SMHC2 to extend the eMMC memory chip on the board. It is recommended that the baseplate use SMHC0 to connect SD cards. SMHC2 recommends expanding other devices or not.

The I/O of the Allwinner T113-i processor can be configured with an on-chip pull-up resistor. These pull-up resistors can meet the pull-up needs of the SD card interface expansion, and the user design does not require an external pull-up resistor. The core board already has a 33 ohm matching resistor in series on the PF2_D2 clock signal, and the user design does not require an external series resistor. Expand the Micro SD card via the SMHC0 interface.

4.3.1. Layout recommendations

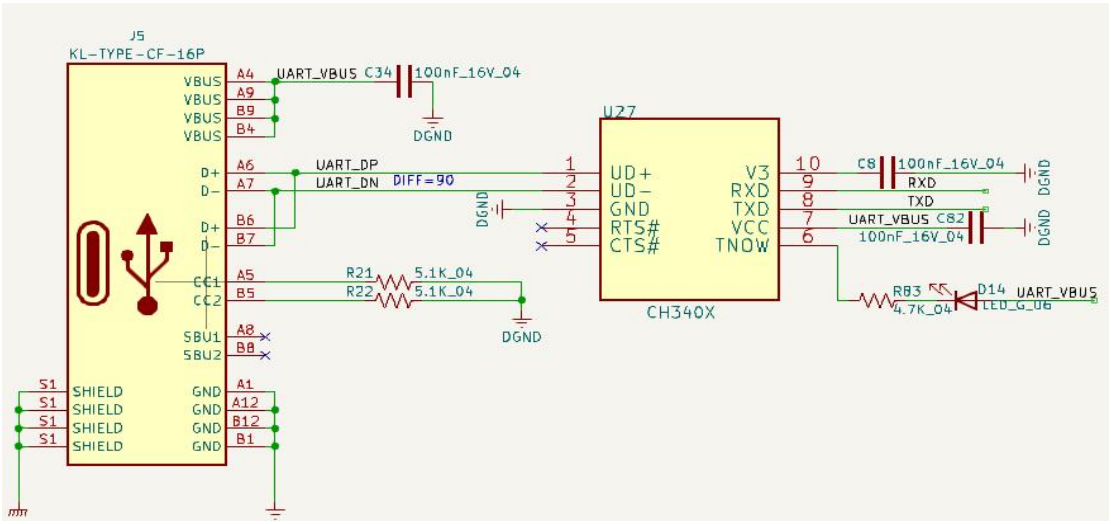
- The interface signal needs to be impeded control, and the single-ended impedance is 50Ω;

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- The SDIO signal line should be of equal length as much as possible, and the error should be less than ±20mil;
- If there is sufficient wiring space, the CLK signal is handled as much as possible. If this is not possible, distance the clock signal from other signals and follow the 3W rule.
- SDIO_CD_B pins are connected in series with 1K resistors for improved ESD performance.

4.4.Debugging the serial port design

4.4.1. USB to UART

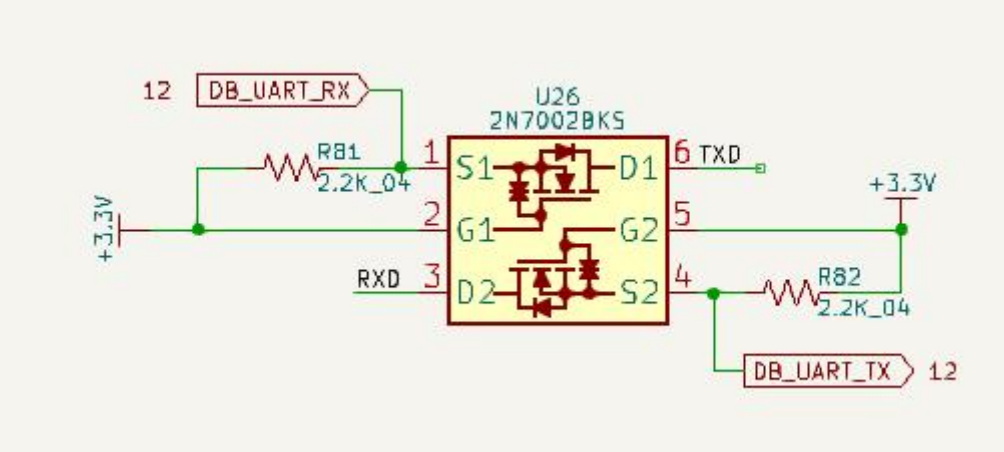


USB to UART reference circuit diagram

The ECK30-T13IA5ME8G-I core board defaults to UART0 as the debugging serial port, and the bottom board uses a CH340X conversion chip to convert the serial port into a USB interface, which is convenient for users to use. The power supply of the CH340X chip is provided by USB, and the power supply of the MCU is provided by the power supply on the board, so the current backfill problem needs to be considered when designing the circuit.

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4.4.2. Protection circuits



Reference circuit diagram for current backfill protection

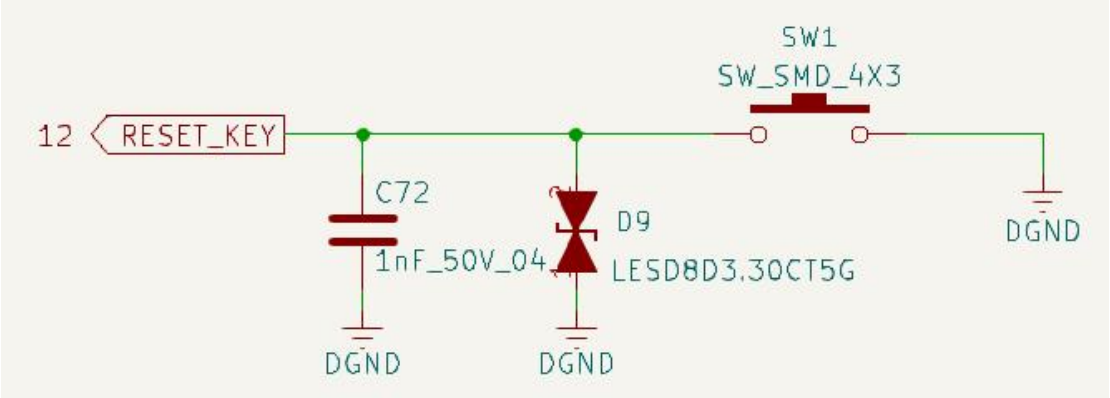
A 2N7002BKS dual NMOS transistor is used to prevent the CH340X chip from backing current into the MCU through the MCU's RXD or TXD's internal diodes when the dual power supply is running. The IO of the CH340X chip automatically prevents internal backfill, that is, when the CH340X has no power but the MCU has power, it will not generate backfill current.

4.4.3. Layout suggestion

- UART_DN/UART_DP signal takes the differential line, and the differential impedance is 90Ω, which ensures that the adjacent layers of the trace have a continuous and complete same reference plane;
- TVS is placed close to the TYPE-C interface.

Isolate the signals before and after, and ensure sufficient distance from the power plane.

4.5.Reset button

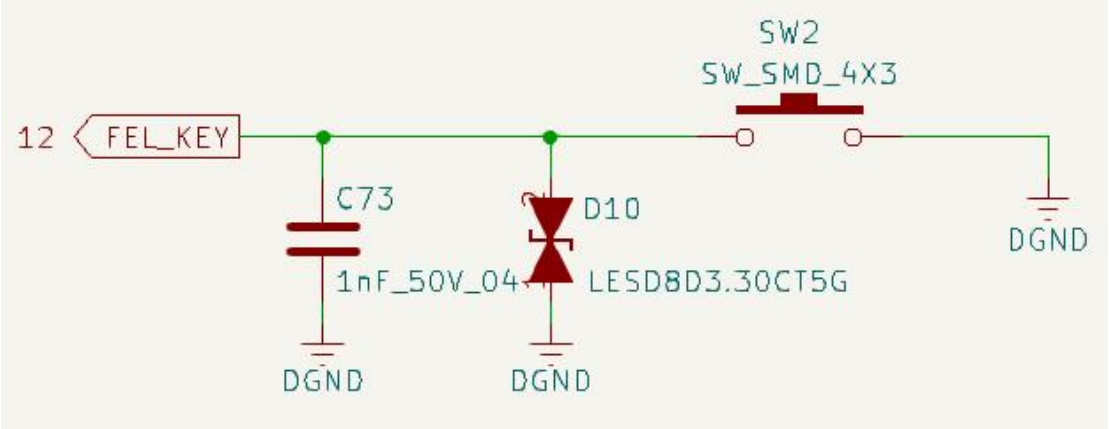


The reset button refers to the circuit diagram

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The RESET_M2 signal from the ECK30-T13IA5ME8G-I core board can be connected to an external button for reset control of the processor. The RESET_M2 signal is a bidirectional input and output signal, which can be used as an external reset input for resetting the processor and is also the output of the processor memory power reset signal. The RESET_M2 signal provides a 10K pull-up resistor within the core board. Therefore, when applying the RESET_M2 signal as a manual reset input on the baseplate, do not connect the pull-up resistor again, connect the button directly, or drive it through the OD gate. Do not drive the RESET_M2 signal through the push-pull output connector. When connecting manual input keys, small capacitors and TVS can be placed to reduce interference and improve ESD performance.

4.6.FEL button



FEL key reference circuit diagram

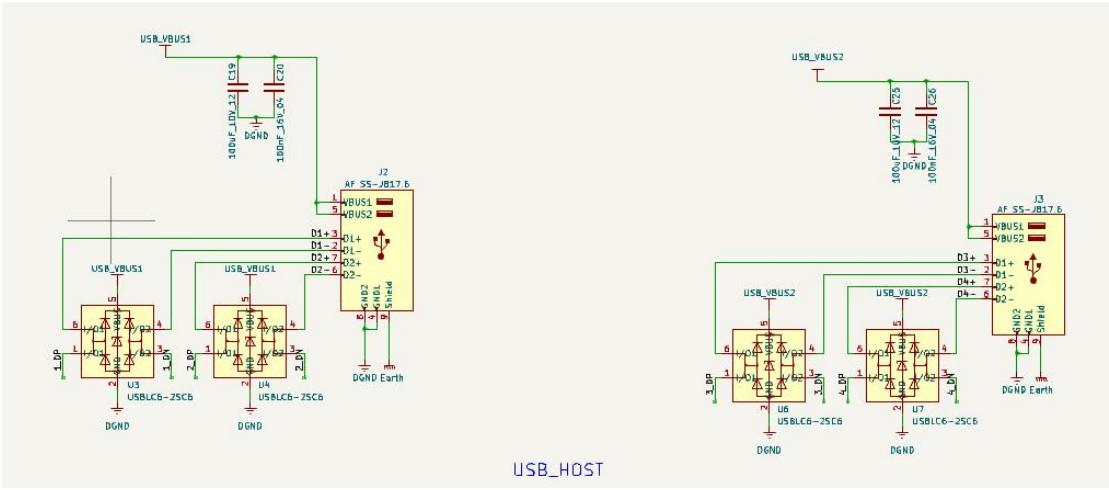
The FEL signal from the ECK30-T13IA5ME8G-I core board is used to connect external buttons to achieve forced firmware burning. When the core board is not powered on, connect the FEL signal to ground, and after powering on, release the FEL and the core board will enter firmware upgrade mode. Users can design buttons or jumpers on the backplane to connect the FEL signal to ground and force the processor into firmware upgrade mode. Since the signal has been designed with a pull-up resistor on the core board, the baseplate design can also consider grounding and appropriate TVS protection, and do not arbitrarily design a pull-up resistor for the FEL signal on the baseboard. If a FEL signal is not used, the signal can be processed in the air and then the firmware can be upgraded via the SD card.

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4.7. USB_HOST interface design

The ECK30-T13IA5ME8G-I core board supports 2 USB 2.0 interfaces. USB0 supports HOST and Device modes, while USB1 only supports HOST mode. USB1 is used on the SBC backplane to connect to the USB HUB chip to lead out 4 USB HOSTs.

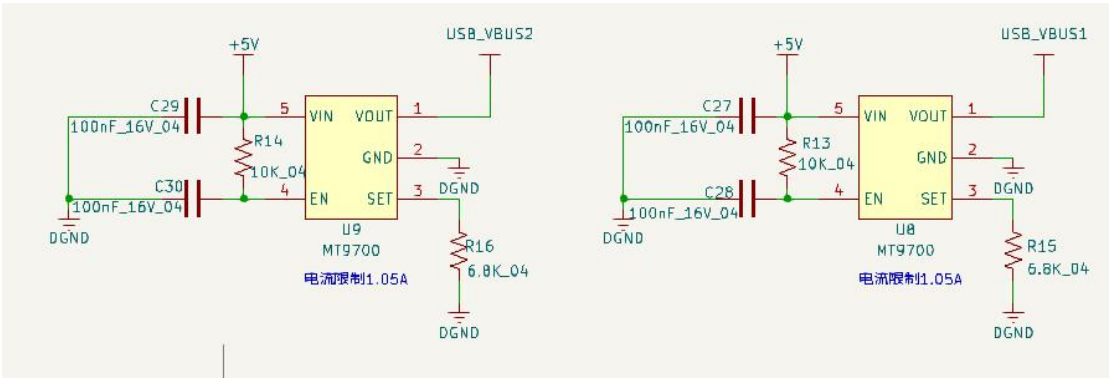
4.7.1. USB_HOST interface reference circuit



Refer to the USB interface circuit diagram

The SBC is designed with two sets of USB double-row female connectors, and the common mode inductor and TVS are placed on the USB signal line, and the TVS parasitic capacitance is recommended to be less than 2pF.

4.7.2. Power supply current limit reference circuit

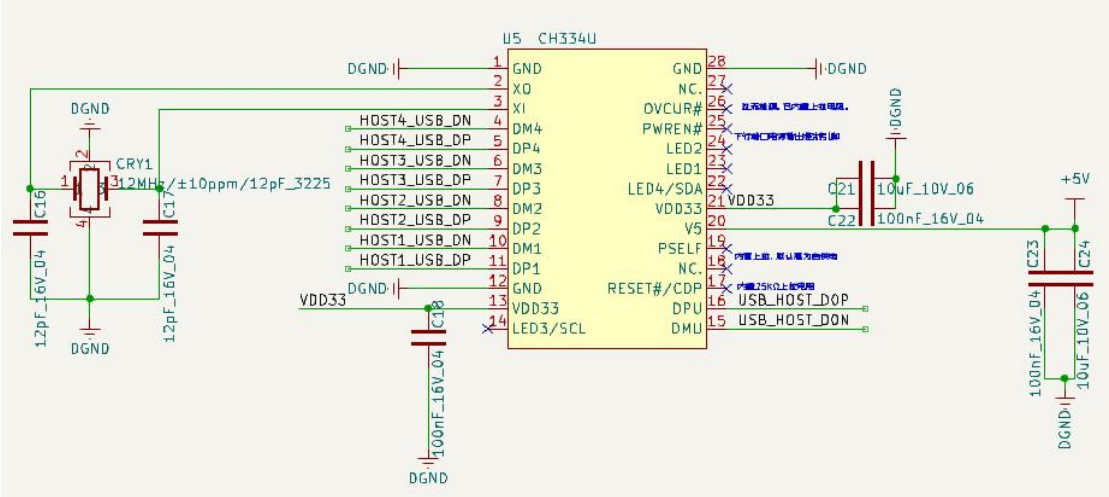


Refer to the USB power supply current limiting circuit diagram

The USB power supply voltage is 5.0V±10%, every two USB channels on the SBC backboard are connected to a power supply, the MT9700 is used to limit the current to 1.05A, and the SET pin of the MT9700 is the current limiting configuration pin, Iset=6.8k/Rset.

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4.7.3. USB HUB reference circuit



USB HUB reference circuit diagram

The USB hub adopts CH334U, the upstream port supports USB2.0 high-speed and full-speed, and the downlink port supports USB2.0 high-speed 480Mbps, full-speed 12Mbps and low-speed 1.5Mbps.

USB_HUB chip leads to 4 USB2.0 channels, all of which are open to users. The VDD33 pin has a built-in LDO circuit, which requires connecting the two VDD33 pins of the chip together and adding a 10uF and a 0.1uF capacitor to ground.

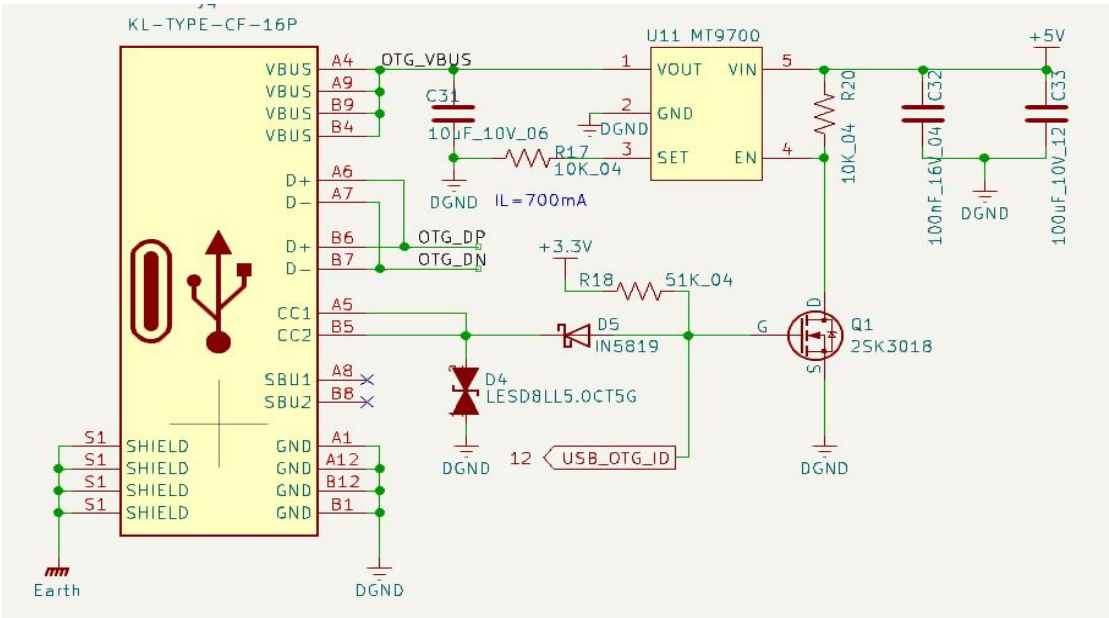
4.7.4. Layout suggestion

- USB_DP/USB_DN signal follows the differential line, and the differential impedance is 90Ω to ensure that the adjacent layers of the trace have a continuous and complete reference plane;
- USB_DP/USB_DN The distance between the signal line and other traces is greater than 10mil, try to avoid the trace under the device;
- USB_DP/USB_DN signal line routing should be as short as possible, the length should not exceed 4000mil, the corner angle of the routing should be greater than or equal to 135 degrees, and the routing vias should not exceed 2;
- USB_DP/USB_DN signal line should not be changed as much as possible, if the layer is changed, it is necessary to place GND reflux vias within 50mil from the layer change via;
- The TVS is placed close to the interface.

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4.8.USB_OTG interface design

4.8.1. OTG reference circuit



USB_OTG reference circuit diagram

The OTG backboard uses a Type-C interface, the CC pin is used as the detection pin, the pull-up resistor is 51K, and a diode needs to be added to the CC pin to prevent current backfill.

When both CC1 and CC2 are pulled down, the uplink port UFP is connected. When neither CC1 nor CC2 is pulled down, the downstream port DFP is connected.

When the USB Type-C interface is connected with the upstream port (UFP) as a downstream port (DFP), the CC pin detects a pulldown of the UFP, that is, the CC pin is pulled low, which indicates that the UFP device is connected and requests VBUS power.

OTG 供电电源用一颗 MT9700 芯片限流至 700mA。

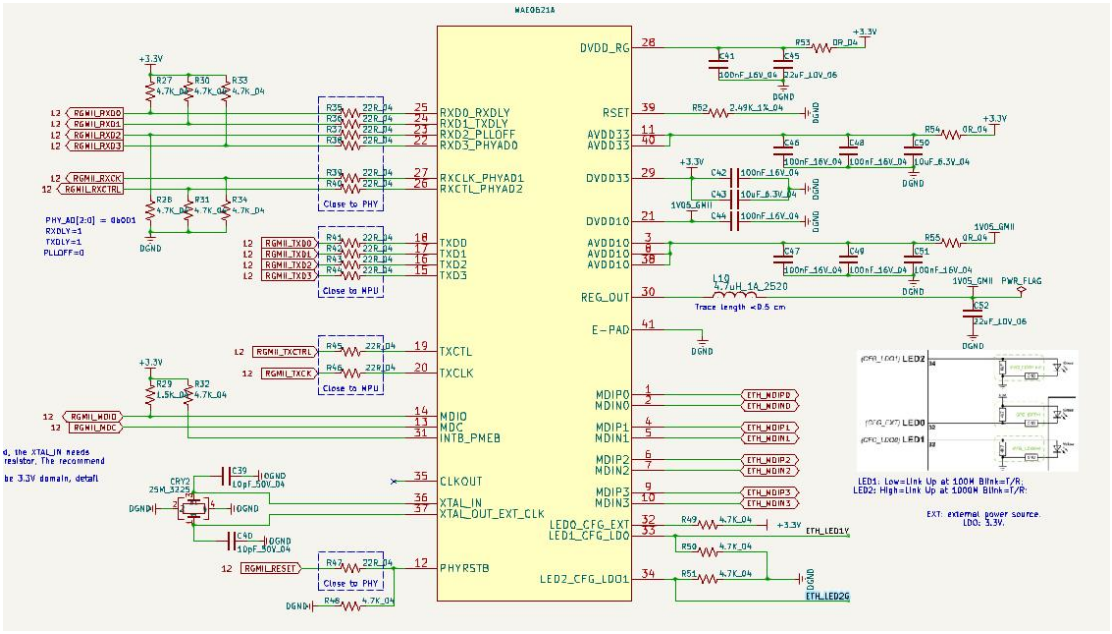
4.8.2. Layout suggestion

- OTG_DN/OTG_DP signal takes the differential line, and the differential impedance is 90Ω, which ensures that the adjacent layers of the trace have a continuous and complete reference plane;
- The VBUS power cable should be wide enough to ensure that enough current can be passed;
- The TVS is placed close to the interface.

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4.9.Network interface design

4.9.1. PHY reference circuit

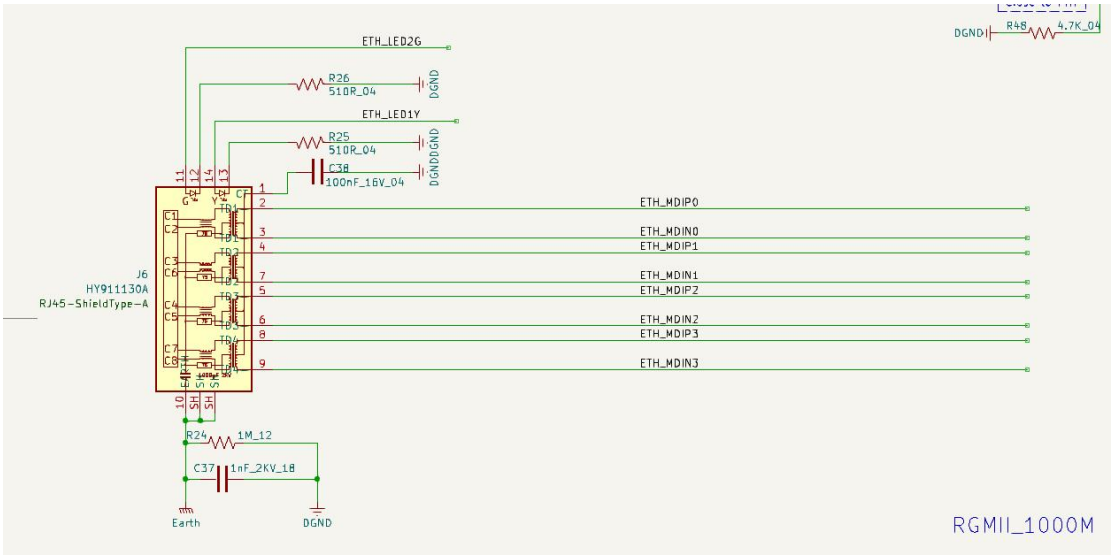


Network PHY circuit reference circuit diagram

The ECK30-T13IA5ME8G-I core board supports one channel 10M/100M/1000M adaptive Ethernet controller. The Ethernet controller supports RGMII and RMII interfaces. The MII interface on the core board is reused for PE/PG pins and only supports 3.3V level. There is no Ethernet PHY circuit in the core board, and users need to design PHY interface chip circuits on the backboard to use Ethernet functions. The default address of the PHY design on the backplane circuit is 001.

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4.9.2. RJ45 connector reference circuit

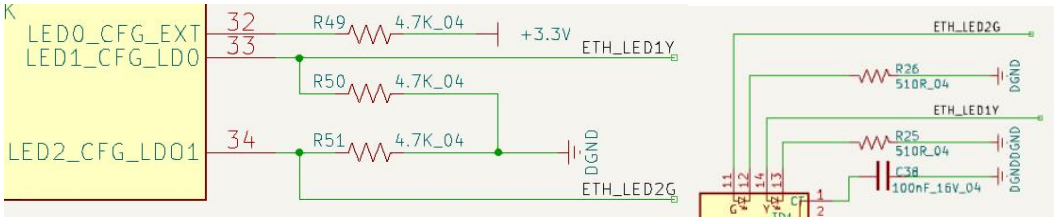


Refer to the circuit diagram for the RJ45 interface of the network

The backplane network port connector selects the RJ45 interface with its own transformer. Voltage-type PHY is adopted, and the middle tap of the transformer is connected in series with the capacitor to the ground.

4.9.3. RJ45 LED reference circuit

In addition to the LED indication function, the LED interface of the PHY chip also has the function of power-on configuration. The LED configuration and the principle of external indicators are shown in the following figure:



Refer to the circuit diagram for the network LED configuration and external indicators

The RJ45 LED indication is shown in the following table:

Direct connection to the LED status indicator

Connection status	LED status	Transmission status	LED status
10M connection	None of them are lit	10M transmission	None of them are lit
100M connection	The yellow LED is on	100M transmission	Yellow LED flashes
1000M connection	The green LED is on	1000M	The green LED flashes

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		transmission	

Since the LED interface is also used as a power-on configuration function when the LED interface is powered on, attention should be paid to the connection method of the external LED device when the LED interface is applied. One is to refer to the network LED configuration and the external indicator to refer to the circuit diagram, which can maintain the state of the pull-up and down resistor when powering up, and can also add a signal driving circuit, such as a Schmitt reverser, before connecting the LED.

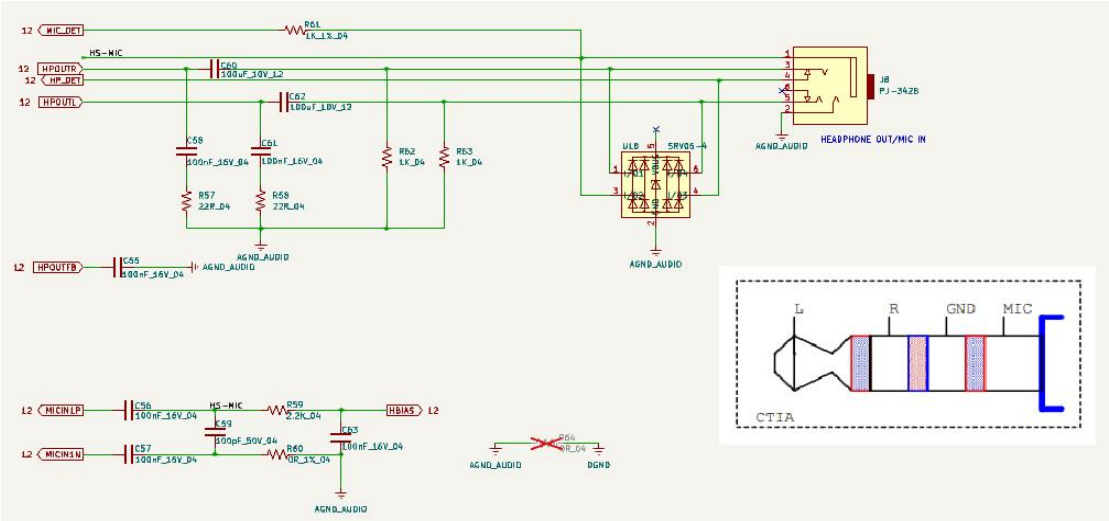
4.9.4. Layout suggestion

- Do not trace the wire and pour copper under the network port socket to prevent the interference on the ground from coupling to the transformer or wiring to affect the signal quality;
- RGMII differential pairs need to be controlled at equal spacing, with an equal length error of ± 10mil and a differential impedance of 100Ω ±10%;
- The length of the signal trace from PHY to the transformer end should not exceed 12cm, and the punching and layer transformation should be avoided as much as possible;
- The RESET resistor of 2.49K should be placed close to the PHY, at a distance of no more than 0.5cm, and should be as far away from other signal lines as possible to avoid unnecessary interference;
- The 22 ohm matching resistor on the RX data line and the clock line is placed close to the PHY, the TX data line and the 22Ω matching resistor on the clock line are placed close to the MCU, and the matching capacitor on the RGMII_RESET line is placed close to the PHY.
- The TVS is placed near the network port seat.

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4.10.Audio interface design

4.10.1. Audio interface reference circuit



Schematic diagram of the AUDIO circuit

The ECK30-T13IA5ME8G-I core board supports up to 2 digital audio interfaces (PCM/I2S), and an I2S signal is drawn from the bottom board to the audio codec chip, and the headset and microphone functions are realized through the audio codec chip.

The audio interface uses 4 3.5mm audio jacks, including headphone and microphone functions, with headset and microphone detection.

4.10.2. Layout suggestion

- MICIN1N/MICIN1P signal lines are routed according to differential lines;

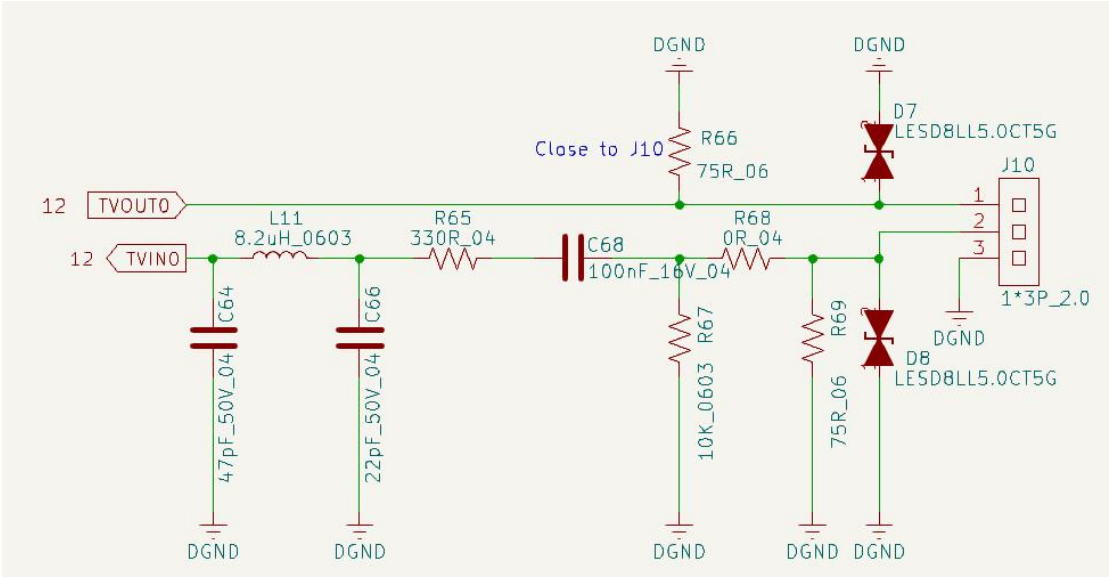
The layout of the audio circuit is far away from the interference source, and it is recommended to plan a separate area on the PCB for placing the analog circuit;

- This design belongs to analog audio signals, and 10mil and above are recommended.
- Digitally and analogue ground at a single point.

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4.11. Analog video interface

4.11.1. Analog video interface reference circuit



Schematic diagram of an analog video circuit

The ECK30-T13IA5ME8G-I core board has 2 dedicated pins LINEOUT and HPOUT for analog audio output interfaces. Lead these two signals to the pins with a spacing of 1 * 3P 2.0mm on the baseplate. The signal port plus TVS prevents static interference.

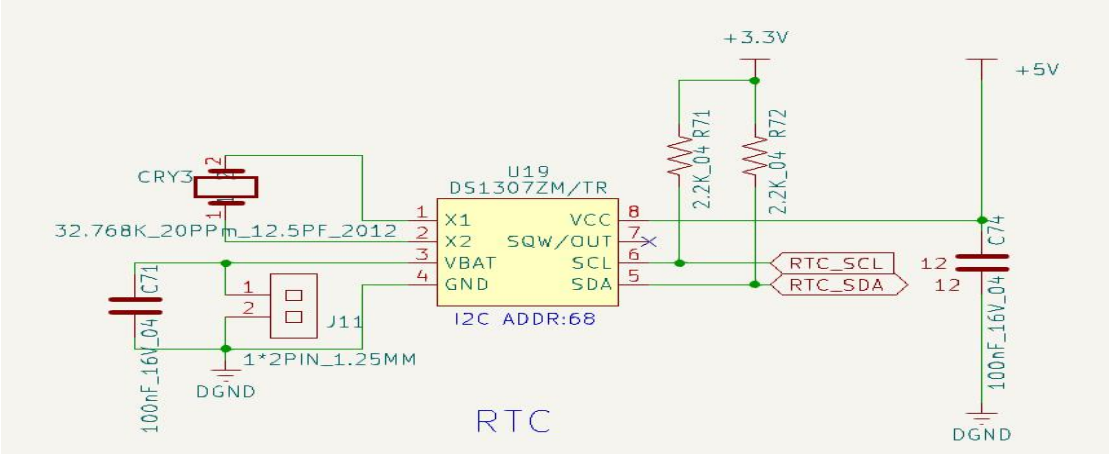
4.11.2. Layout suggestion

- The video signal line should be routed according to the 37.5Ω impedance, and the corner of the cable should not be less than 135 degrees;
- The 75Ω resistor is placed close to the connector.

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4.12.RTC battery interface

4.12.1. RTC clock circuit reference circuit



Schematic diagram of the RTC clock circuit

There is no RTC on the ECK30-T13IA5ME8G-I core board that uses backup battery power. The bottom plate adopts a separate RTC chip, the chip has automatic power-down detection and power switching circuit, the main power supply is powered by +5V power supply, the backup power supply is powered by +3V battery, the battery voltage must be maintained at 2.0V to 3.5V to work normally, and the battery is recommended to use CR2032.

The chip is connected to a 32.768K crystal oscillator with a 12.5pF load capacitor.

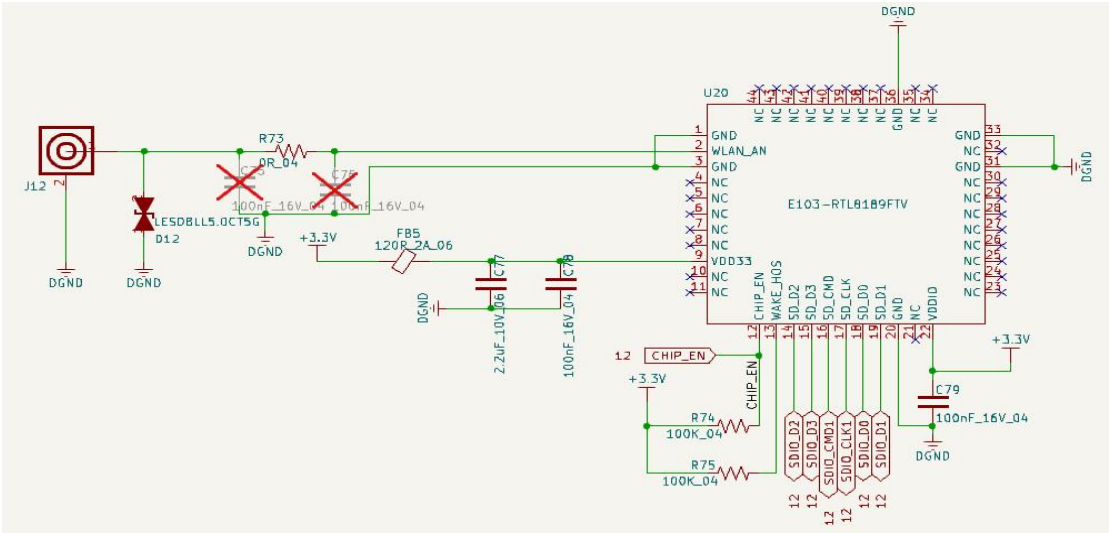
4.12.2. Layout suggestion

- The crystal oscillator is placed close to the RTC chip.

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4.13.WIFI interface design

4.13.1. WIFI interface reference circuit



Schematic diagram of WIFI circuit

The SMHC1 derived from the ECK30-T13IA5ME8G-I core board conforms to the Secure Digital I/O v3.0 protocol and is usually used to connect extended functions, such as WiFi modules. The design adopts the self-developed WIFI module RTL8189FTV-VC-CG, which conforms to the IEEE 802.11b/g/n standard, the maximum data rate can reach 150Mbps, and the communication interface is SDIO 2.0. For details, refer to "E103-RTL8189FTV_UserManual_CN_v1".

The module uses 3.3V power supply. The VDDIO pin is also connected to a 3.3V voltage, ensuring that the voltage of the IO port of the module is 3.3V, and the corresponding IO port of the MCU is in the same power domain. SDC1 is used as the data and clock transmission line for WIFI signals. The module is connected to the enable pin CHIP_EN, and the 100K resistor is pulled up to 3.3V, and the module can be turned off when the level is low to reduce energy consumption. The antenna interface is prone to electrostatic interference, so add a TVS.

4.13.2. Layout recommendations

- The RF trace needs to be calculated to meet the impedance of 50Ω design;
- The RF cable should be as short and wide as possible to reduce energy loss, and the recommended length is less than 6cm;
- RF traces need to have a complete copper pour in the adjacent layer or compartment as a reference ground, it is recommended to use the partition reference, which can ensure that

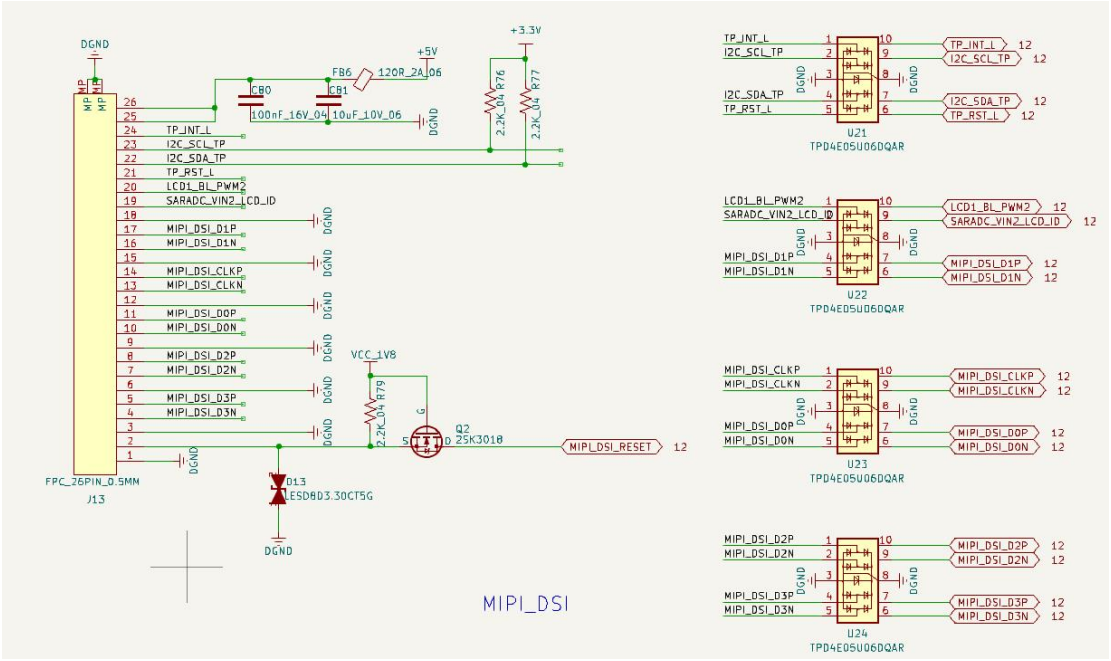
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the trace is wider and reduces loss;

- The distance between the RF trace and the edge of the board is greater than 3cm;
- The RF cable can not be bifurcated and replaced, and the corners are arc-shaped;
- The SCS-G1B coplanar waveguide model is recommended, which is more flexible, and the characteristic impedance can be accurately controlled by adjusting the signal line width, ground wire spacing, and medium thickness.
- The RF trace reflow path is complete, avoiding the span division of the reflow path, and ensuring that the ground of the trace is completely returned to the bottom of the module;
- Perforation around the ground plane of the RF trace, the via spacing is 0.5mm ≤ W ≤ 1mm;
- The SDIO signal line is controlled with equal length, which meets the impedance of 50Ω design, and the length error is controlled within 20mil;
- The TVS is placed close to the antenna.

4.14.MIPI display interface design

4.14.1. MIPI interface reference circuit



Schematic diagram of the MIPI interface circuit

The ECK30-T13IA5ME8G-I core board supports RGB888 (RGB666), dual-channel LVDS (multiplexed pins with RGB interface), MIPI DSI (multiplexed pins with RGB interface), and SPI

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(DBI) display interfaces. The base plate leads the 4-lane MIPI DSI to the 26P-0.5mm lower clamshell FPC connector as the display interface. Display resolution 1920x1080@60fps is supported.

The screen uses 5V as the power supply, and the power supply side is connected in series with magnetic beads to reduce interference, and it is recommended to use the power domain controlled by the MCU as the power supply of the display, so as not to work normally due to power supply timing problems. Add an NMOS transistor and a 2.2K resistor to the signal line MIPI_DSI_RESET as a level shifting circuit to avoid the failure to work normally due to the different levels of the display and MCU terminals. Because the MIPI interface is susceptible to electrostatic interference, TVS is added to all signal lines.

Pay attention to the pin sequence, it is recommended to compare the pin sequence of the FPC connector on the display side before designing, and the pin design of the FPC connector at both ends needs to be vertically mirrored to correctly correspond.

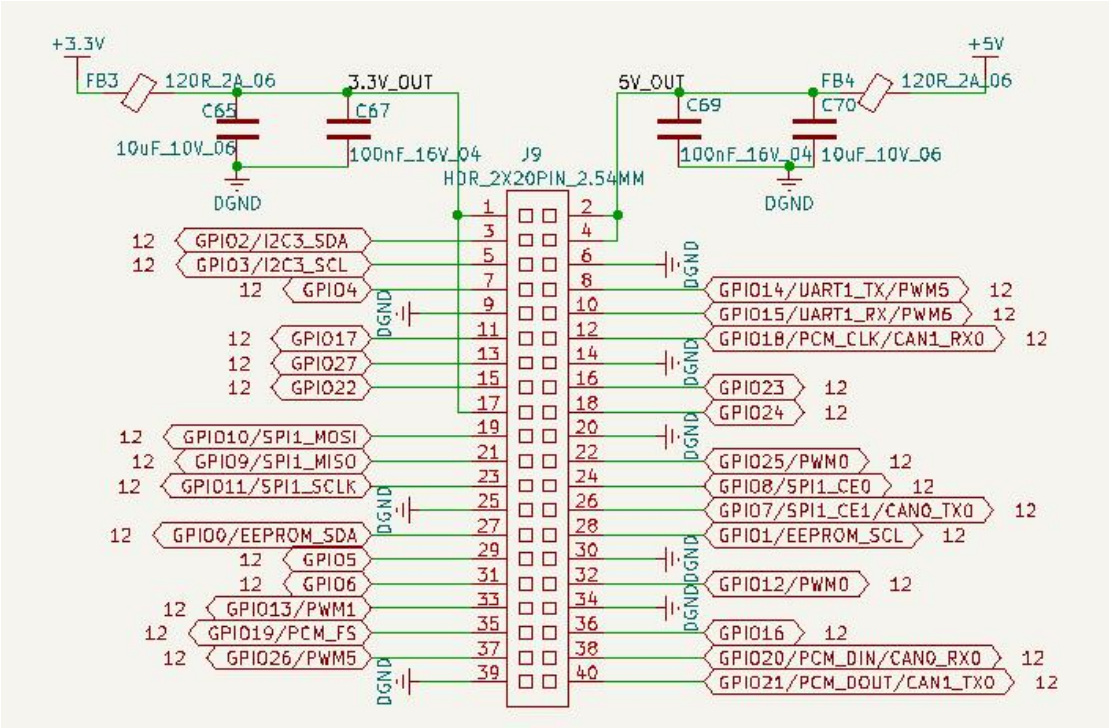
4.14.2. Layout recommendations

- The differential signal needs to meet the 100Ω impedance design, and the equal length of the group is controlled within 5 mil, and the differential pair is controlled within 25 mil.
- Differential signals should be in the same group and layer, and should have a complete power reference plane, and should not be split across sections.
- The TVS is placed close to the interface.

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4.15.Raspberry Pi interface design

4.15.1. Raspberry Pi interface reference circuit



Raspberry Pi 2*20 interface circuit diagram

The ECB30-P4T13IA5ME8G-I SBC is designed with 1 x 2*20 and 2.54mm spacing double row pins, which adopts the interface of standard Raspberry Pi line sequence, and can be reused with 2 channels of CAN, 1 channel I2C, 6 channels of PWM, 1 channel of PCM, etc.

4.15.2. Layout recommendations

- Do not place the double row of needles too close to the edge of the board, leaving a suitable spacing.
- 1. The silk screen print needs to be clearly marked, and pay attention to foolproof.

5. Software Resources

ECB30-P4T13IA5ME8G-I is equipped with an operating system based on the Linux 5.4 kernel, which comes with the cross-compilation toolchain Buildroot source code, U-boot source code, Linux kernel and the source code of each driver module required for embedded Linux system development, as well as various development and debugging tools for Windows desktop environment and Linux desktop environment.

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Operating system:

Linux file system built by Buildroot

System source code:

Submarine 2018

Kernel 5.4

BuildRoot 2019.02

openwrt

Development Environment and Tools:

USB 烧录工具：PhoenixSuit

SD Card Burning Tool: PhoenixCard

The system software resources are shown in the following table:

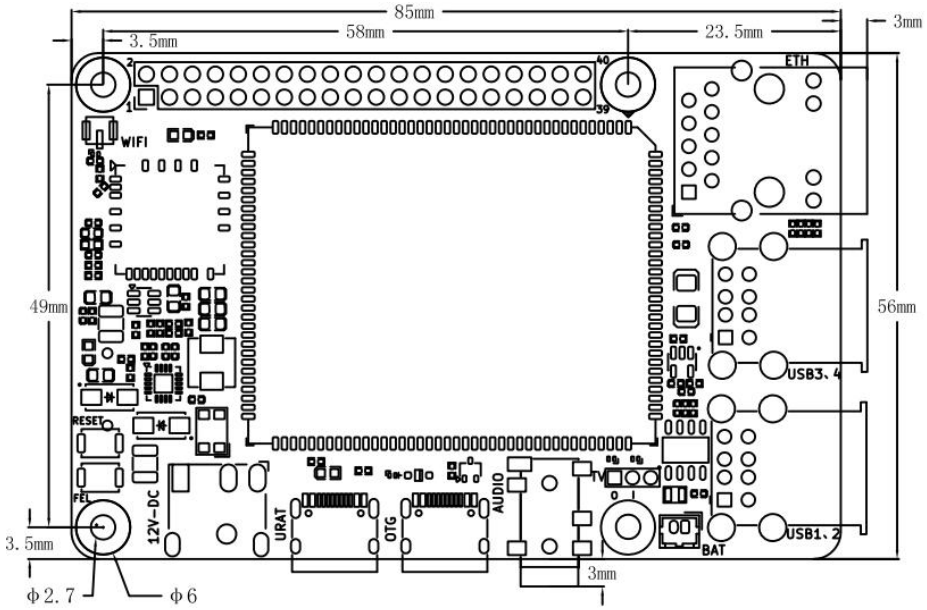
System Software Resource Table

category	name	description	source
SPL	spl-pub	Boot0, boot uboot	<SDK>/brandy/brandy-2.0/spl-pub/
BOOT	de-boot 2018.07	Bootloader	<SDK>/brandy/brandy-2.0/u-boot-2018/
Kernel	Kernel 5.4.61	Linux kernel	<SDK>/kernel/linux-5.4/
Device Driver	Audio	Built-in audio driver	sound/soc/sunxi_v2/*
	AWlink	CAN driven	drivers/net/can/sunxi_awlink.c
	GMAC	Built-in MAC driver	drivers/net/ethernet/allwinner/sunxi-gmac.c
	GPADC	GPADC driver	drivers/input/sensor/sunxi_gpadc.c
	GPIO	GPIO driver	drivers/pinctrl/sunxi
	LCD	Disp2 displays the driver	drivers/video/fbdev/sunxi/disp2/disp/lcd/
	LRADC	Button module driver	drivers/input/keyboard/sunxi-keyboard.c
	SMHC	MMC drive	drivers/mmc/host/sunxi-mmc.c
	SPI	SPI driver	drivers/spi/spi-sunxi.c
	SPI-NAND	SPI-NAND 驱动	drivers/mtd/awnand/spinand
	TVD	CVBS input	drivers/media/platform/sunxi-tvd/
	TVE	CVBS output	drivers/video/fbdev/sunxi/disp2/tv/
	TWI	I2C drive	drivers/i2c/busses/i2c-sunxi.c
	UART	Serial port drive	drivers/tty/serial/sunxi-uart.c
	WINE	CSI driver	drivers/media/platform/sunxi-vin/
operating system	Buildroot 201902	201902 版本 Buildroot	<SDK>/buildroot/buildroot-201902
	Buildroot 202205	202205 版本 Buildroot	<SDK>/buildroot/buildroot-202205
	openwrt	openwrt	<SDK>openwrt/openwrt
Development tools	PhoenixSuit	USB Burning Tool	/tools/PhoenixSuit
	PhoenixCard	SD card flashing tool	/tools/PhoenixCard

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6. Structural dimensions

Unit mm；Error ±0.1mm。



Dimension drawing of the front structure of the single-board computer

7. Refer to the documentation

- T113-i_V1.9.pdf
- E103-RTL8189FTV_UserManual_CN_v1.0.pdf
- ECK30-T13IA5ME8G-I 核心板产品手册.pdf

8. Revision Notes

Revision Explanation Table

version	Modifications	Modify time	weave	proofread	Approval
V1.0	first draft	24-10-21	LJQ	WFX	WFX
V1.1	Modify the extended interface definition	25-11-05	LJQ	WFX	WFX

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