Product Manual
ECB20-PG6Y28C-I Test Board



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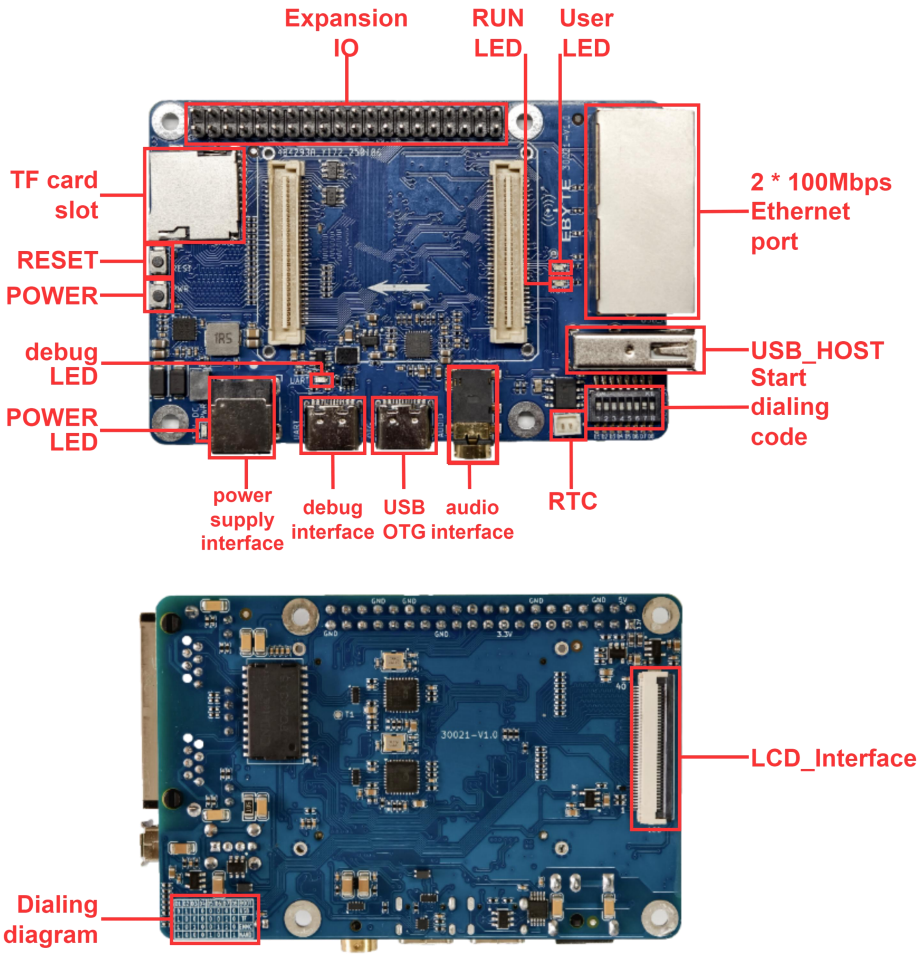
1. Product Overview

1.1.Product Introduction

Ebyte introduces the ECB20-PG6Y28C-I test baseboard, which is designed to be combined with the ECK20-6Y28C series core board via a BTB (Board-to-Board) connector. The test baseboard features a rich set of peripheral interfaces and is engineered for industrial-grade reliability, surpassing the design specifications of standard development boards.

Ebyte provides stable reference designs and a comprehensive software development environment to assist users in validating core board functionalities, streamlining development processes, reducing time-to-market cycles, enhancing design quality, and accelerating product R&D and commercialization.

Functional diagram of the test baseboard is shown below:



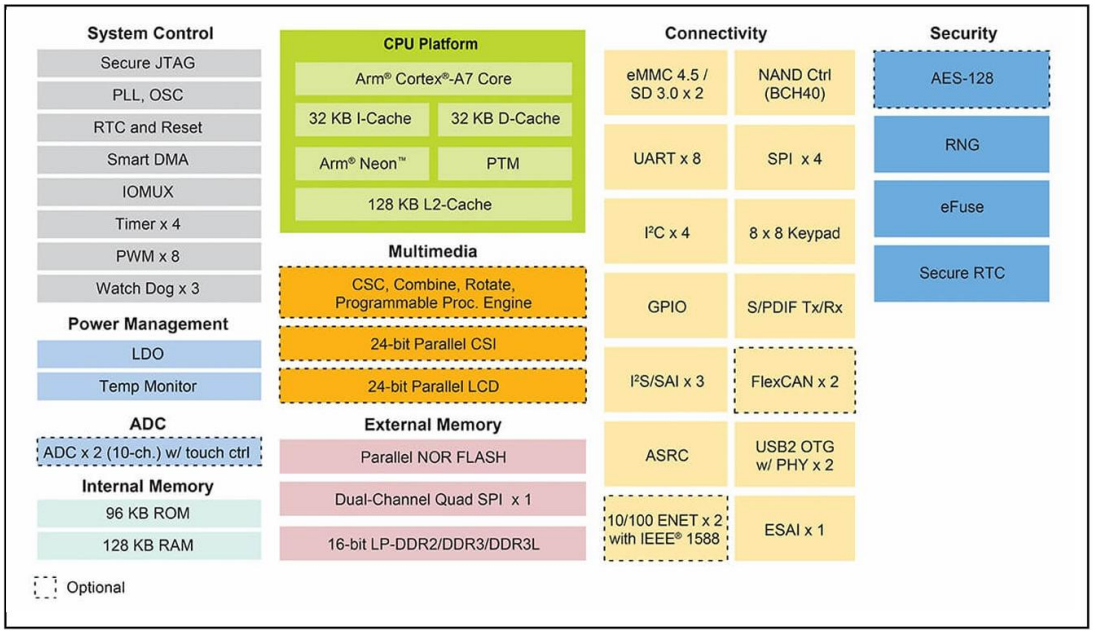
Test backplane functional description diagram

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1.2. i.MX6ULL Chip Introduction

The i.MX6ULL processor is an industrial-grade Cortex-A7-based processor from NXP, with a maximum main frequency of up to 792MHz. It provides 1 x LCD display, 1 x digital camera, 2 x 100Mbps Ethernet, 2 x USB OTG, 8 x UART, 2 x SDIO, 2 x CAN, and multiple GPIO (General-Purpose Input/Output) pins, along with rich I/O resources to support connections to numerous peripheral devices.

The functional block diagram of the i.MX6ULL processor is shown in the following figure:



i.MX6ULL Processor System Functional Block Diagram

1.3.ECK20-6Y28C Series Core Board Introduction

The Ebyte ECK20-6Y28C series core boards are industrial-grade, low-power, cost-effective embedded core boards carefully designed based on the i.MX6ULL processor, featuring a BTB (Board-to-Board) connector with 120-pin pins. The core board integrates the processor, 256/512MB DDR3L (optional), 512MB NAND/8GB eMMC (optional), power management modules, and measures 46x36x6.8mm. It is widely applicable in industrial control, HMI, IoT, and other fields.

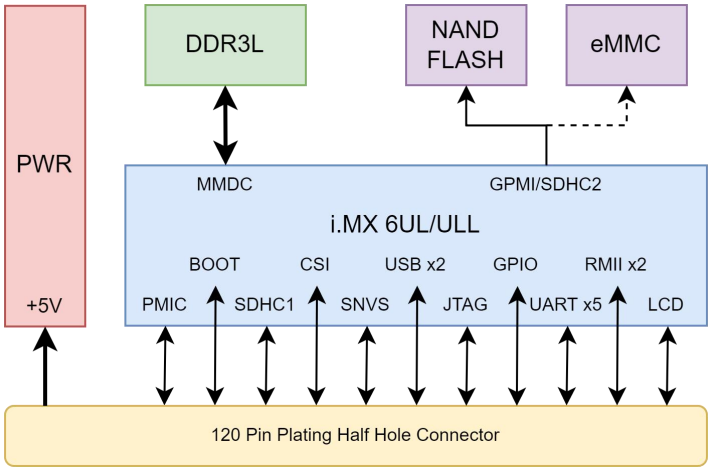
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The front view of the ECK20-6Y28C series core board is shown below (no components on the bottom side of the products):



ECK20-6Y28C Series Core Board Front View

ECK20-6Y28C Series Core Board Functional Block Diagram:



ECK20-6Y28C Series Core Board Functional Block Diagram

1.4.Typical Applications

- Industrial control mainboard;
- Automotive electronics;
- Industrial all-in-one machine;
- Smart city;
- Tablet PC;
- IoT gateway;
- Advertising all-in-one machine;
- Robot.

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2. Specification Parameters

2.1.Functional Parameters

ECB20-PG6Y28C-I Test Baseboard Functional Parameter Table

Power Input	1 × DC socket, 12V 1A input;
Display	1 × 40Pin FPC RGBBB display interface, supports maximum resolution WXGA (1366×768@60fps), with touchscreen and backlight adjustment;
CSI	1 × CSI camera interface (reusable for camera expansion);
USB HOST	1 × USB2.0 HOST;
USB OTG	1 × USBOTG, Type-C interface;
Ethernet Port	2 × 10/100M adaptive RJ45 ports;
TF	1 × TF card slot with insertion detection;
Audio	1 × 3.5mm audio interface, supports headphone output and microphone input.
BOOT	1 × 8-bit boot mode dip switch;
Debug	1 × UART debug serial port, Type-C interface;
UART	3 × multiplexed UART communication interfaces, extended interface output;
CAN	2 × multiplexed CAN interfaces, TTL level, extended interface output;
SPI	3 × multiplexed SPI interfaces, extended interface output;
GPIO	28 × multiplexed GPIO pins, extended interface output;
I2C	1 × I2C interface, extended interface output;
Keypad	1 × reset button; 1 × power button;
Indicators	1 × power indicator LED; 1 × run indicator LED; 1 × user indicator LED; 1 × debug indicator LED;
Watchdog	Supports on-chip watchdog timer function;
RTC	1 × 1.25mm RTC battery holder;
Power Output	2 × 5V @ 1A power outputs, extended interface output; 2 × 3.3V @ 1A power outputs, extended interface output;

2.2.Environmental Characteristics

ECB20-PG6Y28C-I Test Board Environmental Characteristics Table

Operating Temperature	Industrial grade: -40°C ~ 85°C (in a well-ventilated thermal environment);
Storage Temperature	-40°C ~ 85°C;
Operating Humidity	5% ~ 95% humidity, non-condensing;

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Storage Humidity	60°C @ 95% humidity, non-condensing;

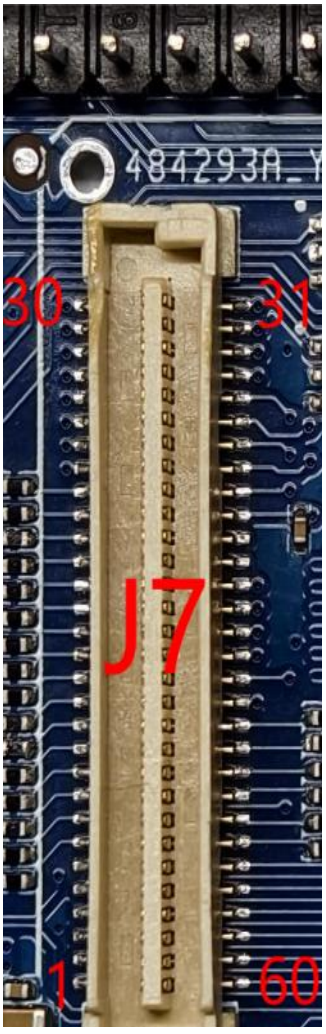
3. Interface Definitions

3.1.Core Board Pin Definitions

The ECK20-6Y28C series core board features a BTB connector that carries 120 signal and power pins, providing abundant peripheral resources. The BTB connector J1 on the core board corresponds to the J7 connector on the base board, while the J2 connector on the core board corresponds to the J10 connector on the base board. For detailed pin definitions, please refer to the 《ECK20-6Y28C_Pin_List_V1.0.xlsx.》 The I/O pin assignments for the BTB interface on the base board are defined as follows:

BTB J7 Pin Definition Table

Pin Name	Pin
LCD_DATA23	J7_30
LCD_DATA22	J7_29
LCD_DATA21	J7_28
LCD_DATA20	J7_27
LCD_DATA19	J7_26
LCD_DATA18	J7_25
LCD_DATA17	J7_24
LCD_DATA16	J7_23
LCD_DATA15	J7_22
LCD_DATA14	J7_21
LCD_DATA13	J7_20
LCD_DATA12	J7_19
LCD_DATA11	J7_18
LCD_DATA10	J7_17
LCD_DATA09	J7_16
LCD_DATA08	J7_15
LCD_DATA07	J7_14
LCD_DATA06	J7_13
LCD_DATA05	J7_12
LCD_DATA04	J7_11
LCD_DATA03	J7_10
LCD_DATA02	J7_9
LCD_DATA01	J7_8



Pin	Pin Name
J7_31	ENET2_TX_CLK
J7_32	ENET2_TX_EN
J7_33	ENET2_RX_EN
J7_34	ENET2_RX_ER
J7_35	ENET2_TX_DATA1
J7_36	ENET2_TX_DATA0
J7_37	ENET2_RX_DATA1
J7_38	ENET2_RX_DATA0
J7_39	SNVS_TAMPER6
J7_40	RESETN
J7_41	PWR_ON_EN
J7_42	VBAT
J7_43	LCD_VSYNC
J7_44	LCD_HSYNC
J7_45	LCD_CLK
J7_46	LCD_ENABLE
J7_47	GPIO1_IO05
J7_48	SNVS_TAMPER9
J7_49	SD1_DATA0
J7_50	SD1_DATA1
J7_51	SD1_DATA3
J7_52	SD1_DATA2
J7_53	SD1_CMD

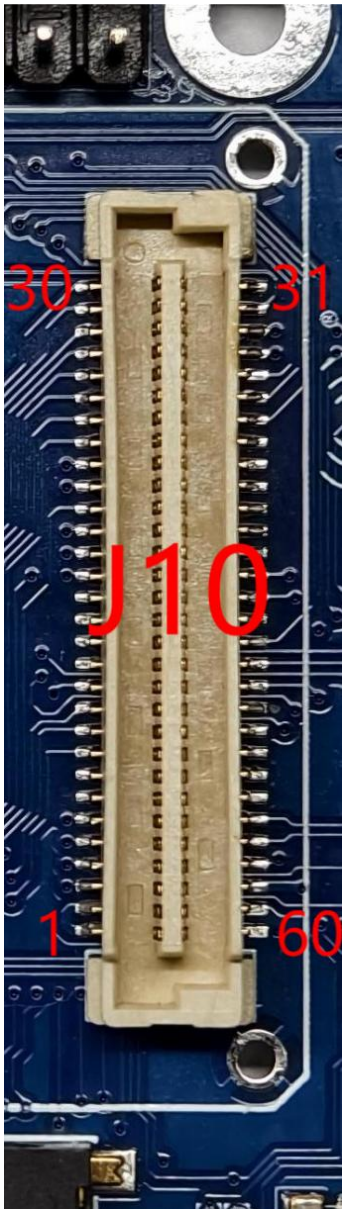
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LCD_DATA00	J7_7
CSI_DATA05	J7_6
CSI_PIXCLK	J7_5
CSI_DATA06	J7_4
CSI_DATA02	J7_3
CSI_MCLK	J7_2
CSI_HSYNC	J7_1

J7_54	SD1_CLK
J7_55	CSI_DATA04
J7_56	CSI_DATA00
J7_57	CSI_DATA01
J7_58	CSI_DATA07
J7_59	CSI_DATA03
J7_60	CSI_VSYNC

BTB J10 Pin Definition Table

Pin Name	Pin
ENET1_RX_ER	J10_30
ENET1_TX_CLK	J10_29
ENET1_TX_DATA1	J10_28
ENET1_TX_EN	J10_27
ENET1_RX_DATA0	J10_26
ENET1_RX_EN	J10_25
ENET1_RX_DATA1	J10_24
ENET1_TX_DATA0	J10_23
JTAG_MOD	J10_22
JTAG_TRST_B	J10_21
JTAG_TMS	J10_20
JTAG_TCK	J10_19
JTAG_TDO	J10_18
JTAG_TDI	J10_17
GPIO1_IO08	J10_16
GPIO1_IO09	J10_15
GPIO1_IO04	J10_14
GPIO1_IO02	J10_13
SNVS_TAMPER2	J10_12
SNVS_TAMPER5	J10_11
SNVS_TAMPER7	J10_10
SNVS_TAMPER8	J10_9
BOOT_MODE1	J10_8
BOOT_MODE0	J10_7
SNVS_TAMPER0	J10_6
SNVS_TAMPER1	J10_5
PWRBTN	J10_4
SNVS_TAMPER4	J10_3
VIN_5V	J10_2
VIN_5V	J10_1



Pin	Pin Name
J10_31	UART5_TX_DATA
J10_32	UART5_RX_DATA
J10_33	UART4_TX_DATA
J10_34	UART4_RX_DATA
J10_35	UART3_RTS_B
J10_36	UART3_CTS_B
J10_37	UART3_RX_DATA
J10_38	UART3_TX_DATA
J10_39	UART2_CTS_B
J10_40	UART2_RTS_B
J10_41	UART2_RX_DATA
J10_42	UART2_TX_DATA
J10_43	UART1_RTS_B
J10_44	GPIO1_IO06
J10_45	GPIO1_IO07
J10_46	UART1_RX_DATA
J10_47	GPIO1_IO03
J10_48	UART1_CTS_B
J10_49	GPIO1_IO01
J10_50	UART1_TX_DATA
J10_51	GPIO1_IO00
J10_52	USB_OTG1_CHD_B
J10_53	USB_OTG1_DN
J10_54	USB_OTG1_DP
J10_55	USB_OTG2_DN
J10_56	USB_OTG2_DP
J10_57	USB_OTG1_VBUS
J10_58	USB_OTG2_VBUS
J10_59	DGND
J10_60	DGND

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3.2.Expansion Interface Pin Definition

The ECB20-PG6Y28C-I test baseboard is designed with a 2.54mm pitch expansion interface compatible with Raspberry Pi, and the pin definitions are as follows:

Expansion Interface Pin Definition Table

Function	Pin Number		Pin number	Function
3.3V_OUT	1		2	5V_OUT
UART5_RX_DATA I2C2_SDA	3		4	5V_OUT
UART5_TX_DATA I2C2_SCL	5		6	DGND
GPIO1_IO5	7		8	UART3_TX_DATA
DGND	9		10	UART3_RX_DATA
GPIO5_IO0_SNVS	11		12	CSI_VSYNC PWM7
GPIO5_IO4_SNVS	13		14	DGND
GPIO5_IO1_SNVS	15		16	UART3_CTS_B CAN1_TX
3.3V_OUT	17		18	UART3_RTS_B CAN1_RX
UART2_CTS_B ECSPI3_MOSI CAN2_TX	19		20	DGND
UART2_RTS_B ECSPI3_MISO CAN2_RX	21		22	GPIO1_IO03
UART2_RX_DATA ECSPI3_SCLK	23		24	UART2_TX_DATA ECSPI3_SS0
DGND	25		26	GPIO1_IO01
CSI_DATA6 ECSPI1_MOSI	27		28	CSI_MCLK
CSI_DATA7 ECSPI1_MISO	29		30	DGND
CSI_DATA4 ECSPI1_SCLK	31		32	CSI_HSYNC PWM8
CSI_DATA2 ECSPI2_MOSI	33		34	DGND
CSI_DATA3 ECSPI2_MISO	35		36	CSI_PIXCLK
CSI_DATA0 ECSPI2_SCLK	37		38	CSI_DATA1 ECSPI2_SS0

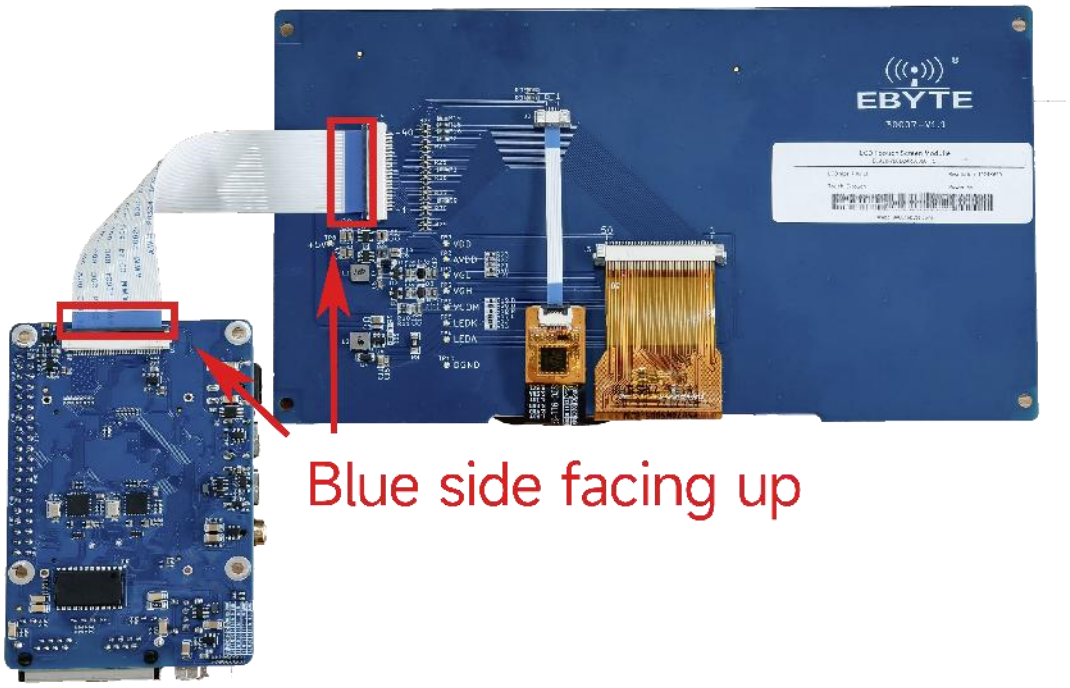
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DGND	39

40	CSI_DATA5 ECSPI1_SS0

3.3.LCD Interface Definition

The ECB20-PG6Y28C-I test board provides 1 RGB888 video output channel, supporting display resolution of 1366×768 at 60 fps. The interface features a 40-pin flip-up FPC socket with 0.5 mm pin pitch. It can be connected to Ebyte's ECA10-7LCD24R1006CT-C touchscreen module for operation. Note that the HDMI port and touchscreen module cannot be used simultaneously. The touchscreen wiring diagram is illustrated in the following figure：



Touchscreen Wiring Diagram

Attention：The silk-screen markings are inversely aligned with the interface package. In the schematic diagram, pin 1 of this package corresponds to silk-screen marking 40. When wiring, ensure both ends of the flat cable have the blue side facing up.

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LCD Interface Pin Definition Table



Pin number	Function	Level	Type
1	5V_IN	5V	PWR_I
2	5V_IN	5V	PWR_I
3	LCD_DATA16	3.3V	DO
4	LCD_DATA17	3.3V	DO
5	LCD_DATA18	3.3V	DO
6	LCD_DATA19	3.3V	DO
7	LCD_DATA20	3.3V	DO
8	LCD_DATA21	3.3V	DO
9	LCD_DATA22	3.3V	DO
10	LCD_DATA23	3.3V	DO
11	DGND	GND	PWR
12	LCD_DATA8	3.3V	DO
13	LCD_DATA9	3.3V	DO
14	LCD_DATA10	3.3V	DO
15	LCD_DATA11	3.3V	DO
16	LCD_DATA12	3.3V	DO
17	LCD_DATA13	3.3V	DO
18	LCD_DATA14	3.3V	DO
19	LCD_DATA15	3.3V	DO
20	DGND	GND	PWR
21	LCD_DATA0	3.3V	DO
22	LCD_DATA1	3.3V	DO
23	LCD_DATA2	3.3V	DO
24	LCD_DATA3	3.3V	DO
25	LCD_DATA4	3.3V	DO
26	LCD_DATA5	3.3V	DO
27	LCD_DATA6	3.3V	DO
28	LCD_DATA7	3.3V	DO
29	DGND	GND	PWR
30	LCD_CLK	3.3V	DO
31	LCD_HSYNC	3.3V	DO
32	LCD_VSYNC	3.3V	DO
33	LCD_ENABLE	3.3V	DO
34	LCD_BL_PWM	3.3V	DO
35	LCD_NRST	3.3V	DO

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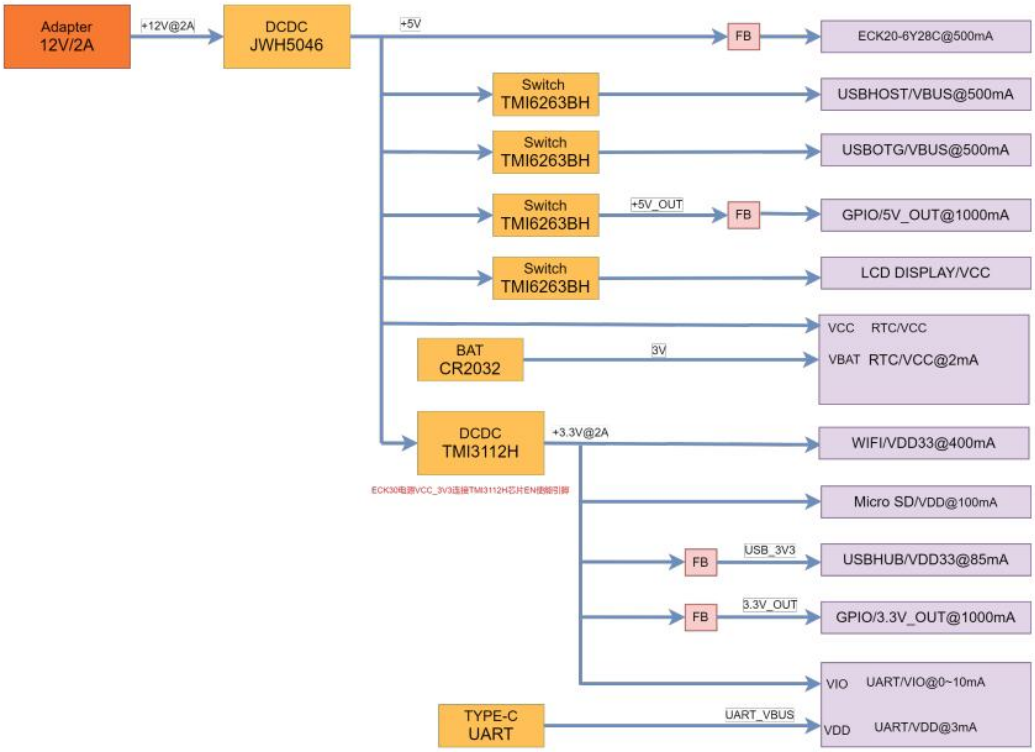
36	I2C2_SDA	3.3V	DO
37	NC	-	-
38	I2C2_SCL	3.3V	DO
39	TP_INT	3.3V	DI
40	TP_NRST	3.3V	DO

4. Circuit Design

4.1.Power Supply

4.1.1.Power Tree

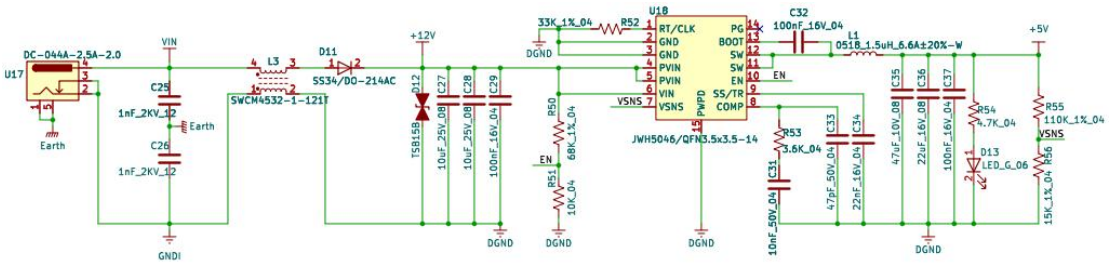
The Test Backplane Power Tree Block Diagram is shown below:



Test Board Power Tree Schematic

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4.1.2. 12V to 5V DC-DC Converter Reference Circuit

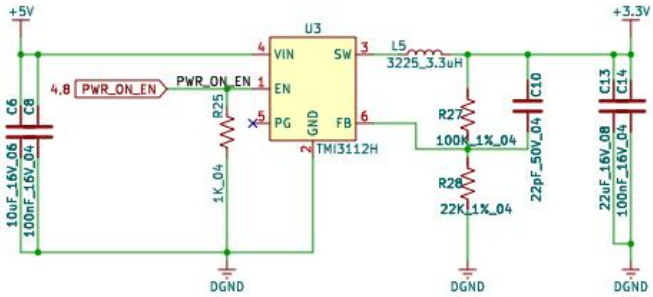


12V to 5V Power Reference Circuit Diagram

The core board requires a 5V voltage supply for normal operation, with full-load power consumption approaching 0.5W. Due to high inrush current during power-up and potential derated performance under high-temperature conditions, insufficient power supply power margin may prevent system boot-up. Therefore, sufficient power margin must be reserved in power design to ensure system stability and reliability.

If a DC-DC converter is used for core board 供电, excessive power margin in the power design may force the converter to operate in discontinuous PWM mode to maintain efficiency, significantly increasing output ripple, which adversely affects digital signal system stability. If an LDO is employed, its power loss and thermal rise must be carefully considered to avoid overheating shutdown or failure in high-temperature environments with poor heat dissipation.

4.1.3. 5V to 3.3V DC-DC Converter Reference Circuit



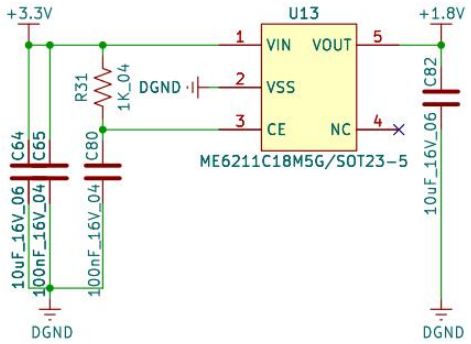
5V to 3.3V Power Reference Circuit Diagram

The test board employs a DC-DC converter chip to step down 5V to 3.3V, with a designed load capability of 2A. To address the power-up sequencing requirements of the

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downstream interface circuits, the 3.3V power domain is controlled by the MCU. The converter's EN pin is connected to the core board's PWR_ON_EN pin, ensuring that this chip operates only after the core board's NVCC power domain is enabled.

4.1.4. 4.1.4. 3.3V to 1.8V LDO Reference Circuit



3.3V to 1.8V Power Reference Circuit Diagram

The test board incorporates a 3.3V-to-1.8V LDO power supply designed to power the analog section of the ES8316 audio codec chip. The 1.8V power supply timing remains synchronized with the 3.3V supply.

4.1.5. Layout Recommendations

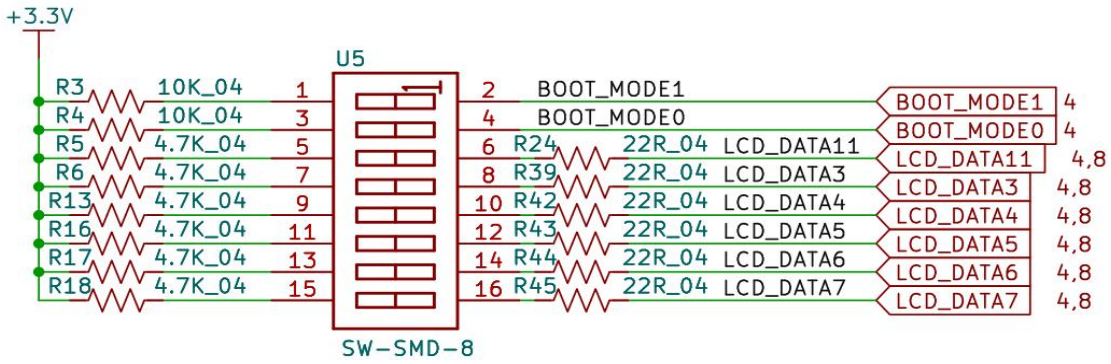
- The minimum distance between different power planes must be at least 20 mils;
- Power and ground traces should be widened as much as possible to meet the required current ratings, while feedback signal traces should not be excessively narrow (a width of 10 mils or more is recommended);
- Signal traces should avoid routing directly below inductors;
- Current loop paths should be minimized, and inductors/capacitors should be placed close to their respective ICs;
- Output capacitors should prioritize low ESR (Equivalent Series Resistance) specifications;
- DC-DC converters, inductors, capacitors, and other key components are recommended to be placed on the top layer for easier debugging, while minimizing via

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usage to reduce parasitic effects and electromagnetic interference;

- Input capacitors should be positioned adjacent to the DC-DC input pins to ensure input currents pass through filtering capacitors before entering the chip;
- Feedback voltage sampling points should be taken immediately after the output capacitor (adjacent to the capacitor);

4.2.BOOT



Boot Mode Configuration Schematic

The i.MX6ULL processor first executes the program stored in its internal Boot ROM upon startup. The Boot ROM determines the boot mode and boot device based on the status of the BOOT_MODE register, eFUSEs, and configuration pins.

The value of the BOOT_MODE register is determined by the voltage levels of the BOOT_MODE0 and BOOT_MODE1 pins during the initial power-up phase, which dictates the boot mode as shown in the following table:

BOOT_MODE Boot Mode Configuration Table

BOOT_MODE [1:0]	**Boot Mode**	Boot Mode Description
00	Boot From Fuses	The boot information is read from internal Fuses. It is recommended to use this method for mass production shipments.
01	Serial Downloader	The device supports downloading programs to Flash via the USB_OTG1 port. It is important to note that in this mode, UART1 and UART2 have higher priority than USB_OTG. If UART1 or UART2 detect incoming data while in this mode, the programmer will be unable to perform USB-based flash programming, and the computer will fail to detect the device.
10	Internal Boot	The boot configuration is read from the Boot Mode pin. This mode is recommended for development purposes and can also be used for mass production.

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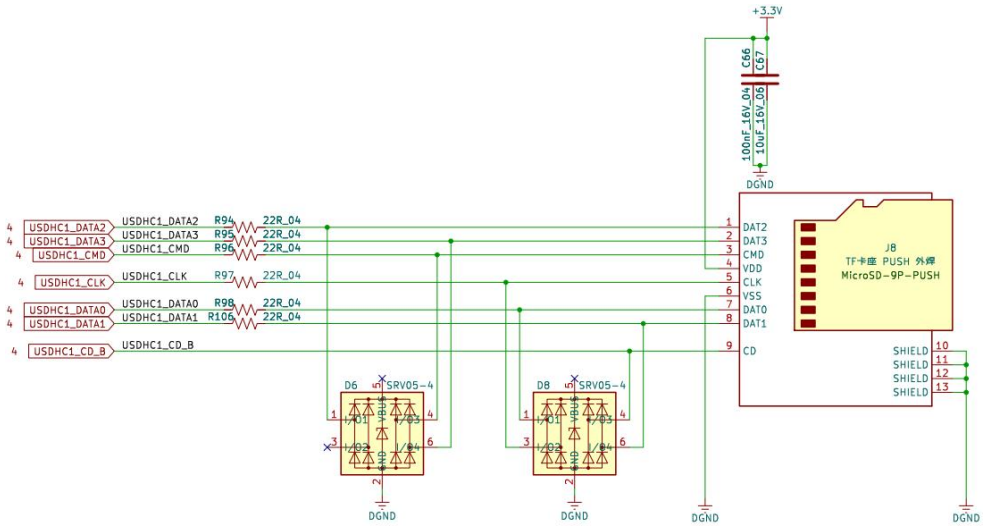
11	Reserved	Retention Mode

The Boot Mode is typically set to Internal Boot Mode. In this mode, the CPU reads the voltage levels of LCD_DATA0-DATA23 pins during power-on reset to determine which device to boot from. The ECK20-6Y2XA series core board has internal pull-down resistors implemented for LCD_DATA0-DATA23 pins. Baseboard designers only need to configure individual pins when designing the baseboard. The reference circuit for baseboard Boot device selection configuration is shown in the following table.

SW								
D1	D2	D3	D4	D5	D6	D7	D8	BOOT DEVICE
OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	USB
ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	MicroSD
ON	OFF	ON	OFF	OFF	ON	ON	OFF	EMMC
ON	OFF	OFF	OFF	ON	OFF	OFF	ON	NAND

BOOT Mode Configuration Table

4.3.TF Interface Design



TF Interface Reference Schematic Diagram

The USDHC1 signal provided by the core board is connected to the TF card socket for TF card booting or storage expansion. The processor's I/O can be configured with on-chip pull-up resistors. These internal pull-up resistors meet the pull-up requirements for SD card

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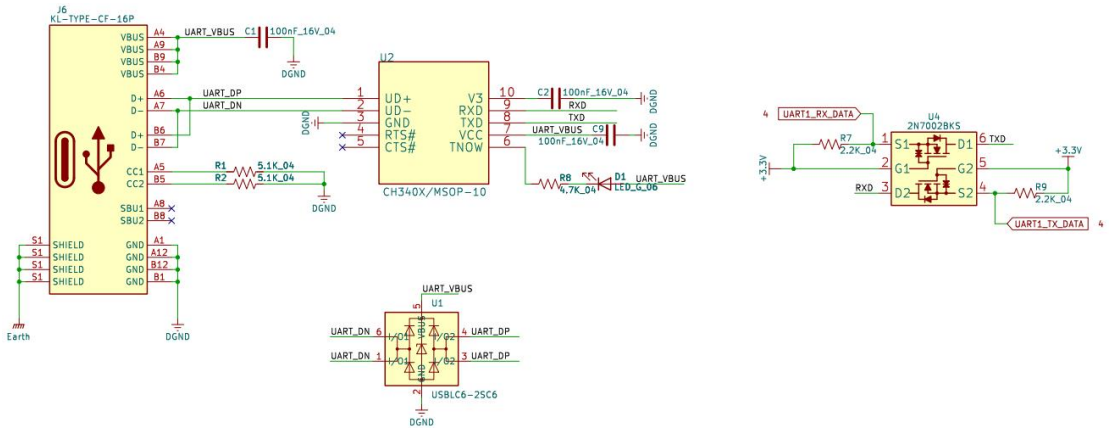
interface expansion, eliminating the need for external pull-up resistors in user designs. Additionally, the core board already includes a 10Ω series termination resistor on the USDHC clock signal, so no external series resistors are required in user implementations.

4.3.1. Layout Recommendations

- The interface signals require impedance control, with a single-ended impedance of 50Ω.;
- SDIO signal lines should be kept as equal as possible, with an error margin of less than ±20 mils;
- If sufficient layout space is available, the CLK signal should ideally be shielded by ground. If not possible, maintain a minimum distance between the clock signal and other signals in accordance with the 3W rule;
- The SDIO_CD_B pin should have a 1K resistor connected in series to enhance its ESD protection performance;

4.4. Debugging Serial Port Design

4.4.1. Debugging UART Reference Circuit



UART Schematic Diagram

The test board defaults to UART1 as the debugging serial port, utilizing a Type-C interface. Users can perform debugging by simply connecting a USB Type-C cable.

The CH340X chip is used to convert USB signals into debugging serial port signals. The

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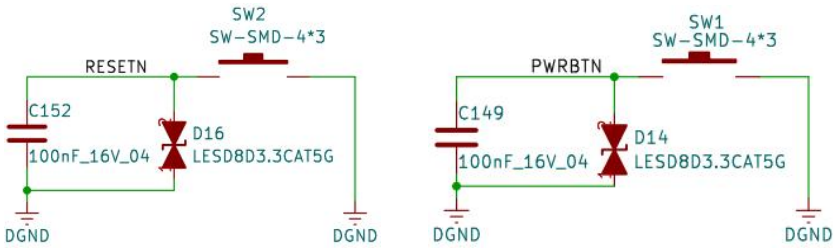
CH340X chip is powered by the 5V voltage supplied through the external Type-C cable.

When designing the circuit, current backflow must be considered. A 2N7002BKS dual NMOS transistor is used to prevent the PC from causing current backflow into the MCU through the internal diodes of the RXD or TXD pins in a dual-power supply mode.

4.4.2. Layout Recommendations

- Place the TVS near the TYPE-C interface;
- isolate the input and output signals, and ensure sufficient distance between power planes;

4.5. Reset and Power Buttons



Reset and Power Buttons Reference Circuit Diagram

The baseboard design includes a reset button and a power button, with the reset button connected to the RESETN signal of the core board.

The power button is connected to the PWRBTN signal of the core board.

The RESETN signal on the core board incorporates a debounce circuit and pull-up resistor. The PWRBTN signal is connected to the processor's ON/OFF pin, which also features an internal pull-up resistor. Since both signals already have pull-up resistors on the core board, no additional pull-up resistors should be added in the baseboard application - simply connect the buttons directly or use an OD gate driver.

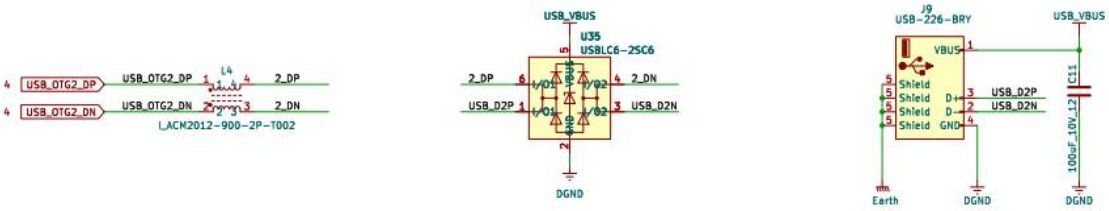
Attention: Do not arbitrarily pull up the reset and power button signals through resistors. Improper pull-up of the power rail may cause indeterminate signal inputs to the button signal interface during system standby or shutdown. For example, some baseboards pull up the PWRBTN signal to the NVCC_3.3V power supply. When the system is powered off, the NVCC_3.3V power supply is also disabled, causing its voltage to drop to 0V. This effectively pulls the PWRBTN signal down to ground (equivalent to pressing the PWRBTN key), re-triggering system boot and ultimately preventing normal software shutdown.

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4.6.USB_HOST Interface Design

The ECK20-6Y28C series core board supports two USB 2.0 ports. USB0 supports HOST and DEVICE modes, while USB1 supports only HOST mode. On the test baseboard, USB1 is used to connect the USB interface and provide one USB HOST port.

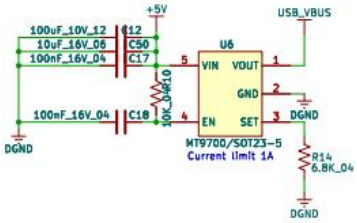
4.6.1.USB_HOST Interface Reference Circuit



USB Interface Reference Circuit Diagram

The ECB20-PG6Y28C-I test baseboard is designed with two USB 2.0 interfaces. Common-mode inductors and TVS devices are placed on the USB signal lines, with the recommendation that the TVS's parasitic capacitance be less than 2pF.

4.6.2.Power Current Limiting Reference Circuit



USB Power Current Limiting Reference Circuit Diagram

The USB single-channel power supply voltage is 5.0V ±10%. The test baseboard uses the USB_VBUS power supply. To accommodate high initial currents when USB devices are connected, the MT9700 chip is employed to limit the current to 1.05A. The MT9700's SET pin is a limiting configuration pin, with Iset = 6.8k / Rest.

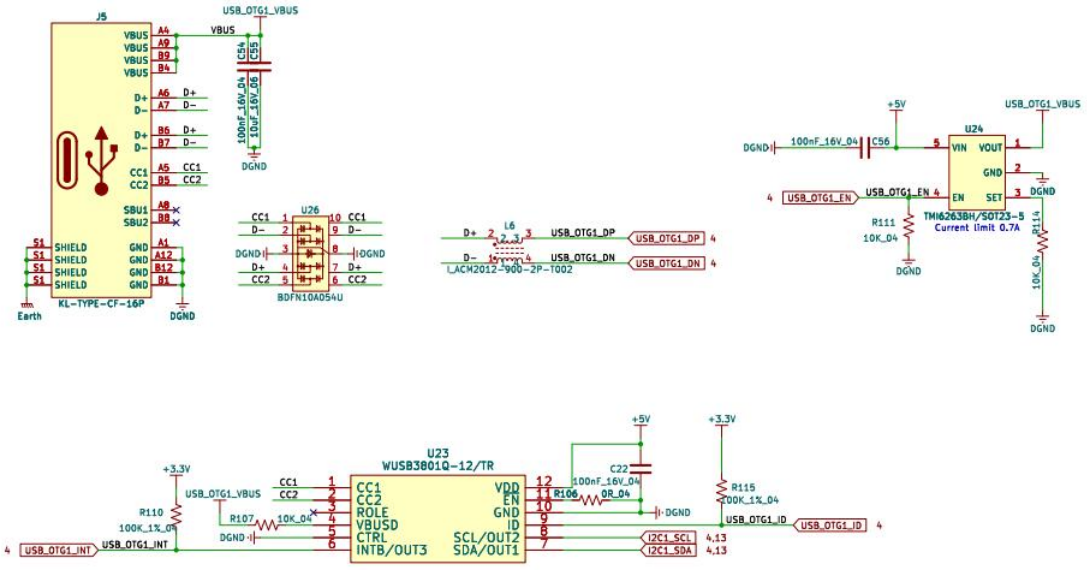
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4.6.3. Layout Recommendations

- USB_DP/USB_DN signals shall be routed as differential traces with a differential impedance of 90Ω, ensuring that adjacent layers maintain continuous and complete co-planar reference planes;
- USB_DP/USB_DN signal traces shall maintain a minimum spacing of 10 mils from other traces and avoid routing under components whenever possible;
- USB_DP/USB_DN signal traces should be as short as possible, with maximum length not exceeding 4000 mils, trace corner angles ⩾135°, and no more than 2 vias per trace segment;
- USB_DP/USB_DN signal traces should avoid layer transitions whenever possible. If layer transitions are required, ground return vias must be placed within 50 mils of the layer transition vias;
- TVS should be placed close to the interface.

4.7. USB_OTG Interface Design

4.7.1. OTG Reference Circuit



USB_OTG Reference Circuit Diagram

The system employs the WUSB3801Q-12 OTG identification chip to detect whether an

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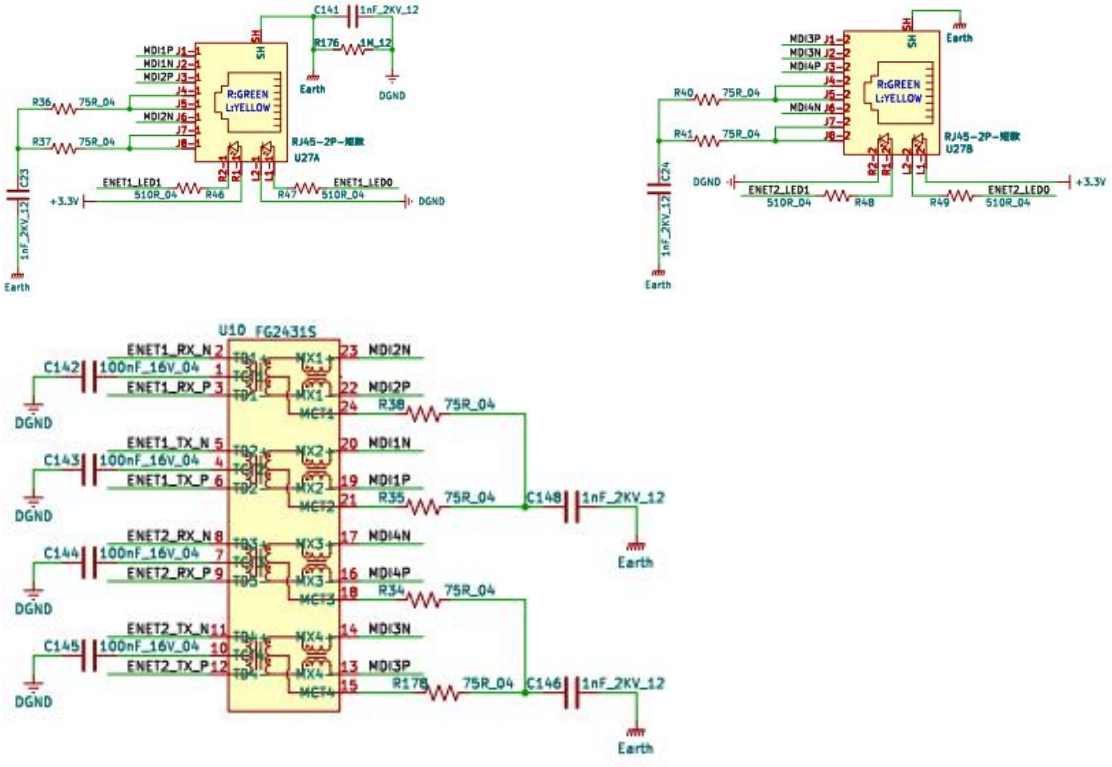
externally connected device operates in Device or Host mode. When a device is connected in Device mode, the USB current-limiting chip TMI6263BH is enabled to supply power externally. Simultaneously, the USB current-limiting chip will restrict the current to 700mA.

4.7.2. Layout Recommendations

- OTG_DN/OTG_DP signals shall be routed as differential traces with a differential impedance of 90Ω, ensuring that adjacent layers maintain continuous and complete co-planar reference planes;
- The VBUS power trace should be sufficiently wide to ensure adequate current capacity;
- TVS should be placed close to the interface;

4.8. Network Interface Design

4.8.1. RJ45 Connector Reference Circuit



Network RJ45 Interface Reference Circuit Diagram

The baseboard is designed with two 100Mbps RJ45 interfaces. A voltage-type PHY is

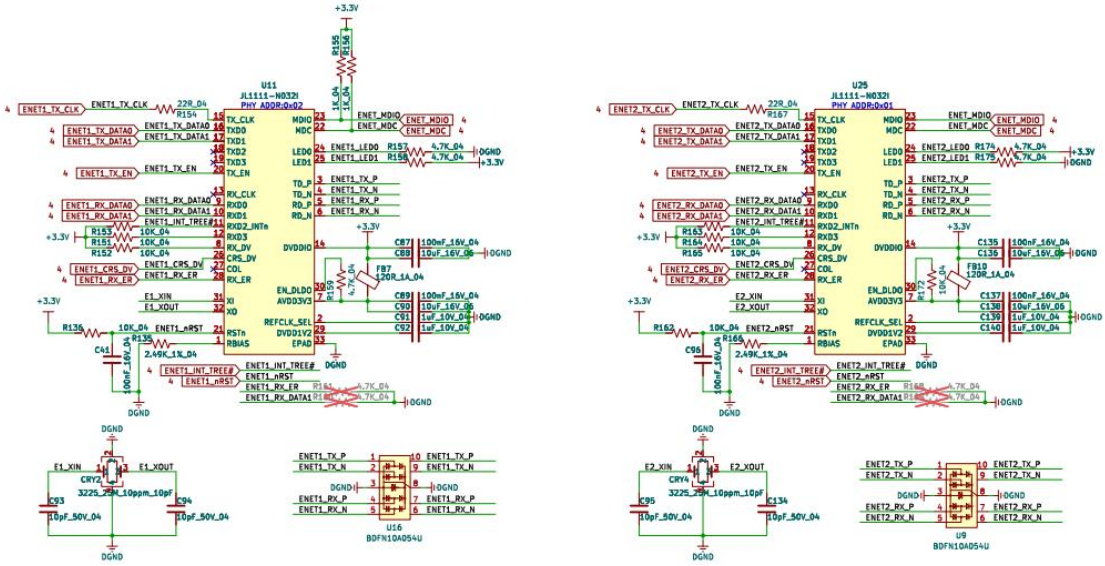
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employed, with the center tap of the transformer connected to ground through a series capacitor. The RJ45 LED indications are as follows:

LED Status Indicators for Direct Connection

Connection Status	LED Status	Transmission Status	LED Status
10M Connection	Yellow LED On	10M Transmission	Yellow LED Blinking
100M Connection	Green LED On	100M Transmission	Green LED Blinking

4.8.2. PHY Reference Circuit



Network PHY Circuit Reference Design Diagram

The baseboard design incorporates two PHY circuitry sets, with chip addresses configured through LED0 and LED1 as 0x02 and 0x01 respectively. Detailed configuration parameters are provided in the following table:

PHY Address Configuration Table

Device Position Number	LEDO	LED1	Address
U11	0	1	0x02
U25	1	0	0x01

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The PHY design is based on the JL11x1 Fast Ethernet PHY Datasheet V1.11 and employs a 25 MHz passive crystal-based clocking scheme.

The specific functionalities of the PHY chip requiring hardware configuration are detailed in the following table, including pin assignments and configurations:

PHY Pin Configuration Table

PIN NAME	PIN NO.	I/O	DESCRIPTION
RXDV	8	O, LI, PD	0: MI, 1☑: RMII mode
RXD1	10	O, LI, PD	0☑: LED, 1: WOL
LED0	24	O, LI, PD	PHY address will be set to 00000 to 00011 (For detailed pin assignments, refer to the PHY Address Configuration Table)
LED1	25	O, LI, PD	
RXD3	12	O, LI, PD	0: RMII TXCLK output, 1☑: RMII TXCLK input
RX_ER	28	O, LI, PD	0☑: UTP Mode, 1: Fiber Mode
EN_DLDO	30	I, PU	0: Pulled-down to Ground will use external 1.2V power supply, internal DLDO will be disabled, 1☑: Pulled-up to AVDD3V3 or floating will enable internal 1.2V LDO for digital
REFCLK_SEL	2	I, PU	0: 50MHz, 1: 25MHz

4.8.3. Layout Recommendations

- Do not route traces or apply copper fill beneath the Ethernet port connector to avoid ground noise coupling into the magnetics or signal traces, which may compromise signal integrity;
- RGMII differential pairs require equal spacing control, length tolerance ±10mil, differential impedance of 100Ω ±10%;
- Signal trace length from PHY to transformer end should not exceed 12 cm, and avoid vias and layer changes as much as possible;
- The 2.49KΩ RESET resistor should be placed close to the PHY, with a distance not exceeding 0.5 cm, and should be kept as far away as possible from other signal lines to avoid unnecessary interference;
- The 22Ω matching resistors on RX data lines and clock lines should be placed close to the PHY; the 22Ω matching resistors on TX data lines and clock lines should be

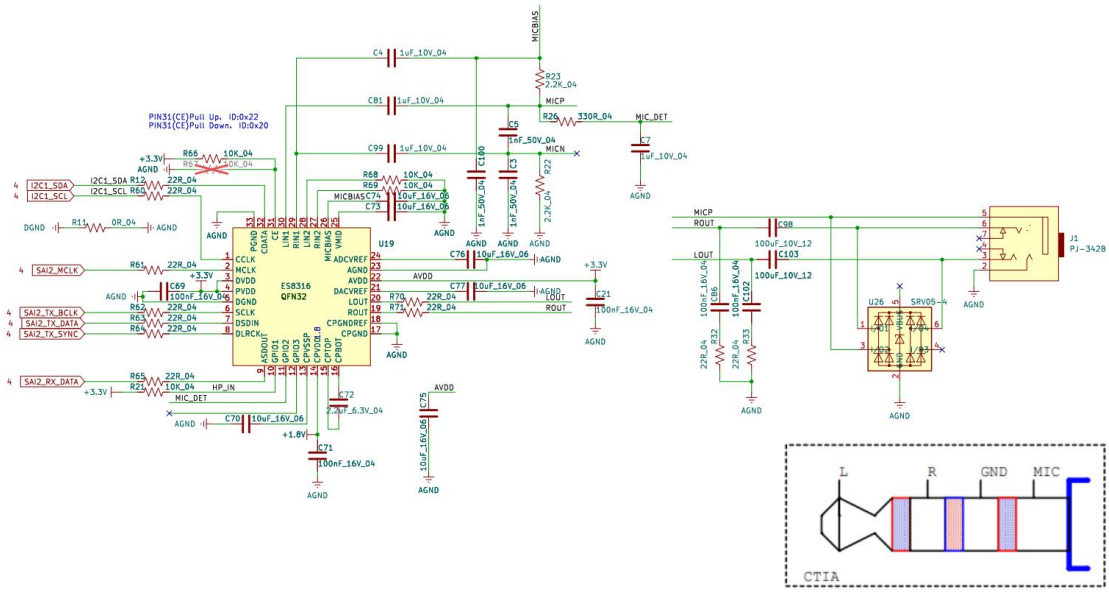
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placed close to the MCU; and the matching capacitor on the RGMII RESET line should be placed close to the PHY;

- The TVS should be placed close to the RJ45 connector;

4.9.Audio Interface Design

4.9.1.Audio Chip Circuit Design



Audio Chip Circuit Reference Diagram

The baseboard is designed with the ES8316 audio codec chip to implement headphone and microphone functions. The chip communicates with the core board via SAI and I2C signal interfaces. In the audio circuit, AUDIO_GND is isolated from the digital circuit's DGND using a zero-ohm resistor. Power pin capacitors and audio signal filter capacitors should also be connected to AUDIO_GND.

The headphone output, microphone input, and insertion detection interface are routed to a 3.5mm TRRS headphone jack compliant with international standards.

4.9.2.Layout Recommendations

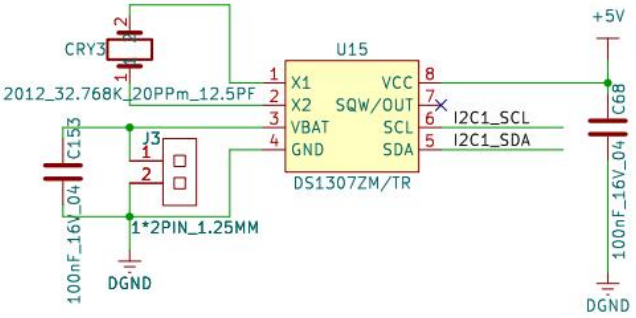
- MICIN1N/MICIN1P signal lines should be routed as differential-like lines;
- The layout position of the audio circuit should keep away from interference sources, and it is recommended to allocate a dedicated area on the PCB for analog circuits;

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- This design involves analog audio signals, and it is recommended to maintain a power trace spacing of 10 mil or more;
- Digital ground and analog ground should be connected through single-point grounding.

4.10.RTC Battery Interface

4.10.1.RTC Clock Circuit Reference Circuit



RTC Clock Circuit Schematic Diagram

The ECK20-6Y28C series core board does not use a backup battery-powered RTC. The baseboard employs a standalone RTC chip featuring automatic brownout detection and power switch circuitry. The main power supply is +5V, while the backup power is provided by a +3V battery. The battery voltage must remain between 2.0V and 3.5V for normal operation, and a CR2032 battery is recommended.

The chip includes a built-in 12.5pF load capacitor, and an external 32.768kHz crystal is required.

4.10.2.Layout Recommendations

- The crystal oscillator should be placed close to the RTC chip.
- Battery holder traces should be thickened to reduce trace resistance and minimize line loss.

4.11.Layout Recommendations

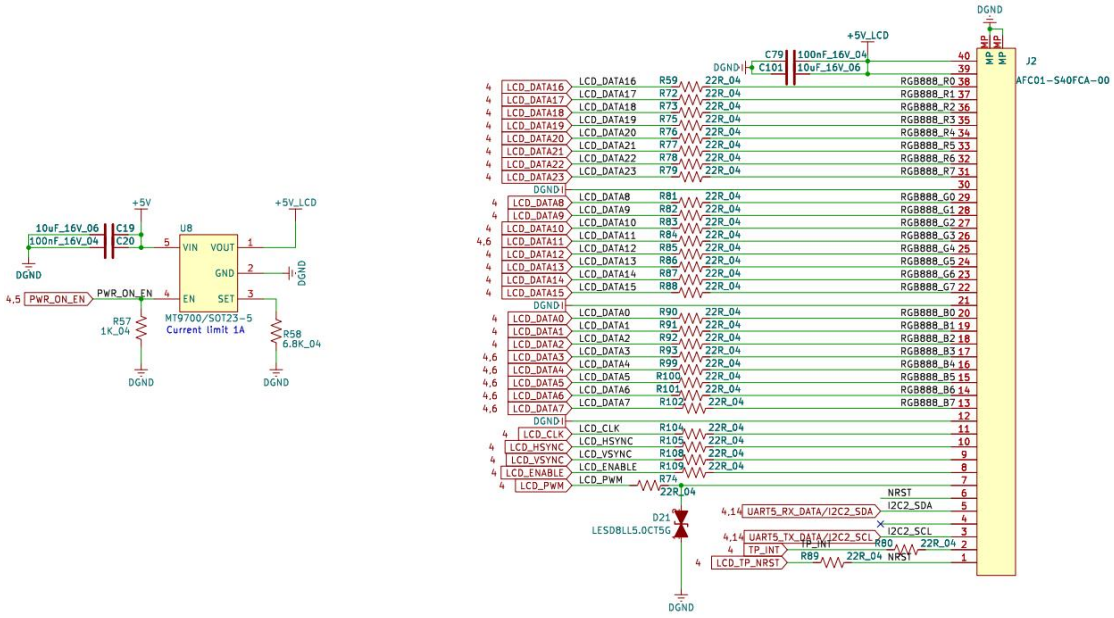
- USB_DP/USB_DN differential pairs must be routed with a differential impedance of 90Ω, ensuring adjacent layers have continuous and intact ground reference planes;

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- USB_DP/USB_DN traces should maintain a spacing of more than 10 mil from other traces and avoid routing under components;
- USB_DP/USB_DN traces should be kept as short as possible (length ≤ 4000 mil), with corner angles ≥135°, and no more than 2 vias per trace;
- USB_DP/USB_DN traces should avoid layer changes whenever possible; if layer changes are required, ground return vias must be placed within 50 mil of the layer-change vias;
- TVS devices should be placed close to the interface.

4.12.RGB_LCD Display Interface Design

4.12.1.RGB_LCD Display Interface Reference Circuit



RGB_LCD Display Interface Reference Circuit Diagram

The baseboard is designed with an RGB_LCD touch screen module interface, compatible with EBYTE ECA10-7LCD24R1006CT-C touch screen modules. The LCD_PWM signal is used to adjust the screen backlight, and a TVS is connected to prevent interference from damaging the backlight power chip.

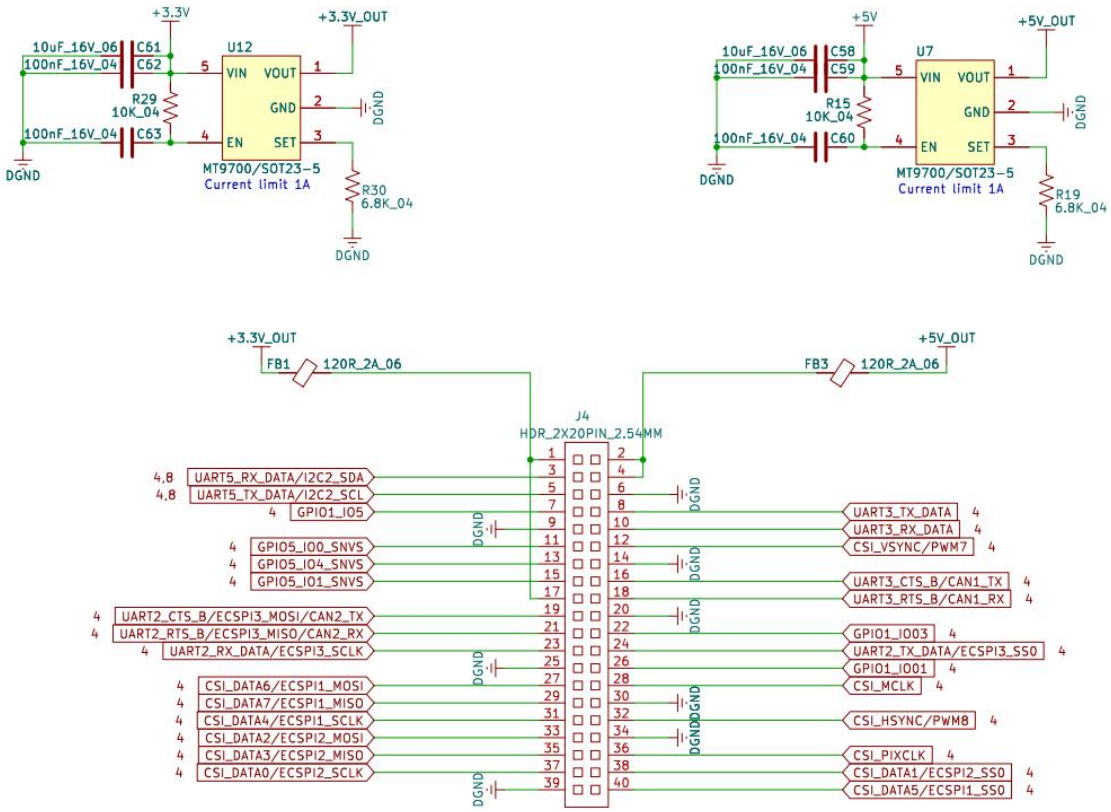
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4.12.2. Layout Recommendations

- RGB signal traces must be length-matched with an error margin of ±20 mil, meeting 50Ω impedance design;
- TVS components should be placed close to the interface.

4.13. Expansion Interface Design

4.13.1. Expansion Interface Reference Circuit



Expansion Interface Circuit Schematic Diagram

The baseboard is designed with expansion interfaces compatible with Raspberry Pi, expanding 50-pin power and signal pins. The expansion interfaces include 5V and 3.3V power outputs, each limited to 1A via the MT9700 current limiter. The signals include CSI, I2C, SPI, AUDIO, IO, UART, and CAN, with partial signal multiplexing and configurable functions. The I2C2 bus is connected to the touch screen interface, and address conflicts must be avoided during use. The CAN signals operate at TTL levels and require a level-shifting chip for user implementation. BaiRui CTM05S is recommended for level conversion.

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4.13.2. Layout Recommendations

- The dual-row pins should not be placed too close to the board edge, leaving appropriate spacing.
- Pin 1's silk-screen label must be clearly marked, with attention to anti-error precautions.

5. Software Resources

ECB20-PG6Y28C-I Test Board is equipped with an operating system based on Linux kernel version 5.10.9. The development board is pre-equipped with cross-compilation toolchains, U-boot source code, Linux kernel sources, and various driver modules required for embedded Linux system development. It also includes development and debugging tools for both Windows and Linux desktop environments.

Operating System：Ubuntu 20.04

System Source Code: u-boot 2020.04

Kernel 5.10.9

Yocto gatesgarth

Flashing Tool：uuu

Configuration Tool：Config Tools for i.MX V15

System software resources are listed in the following table：

System Software Resources Table

category	Name	Description	source code
BOOT	u-boot 2020.04	Bootloader	/source/u-boot_2020.04.tar.xz
Kernel	Kernel 5.10.9	Linux Kernel	/source/kernel_5.10.9.tar.xz
Device Driver	MMC	eMMC/TF Card Driver	drivers/mmc/host/sdhci-esdhc-imx.c
	NAND	MTD Driver	drivers/mtd/nand/raw/gpmi-nand/gpmi-nand.c
	SPI	SPI Driver	drivers/spi/spi-imx.c
	I2C	I2C Driver	drivers/i2c/busses/i2c-imx.c
	USB Host	USB Driver	drivers/usb/host/ohci-platform.c
	Ethernet	Network Driver	drivers/net/ethernet/freescale/fec_main.c

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	UART	Serial Port Driver	drivers/tty/serial/imx.c
	Can bus	CAN Bus Driver	drivers/net/can/flexcan.c
	GPIO key	Key Driver	drivers/input/keyboard/gpio_keys.c
	RTC	RTC Driver	drivers/rtc/rtc-snvs.c
	GPIO Led	Led Driver	drivers/leds/leds-gpio.c
	LCD	LCDIF Driver	drivers/video/fbdev/mxsfb.c
	Resistive Touch	ADC Touch Driver	drivers/input/touchscreen/imx6ul_tsc.c
Operating System	Rootfs	Ubuntu 20.04 system	/images/rootfs.tar.bz2
Development Tools	Yocto gatesgarth	OS Build	/source/yocto-gatesgarth.tar
	Gcc	Cross Compiler	/tools/gcc-linaro-7.5.0-2019.12-x86_64_arm-linux-gnueabihf.tar.xz
	uuu	Flashing Tool	/tools/uuu
	Config Tools for i.MX	Resource Configuration Tool	/tools/Config_Tools_for_i.MX_v15_x64.exe
	Balena Etcher	SD Bootable Media Creator	/tools/balenaEtcher-Portable-1.18.11.exe

6. Structural Dimensions

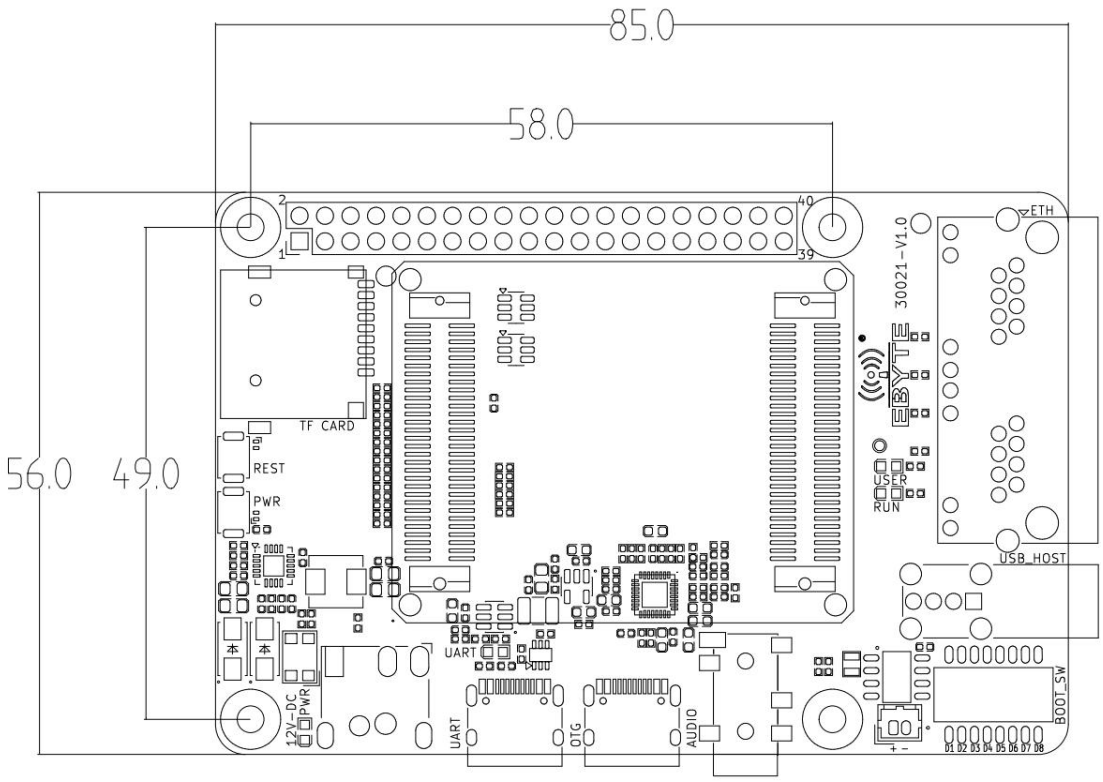
Unit: mm; Tolerance: ±0.1mm.

Side Thickness: 18mm (Front side highest component: 13.4mm + PCB: 1.6mm + Back side highest component: 3mm).

BTB Connector Height: 5mm.

Front dimensions are shown in the following figure:

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Front Structural Dimension Drawing of Test Board Base

7. Reference Documents

- i.MX6ULL_V1.9.pdf
- E103-RTL8189FTV_UserManual_CN_v1.0.pdf
- ECK20-6Y2XC Core Board Product Manual V1.0.pdf
- JL11x1 Datasheet Fast Ethernet PHY V1.11.pdf

8. Revision Notes

Revision Notes Table

Version	Modification Content	Modification Time	Prepared By	Reviewed By	Approved By
V1.0	Initial Draft	25-2-12	LJQ	WFX	WFX

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