ECB10-PGD Base Board

Product Manual



Chengdu Ebyte Electronic Technology Co.,Ltd.

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Contents

Table Index 2
Image Index 3
1. Product Overview 4
1.1. Product Introduction 4
1.2. Introduction to the STM32MP13xD chip 5
1.3. ECK10-13xD Series Core Board Introduction 7
1.4. Typical Applications 8
2. Product Selection 8
2.1. Model configuration 8
2.2. Model code 8
3. Specifications 9
3.1. Functional parameters 9
3.2. Environmental characteristics 9
4. Interface Description 10
4.1. power supply 10
4.2. Debug interface 12
4.3. TF card interface 12
4.4. Buttons and indicators 13
4.5. USB2.0 interface 13
4.6. USB_OTG interface 13
4.7. Ethernet interface 15
4.8. Audio Interface 17
4.9. RTC 18
4.10. RGB display interface 18
4.11. GPIO expansion interface 20
5. Software Resources 21
6. Structural dimensions 23
7. Reference Documentation 23
8. Revision Notes 24
9. About us 24

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Table Index

Table 2-1 Product selection and configuration table 8
Table 3-1 ECB10- PGD Base board function parameters 9
Table 3-2 ECB10-PGD test board environmental characteristics 9
Table 4-1 Power consumption parameters 11
Table 4-2 Button Function Table 13
Table 4-3 Status Light Function Table 13
Table 4-4 PHY pin configuration table 16
Table 4-5 LED status indication table 16
Table 4-6 RGB LCD interface definition table 19
Table 4-7 J10 Raspberry Pi expansion interface pin definition 21
Table 5-1 System software resources 22
Table 8-1 Revision Description Table 24

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Image Index

Figure 1.1 Base board functional description diagram 5
Figure 1.23 STM32MP135D system functional block diagram 6
Figure 2.1 Model code description 8
Figure 4.1 Base board power tree diagram 10
Figure 4.2 Base board power supply circuit reference diagram 11
Figure 4.3 Power interface diagram 11
Figure 4.4 Debug interface diagram 12
Figure 4.5 TF card interface diagram 12
Figure 4.6 USB2.0 interface diagram 13
Figure 4.7 USB_OTG interface diagram 14
Figure 4.8 USB_OTG reference circuit diagram 14
Figure 4.9 Ethernet interface diagram 15
Figure 4.10 RJ45 Ethernet components 15
Figure 4.11 Audio interface diagram 17
Figure 4.12 Audio interface schematic diagram 17
Figure 4.13 Comparison of four-segment headphone structure definitions 18
Figure 4.14 RTC battery interface diagram 18
Figure 4.15 RGB888 display interface diagram 18
Figure 4.16 Raspberry Pi expansion interface diagram 20
Figure 6.1 Base board front dimensions 23

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1. Product Overview

1.1. Product Introduction

Based on the ECK10-13xD series core board, Ebyte has launched the ECB10-PGD Base board . The core board features a 204-pin DDR3 gold finger design, making it easy for users to install and remove . The Base board design fully utilizes the core board's interfaces, including an RGB888 display interface, USB2.0, USB OTG, a TF card slot, a debug port, an Ethernet port, an audio port, and a rich set of expanded GPIO ports.

The ECB10-PGD's highly reliable quality and excellent cost control enable it to be deployed in large quantities in industrial environments. It also provides a stable reference design and a comprehensive software development environment, including hardware design documentation, software development manuals, and open-source Base board schematics, package files, and PCB design files. This effectively helps users verify core board functionality, improve development efficiency, shorten development cycles, optimize design quality, and accelerate product development and time to market.

The Base board does not come with a core board by default. Users can select a suitable core board according to their needs and install it on the Base board for use.

The Base board function diagram is as follows:

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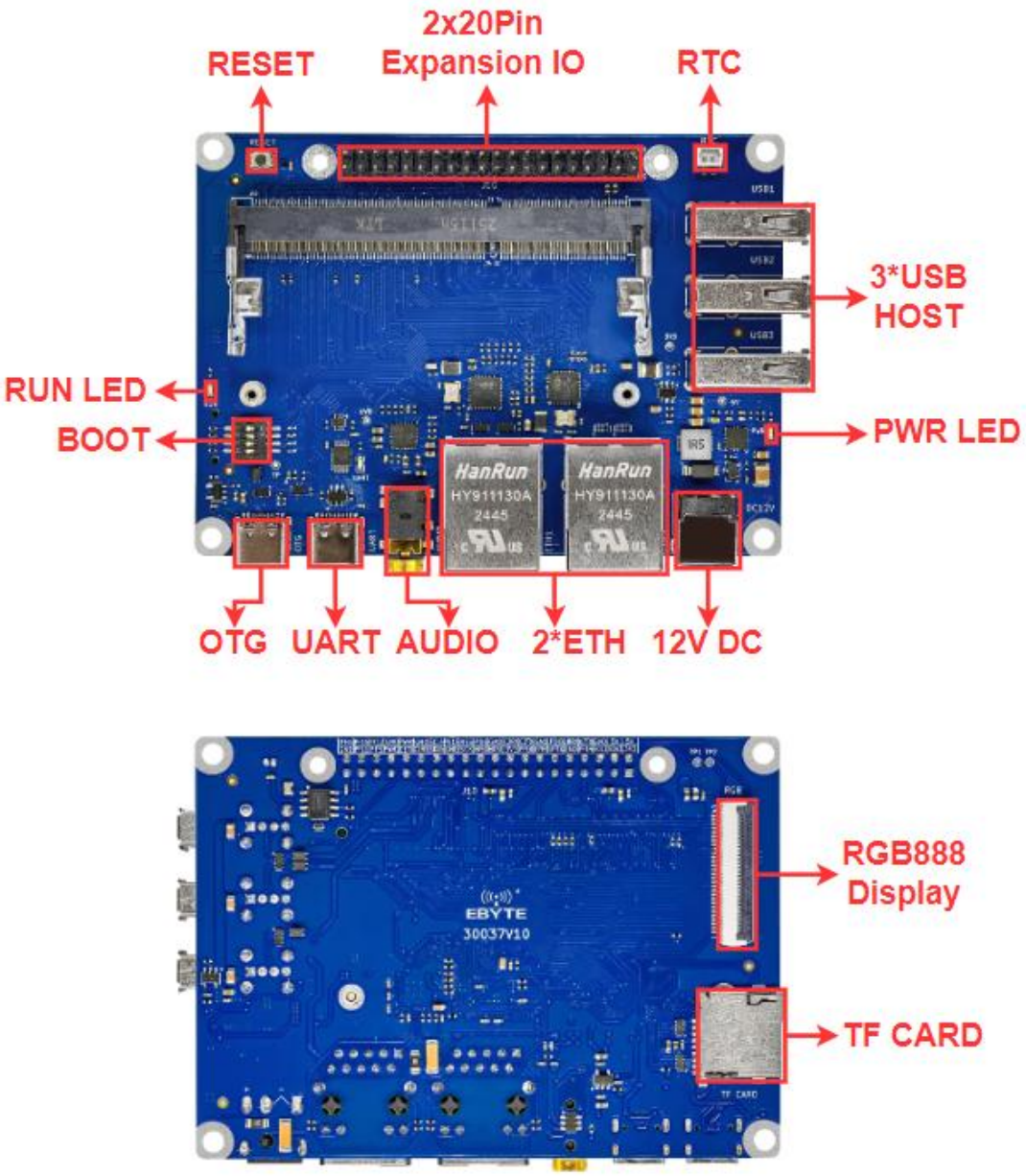


Figure 1.1 Base board functional description diagram

1.2. Introduction to the STM32MP13xD chip

STMicroelectronics' STM32MP13xD series processors utilize a single ARM Cortex-A7 core with a maximum clock speed of 1 GHz. They offer a rich array of I/O interfaces, including an LCD display , a digital camera, two Gigabit Ethernet controllers, two USB ports, eight UARTs, two SDIO ports, two CAN controllers, and multiple GPIOs. They are suitable for commercial, industrial, and automotive applications .

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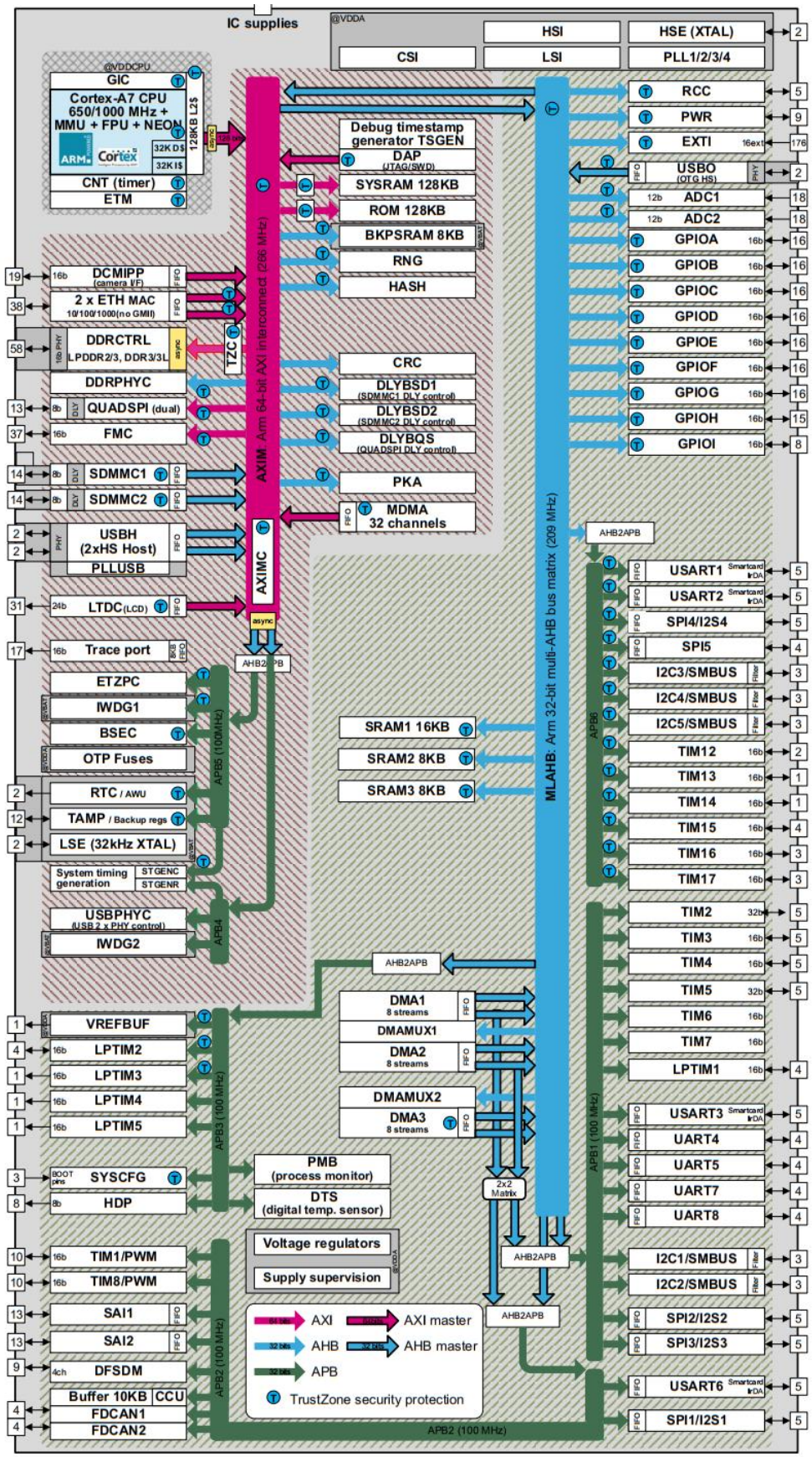


Figure 1.23 STM32MP135D system functional block diagram

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1.3. ECK10-13xD Series Core Board Introduction

The ECK10-13xD series core board of Ebyte is carefully designed based on ST's STM32MP13xD series processor and uses standard SO - DIMM. This commercial-grade embedded core board features cost-effective , low power consumption, and high reliability in a 204-pin DDR3 gold finger package. It can be widely used in Information sharing and self-service terminals, smart manufacturing, and other electronic commercial and industrial equipment. For more information, refer to the 《ECK10-13xD Product Manual (CN) V1.0》.

The ECK10-13xD series core boards include four specific product models. These differ primarily in processor model and eMMC storage capacity. Customers can select the appropriate model based on their needs. For detailed product selection information, see the Product Selection section in the 《ECK10-13xD Product Manual (CN) V1.0》.

The Product Actual Photo of the ECK10-13xD series core board is as follows:



Figure 1.3 front view of the core board



Figure 1.4 back view of the core board

The functional block diagram of the ECK10-13xD series core board is as follows:

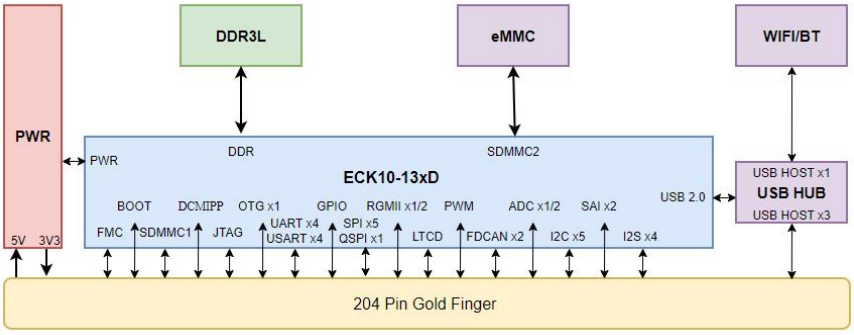


Figure 1.5 ECK10-13xD series core board functional block diagram

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1.4. Typical Applications

- Smart home;
- Smart toys;
- Smart cities;
- tablet computers ;
- IoT gateway ;
- Advertising all-in-one machine ;
- Industrial all-in-one machine ;
- Industrial control motherboard;
- Robots and drones.

2. Product Selection

2.1. Model configuration

ECB10-PGD series base board selection and configuration table is as follows:

Table 2-1 Product selection and configuration table

No	Model	Operating temperature
1	ECB10-PGD-I	industrial grade, -40℃ ~ 85℃

2.2. Model code

The product model coding is shown in the figure below:

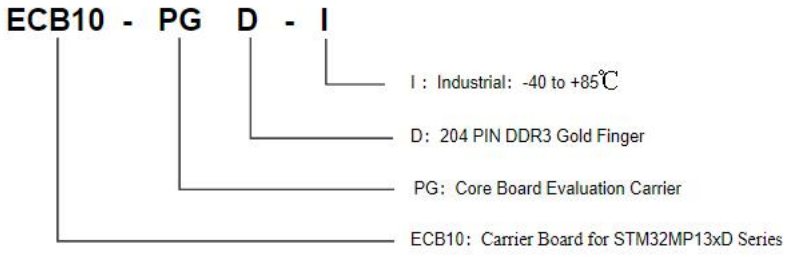


Figure 2.1 Model code description

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3. Specifications

3.1. Functional parameters

Table 3-1 ECB10- PGD Base board function parameters

Power input	1x DC socket, 12V input;
Display Output	1x 40-pin FPC parallel display interface, maximum resolution supports WXGA (1366 × 768@60fps) , RGB888 parallel display output , and supports touch screen;
USB HOST	3x USB2.0 HOST;
USB OTG	1x USB OTG;
Ethernet	2x 10/100 /1000M adaptive RJ45 Ethernet port;
TF card	1x TF card slot, supports plug-in detection ;
Audio	1x 3.5mm four-section headphone jack, supports MIC input ;
Debug	1x UART debug serial port , Type-C interface ;
GPIO	1x 2.54mm2x20Pin standard RPI expansion interface, providing 3.3V and 5V power output, a total of 28 GPIO ports, multiplexing 1x SPI interface, 2 x I2C interface, 2x UART, and 2x FDCAN;
Button	1x RESET button;
Status light	1x power indicator light ;1 running indicator light ;1 debugging indicator light ;
RTC	1x 1.25mm 1x2Pin RTC battery holder;
BOOT	1x DIP switch to select the starting mode ;
PCB size	100x72x1.6mm, 2.5 inches ;

3.2. Environmental characteristics

Table 3-2 ECB10-PGD test board environmental characteristics

Operating temperature	Industrial grade: -40℃ ~ 85℃ (environment with good heat dissipation conditions);
Storage temperature	-40℃ ~ 85℃;
Operating humidity	5~95% humidity, non-condensing;
Storage humidity	60℃@95% humidity, non-condensing;

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4. Interface Description

4.1. power supply

4.1.1. Power Tree

The Base board power tree diagram is as follows:

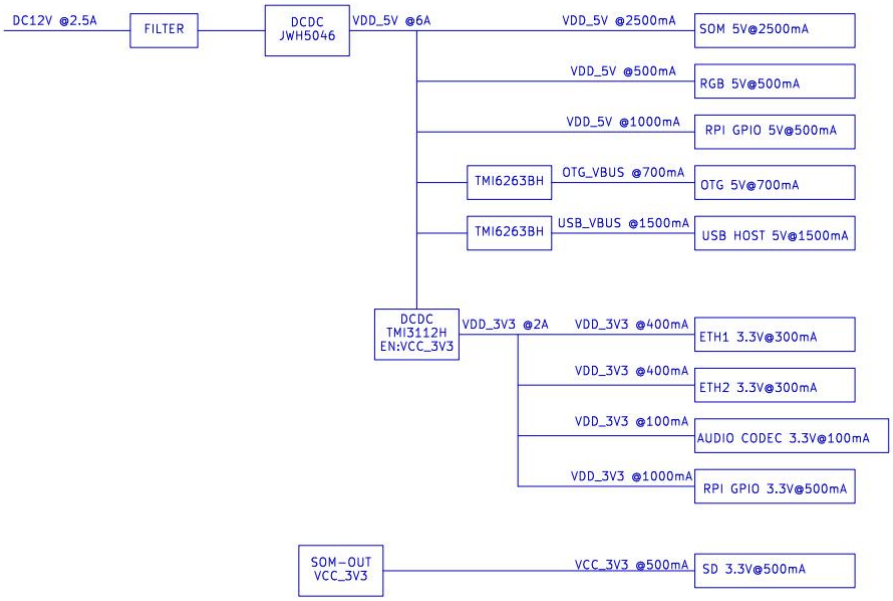


Figure 4.1 Base board power tree diagram

4.1.2. Power supply design

The power supply utilize a 12V DC input and features reverse polarity protection and TVS surge protection circuitry. The 12V is stepped down to 5V via a DC-DC converter, supporting a maximum current of 6A. The 5V is then stepped down to 3.3V via a DC-DC converter, supporting a maximum current of 2A. The 3.3V power supply is then stepped down to 1.8V via an LDO, providing the IO level for the audio decoder chip. See the Base board power tree diagram for detailed power routing.

Because the TF card and serial port debugging circuit need to be powered on before other interfaces, the core board's VCC_3V3 power supply is used. The 3.3V power enable signal is controlled by the core board's VCC_3V3 output to ensure normal backplane timing and avoid IO leakage.

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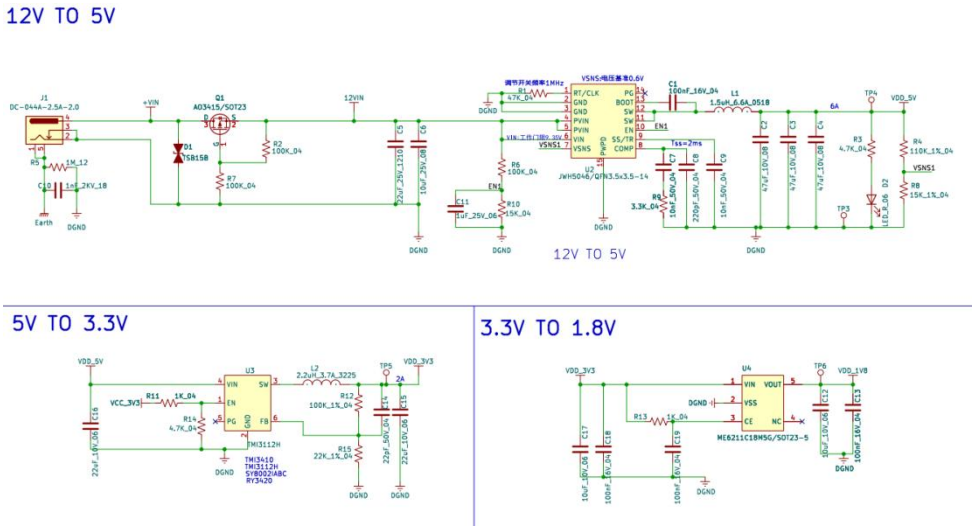


Figure 4.2 Base board power supply circuit reference diagram

The power input port is located in the lower right corner of the Base board and uses a DC2.0 round connector, as shown in the power port diagram. Users can select a 12V power adapter with the appropriate power rating based on their needs. For detailed power distribution, refer to the Base board power tree diagram.



Figure 4.3 Power interface diagram

4.1.3. Power consumption

Table 4-1 Power consumption parameters

Working conditions	Power supply voltage (V)	Average current (A)	Power consumption (W)
Uboot status, kernel not booted	12	0.13	1.56
After the system starts, no application is running	12	0.17	2.04
Software reload testing	12	0.31	3.72
mem mode sleep state	12	0.07	0.84
Power consumption in poweroff state	12	0.12	1.44

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4.2. Debug interface

The debug port converts UART signals to USB signals via the CH340X chip. The Type-C interface is designed for user convenience, eliminating the need for a serial port converter chip. When a signal is connected to the Type-C debug port on the Base board, the yellow UART LED above the port illuminates steadily. The debug port is located on the lower right side of the Base board, as shown in the following figure.

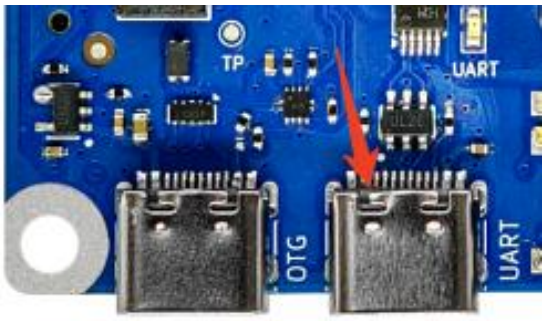


Figure 4.4 Debug interface diagram

4.3. TF card interface

The TF card slot is located on the right side of the back panel. Users can purchase a TF card larger than 16GB. Find the corresponding product on the Chengdu Yibite official website, download the relevant program, and then burn it to the card. Alternatively, you can directly burn the program via OTG. When inserting an SD card, pay attention to the orientation, as shown in the figure below. When removing it, gently press inward on the card to eject it.

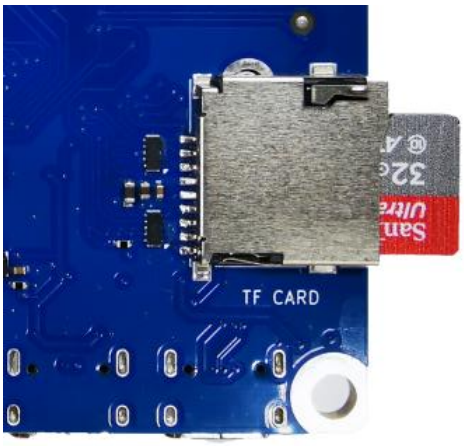


Figure 4.5 TF card interface diagram

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4.4. Buttons and indicators

Table 4-2 Button Function Table

Button Name	Function	Remark
RESET	Hardware reset signal	

Table 4-3 Status Light Function Table

Status light name	Function	Remark
PWR	Power indicator	Red, steady on
RUN	Running indicator light	Green, flashing
UART	Debug serial port indicator	Yellow, steady on

4.5. USB2.0 interface

This product provides three USB 2.0 ports located on the right side of the front panel, as shown in the USB 2.0 port diagram below. Users can use these ports to connect devices such as a mouse, keyboard, and USB flash drive, or to connect multiple devices to an external USB hub. Note that the USB 2.0 ports only support host mode, and all three ports support a total output current of 1500mA.



Figure 4.6 USB2.0 interface diagram

4.6. USB_OTG interface

A USB_OTG port is provided, located on the lower left side of the front of the Base board, as shown in the USB_OTG port diagram below. It uses a TYPE-C port for user convenience and supports OTG and HOST modes. Users can directly burn programs through this port.

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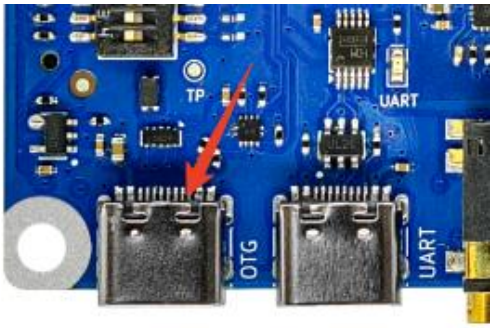


Figure 4.7 USB_OTG interface diagram

The OTG interface design incorporates a TPYE-C power configuration detection circuit, using the Type-C configuration chip WUSB3801Q-12 to detect the CC pin configuration of the external device . By comparing the CC pin voltage levels, it detects the CC connection status under different connection topologies and settings. This information is then output to the processor, which controls whether the OTG circuit load switch outputs power. See the diagram below for the circuit design.

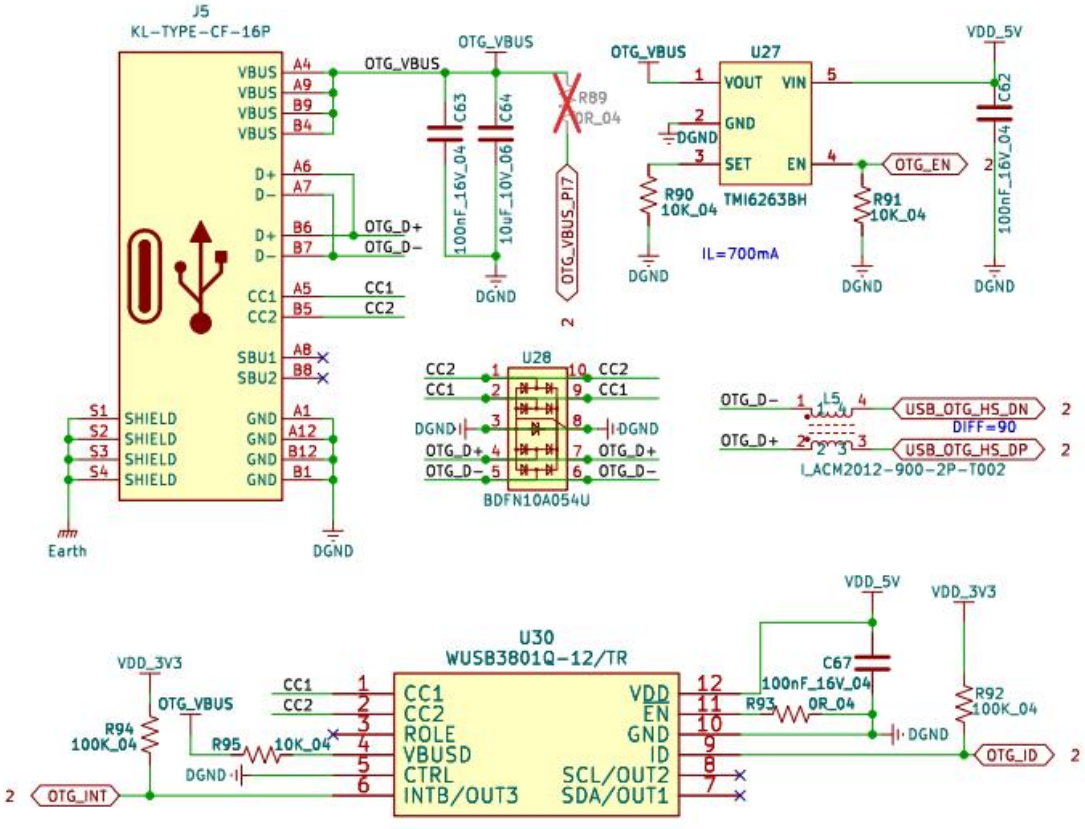


Figure 4.8 USB_OTG reference circuit diagram

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4.7. Ethernet interface

Two RJ45 Ethernet interfaces are located at the bottom of the front of the Base board, as shown in the following figure:



Figure 4.9 Ethernet interface diagram

Both Ethernet ports support 10M/100M /1000M adaptive Ethernet controllers . The RJ45 Ethernet port consists of the Ethernet controller (MAC), Ethernet physical layer (PHY), Ethernet transformer, and RJ45 connector, as shown in the figure below.

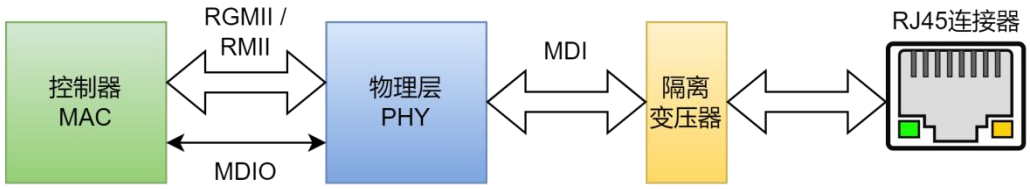


Figure 4.10 RJ45 Ethernet components

The Base board uses the MAE0621A physical layer chip, designed according to the MAE0621A Design Guide V1.1. A 25MHz passive crystal clock is used. The RJ45 connector has a built-in transformer, eliminating the need for a separate transformer circuit. During PCB layout, ensure the copper under the RJ45 connector is hollowed out to prevent interference from the transformer.

the ETH 1 PHY design is 001 (binary), that is, PHYAD0, PHYAD1, and PHYAD2 corresponding to PHYAD[2:0] are configured as 001. RXDLY and TXDLY are both configured as 1 (valid), and PLLOFF is configured as 0 (invalid).

the ETH 2 PHY design is 010 (binary), that is, PHYAD0, PHYAD1, and PHYAD2 corresponding to PHYAD[2:0]

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are configured as 010 respectively. RXDLY and TXDLY are both configured as 1 (valid), and PLLOFF is configured as 0 (invalid).

Some functions of the PHY chip require corresponding configuration by hardware. The specific pins and configurations are as follows:

Table 4-4 PHY pin configuration table

PIN NAME	PIN NO.	I/O	DESCRIPTION
PHYAD0	22	O/LI/PU	PHYAD[2:0]. Sampled on reset. The PHY address selects MII management PHY address.
PHYAD1	27	O/LI/PD	
PHYAD2	26	O/LI/PD	
PLLOFF	23	O/LI/PD	ALDPS Mode PLL Off Configuration. Pull up to stop PLL when entering ALDPS mode.
TXDLY	24	O/LI/PD	RGMII Transmit Clock Timing Control. Pull up to add 2ns delay to TXC for TXD latching.
RXDLY	25	O/LI/PU	RGMII Receive Clock Timing Control. Pull up to add 2ns delay to RXC for RXD latching.
CFG_EXT	32	O/LI/PD	RGMII and SMI I/O Pad Power Source Mode Configuration. When pulling down CFG_EXT, CFG_LDO[1:0] represent LDO output voltage setting for IO pad: 2'b00: Reserved; 2'b01: 2.5V from internal LDO; 2'b10: 1.8V from internal LDO; 2'b11: 1.5V from internal LDO. When pulling up CFG_EXT, CFG_LDO[1:0] represent the input voltage of IO pad is selected from external power: 2'b00: 3.3V from external power; 2'b01: 2.5V from external power; 2'b10: 1.8V from external power; 2'b11: 1.5V from external power.
CFG_LDO0	33	O/LI/PU	
CFG_LDO1	34	O/LI/PD	

Table 4-5 LED status indication table

Connection Status	LED Status	Transmitting Status	LED Status
10MConnection	2 LED off	10MTransmitting	2 LED off
100MConnection	Yellow LED On	100MTransmitting	Yellow LED Blinking
1000MConnection	Green LED On	1000MTransmitting	Green LED Blinking

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4.8. Audio Interface

The audio interface is located at the lower left of the Base board. The audio interface uses a 3.5mm, CTIA four-section headphone interface, which supports microphone input and headphone output, as shown in the figure below.



Figure 4.11 Audio interface diagram

Since the STM32MP13xD series processors do not have analog audio signals, the Base board uses a set of I2S as digital audio signals and uses the audio codec ES8316 to implement the codec conversion between analog audio and I2S digital audio. The schematic diagram is as follows:

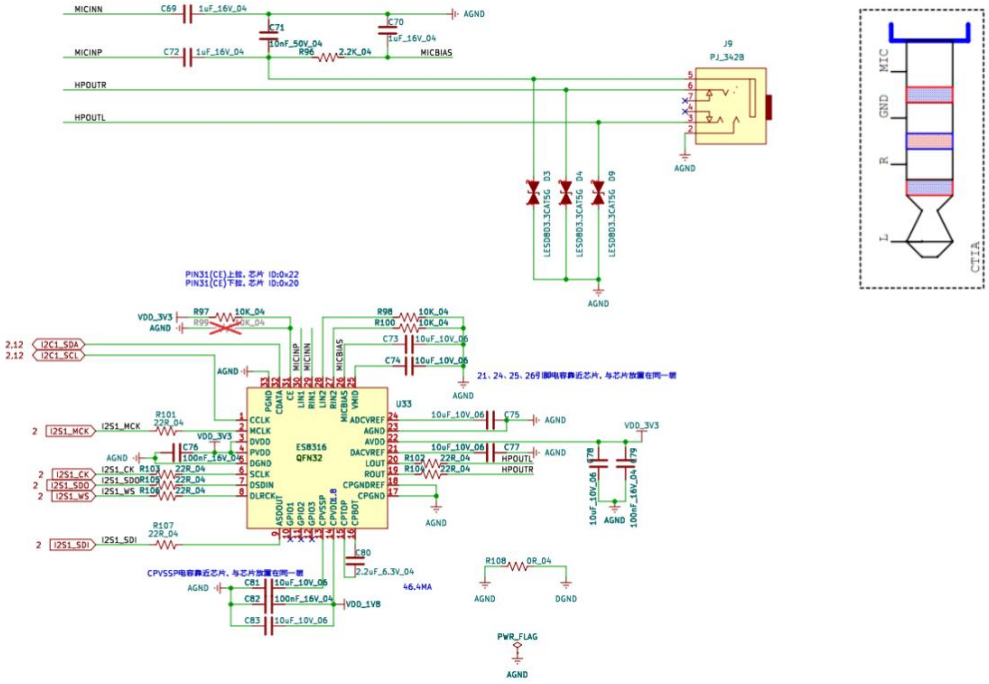


Figure 4.12 Audio interface schematic diagram

Note that different standard headphone jack structures and wiring sequences are different. You need to connect according to the actual interface used. For details, refer to the corresponding headphone jack manual. This product uses

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the American standard CTIA four-segment headphone. The differences between the American standard and European standard interfaces are shown in the figure below .

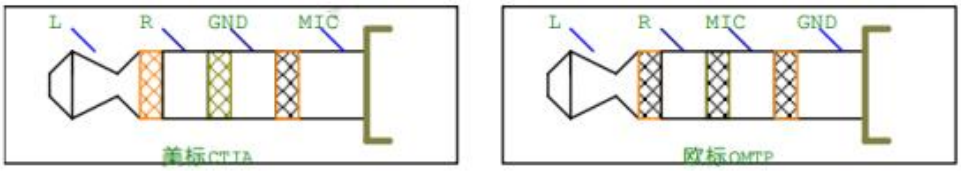


Figure 4.13 Comparison of four-segment headphone structure definitions

4.9. RTC

The Base board uses a separate RTC chip to provide clock data. The chip features automatic power-loss detection and power switching circuitry. The main power supply is a +5V power supply, and the backup power supply is a +3V battery. The battery voltage must be maintained between 2.0V and 3.5V for normal operation. In battery-powered mode, the oscillator consumes less than 500nA. A CR2032 battery is recommended. The battery interface uses a 1x2-pin, 1.25mm-pitch connector located on the upper right side of the front of the Base board, as shown in the figure below.



Figure 4.14 RTC battery interface diagram

4.10. RGB display interface

The RGB display interface uses a 40-pin 0.5mm FPC connector, located on the right side of the back of the Base board, as shown in the following figure:

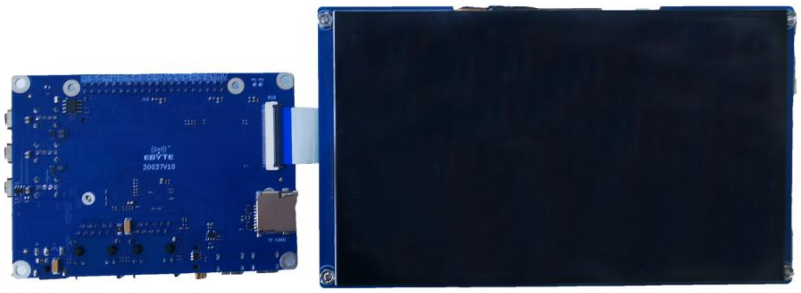


Figure 4.15 RGB888 display interface diagram

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This interface uses the RGB888 data format and supports touch screens (capacitive screens). It only supports LCDs with RGB interfaces (not LCDs with MCU interfaces). It is compatible with Ebyte's 7- inch RGB interface touch screen module ECA10-7LCD24R1006CT-C . Note that the order of the Base board FPC interface definition is opposite to that of the ECA10-7LCD24R1006CT-C display screen FPC interface definition. Pin 1 of the Base board corresponds to pin 40 of the display screen, and pin 40 of the Base board corresponds to pin 1 of the display screen. Do not connect them incorrectly, otherwise the circuit board may be damaged. The RGB LCD interface definition is shown in the following table:

Table 4-6 RGB LCD interface definition table

Pin No.	Pin Name	MCU I/O	Functions
1	LCD_RST	PG12	Screen display reset
2	TP_INT	PD8	Touch interruption
3	TP_SCL	PF2	Touching the I2C clock signal, there is a 2.2K pull-up
4	NC	/	/
5	TP_SDA	PF1	Touch I2C data signal, with 2.2K pull-up
6	TP_RST	PG8	Touch reset
7	LCD_PWM	PD12	Screen backlight adjustment
8	LCD_DE	PH9	Data enable signal
9	LCD_VSYNC	PG4	Frame synchronization signal
10	LCD_HSYNC	PE9	Line synchronization signal
11	LCD_CLK	PD9	Pixel clock signal
12	GND	/	power ground
13	LCD_B7	PE15	Blue signal B7
14	LCD_B6	PB6	Blue signal B6
15	LCD_B5	PD15	Blue signal B5
16	LCD_B4	PH3	Blue signal B4
17	LCD_B3	PF8	Blue signal B3
18	LCD_B2	PH7	Blue signal B2
19	LCD_B1	PE13	Blue signal B1

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20	LCD_B0	PD5	Blue signal B0
21	GND	/	power ground
22	LCD_G7	PE4	Green signal G7
23	LCD_G6	PE12	Green signal G6
24	LCD_G5	PD10	Green signal G5
25	LCD_G4	PD13	Green signal G4
26	LCD_G3	PF3	Green signal G3
27	LCD_G2	PD1	Green signal G2
28	LCD_G1	PH2	Green signal G1
29	LCD_G0	PE14	Green signal G0
30	GND	/	power ground
31	LCD_R7	PD11	Red signal R7
32	LCD_R6	PH8	Red signal R6
33	LCD_R5	PE7	Red signal R5
34	LCD_R4	_PD14	Red signal R4
35	LCD_R3	PB12	Red signal R3
36	LCD_R2	PG7	Red signal R2
37	LCD_R1	PD4	Red signal R1
38	LCD_R0	PA15	Red signal R0
39	VDD_5V	/	5V power supply
40	VDD_5V	/	5V power supply

4.11. GPIO expansion interface

Design a Raspberry Pi 2x20Pin 2.54mm standard expansion interface, located on the upper front of the Base board, as shown in the figure below.



Figure 4.16 Raspberry Pi expansion interface diagram

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The IO interface provides multiplexing functions, including up to 1x SPI interface, 2x CAN interfaces (TTL level), 1x I2C interfaces, and 2x UART interfaces, which can be configured according to user needs. In addition, the 3.3V and 5V power supplies provided by each expansion interface support 500mA current output. Detailed definitions are provided in the table below.

Table 4-7 J10 Raspberry Pi expansion interface pin definition

Pin No.	Pin. Function	Pin No.	Pin Function
1	3V3	2	5V
3	PD7/I2C3_SDA	4	5V
5	PH12/I2C3_SCL	6	GND
7	GPIO_PF14	8	PE1/UART8_TX
9	GND	10	PF9/UART8_RX
11	PE8/UART7_TX	12	GPIO_PD0
13	PE10/UART7_RX	14	GND
15	GPIO_PF10	16	PG0/CAN2_TX
17	3V3	18	PE0/CAN2_RX
19	PH10/SPI2_MOSI	20	GND
21	PB5/SPI2_MISO	22	GPIO_PD6
23	PB10/SPI2_SCK	24	PB13/SPI2_NSS
25	GND	26	GPIO_PG15
27	PB8/I2C4_SDA	28	PE2/I2C4_SCL
29	PG10/CAN1_TX	30	GND
31	PG9/CAN1_RX	32	PE11/PWM1
33	PF13/PWM2	34	GND
35	GPIO_PF5	36	GPIO_PF12
37	PI12	38	GPIO_PF15
39	GND	40	GPIO_PH4

5. Software Resources

The ECB10-PGD Base board and the CK10-13xD core board are equipped with an operating system based on the Linux 5.15 kernel. The core board comes with the cross-compilation tool chain required for embedded Linux system development, TF-A source code, Optee-OS source code, U-boot source code, source code for the Linux kernel and various driver modules, and various development and debugging tools for Windows and Linux desktop environments.

operating system:

Ubuntu 18.04 system

System source code:

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TF-A 2.6

Op-tee 3.16

U-boot 2021.10

Kernel 5.15.67

BuildRoot 2022.02.3

Development environment and IDE:

Burning tool: STM32CubeProgrammer

Development tool: STM32CubeMX

System software resources are shown in the following table:

Table 5-1 System software resources

Type	Name	Description	Source Code
FSBL	TF-A	First level bootloader	/source/tf-a.tar.gz
SSBL	Op-tee	Second level bootloader	/source/optee.tar.gz
SSBL	U-boot	Second level bootloader	/source/u-boot.tar.gz
Linux kernel	Kernel	Linux Kernel	/source/linux.tar.gz
Device Driver	USB Host	USB Host	kernel/
	USB OTG	USB OTG	kernel/
	I2C	I2C bus driver	kernel/
	SPI	SPI bus driver	kernel
	TTY	TTY serial port driver	kernel
	RS232	TTY serial port driver	kernel
	RS485	TTY serial port driver	kernel
	CAN	CAN bus driver	kernel
	Ethernet	10M/100M/1000M driver	kernel
	MMC	EMMC/TF card storage driver	kernel
	NAND	NandFlash storage driver	kernel
	LCD	RGB display driver	kernel
	PWM	PWM control drive	kernel
	ADC	ADC driver	kernel
	RTC	Real time clock driven	kernel
	GPIO	GPIO driver	kernel
	Touch	Capacitive touch drive	kernel
	Watchdog	Watchdog driver	kernel
Operatating System	Rootfs	Builroot system	/images/ rootfs.ext4 /images/ubuntu-1804.ext4

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Develop Tool	BuildRoot	Ubuntu 18.04 system	/ source /ebyte-mp135-sdk-buildroot.tar.gz
	SDK	Operating System Construction	/tools/SDK-x86_64-stm32mp1-openstlinux.tar.gz
	STM32CubeProgrammer	arm-ostl-linux-gnueabi-gcc 11.3	/tools/ SetupSTM32Cube Programmer-2.5.0.exe
	STM32CubeMX	Burning tool	/tools/ en.stm32cubemx_v6-0-1.zip
	Win32DiskImager	Resource allocation tool	/tools/ Win32DiskImager-1.0.0-binary

6. Structural dimensions

Unit: mm; error: ±0.1mm.

The front dimensions are shown in the figure below:

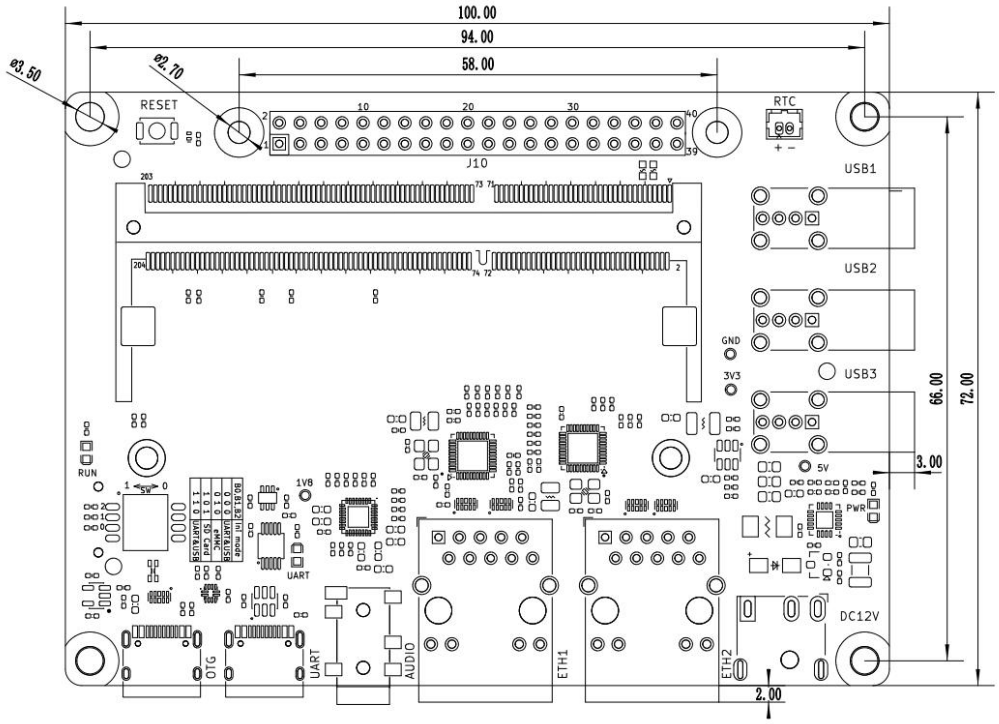


Figure 6.1 Base board front dimensions

7. Reference Documentation

- STM32MP135DAF7 Datasheet.pdf
- ECK10-13xD_ProductManual_CN_V1.0.pdf

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8. Revision Notes

Table 8-1 Revision Description Table

Version	Modifications	Modification time	prepared by	Proofreading	Approval
V1.0	First Draft	25-8-20	WJ	LQ	WFX

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