E106-xxxG27P2 (SX1303) Product Specification Sheet

SX1303 470MHz/915MHz PCIE 27dBm



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1. Overview

1.1. Introduction

The E106-xxxG27P2 (SX1303) module is a LoRa gateway RF module designed based on the SX1303 chip solution. It features a standard Mini PCI-e form factor and an SPI interface; the module incorporates a built-in PA and LNA, and adopts a half-duplex design, facilitating rapid development of LoRa gateway devices by users.

The SX1303 is Semtech's next-generation LoRa gateway baseband chip, featuring the SX1250 front-end module and supporting frequency hopping factors ranging from SF5 to SF12. Compared to the previous-generation SX1301 gateway solution, it enables higher data transmission rates, significantly reduces power consumption, simplifies the thermal design of the gateway, and delivers substantially enhanced performance.

E106-xxxG27P2 (SX1303) refers to two separate modules operating at the 915 MHz and 470 MHz frequency bands, respectively; they are compatible in terms of packaging, with the only difference being their respective frequency bands.

product model	E106-470G27P2(SX1303)	E106-915G27P2(SX1303)
Product Schematic Diagram		
Operating frequency band	CN470	US915
transmitting power	27dBm	27dBm
size	50.95*30mm	50.95*30mm

Note: For detailed specifications, please refer to this article.

1.2. Main Characteristics

- Supports the PCI Express Mini Card 1.2 standard interface;
- Equipped with precise timestamping, enabling further TDOA network-based positioning;
- Supports multiple modulation schemes, including LoRa and (G)FSK;
- Maximum transmit current: 360 mA; Maximum receive current: 60 mA;
- I-PEX antenna interface; half-duplex communication;
- Standard SPI digital interface;
- Supports up to 8 receive channels with full SF5–SF12 resolution, featuring a minimum receive sensitivity of-141 dBm;
- Supports one transmit channel with a maximum transmit power of 27 dBm (typical value: 26 dBm);
- Supported unlicensed frequency bands: CN470, US915;

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1.3. Module Block Diagram

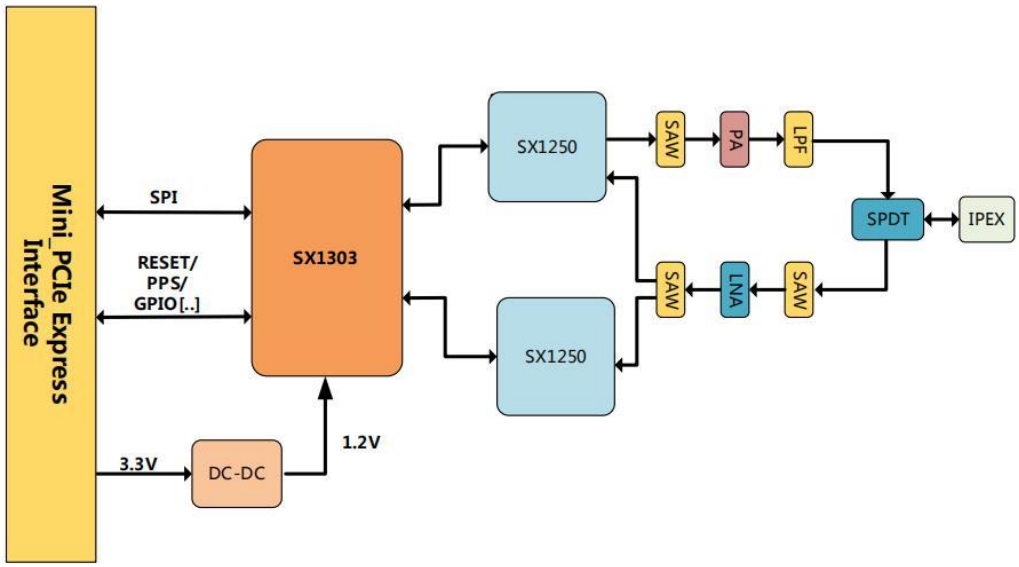


Figure 1: Functional Block Diagram of the E106-xxxG27P2 (SX1303) Gateway Module

2. Interface Electrical and RF Performance

2.1. Power Supply Characteristics

The E106-xxxG27P2 module is powered by a 3.3 V supply; the input voltage is 3.3 V ±9%, and the power supply input must have a minimum current delivery capability of 500 mA. The module's input current requirements are as shown in the table below:

Table 7: Power Input Range

parameter	description	least value	representative value	crest value	unit
VCC	Module Supply Voltage	3.0	3.3	3.6	V

2.2. IO Interface Characteristics

The digital I/O electrical characteristics of the E106-xxxG27P2 module are shown in the table below.

Table 8: IO Interface Electrical Characteristics

parameter	description	least value	crest value	unit
VIH	put high level voltage	0.7*VCC	VCC+0.3	V
VIL	Input low-level voltage	-0.3	0.3*VCC	V
VOH	output high level voltage	VCC-0.5	VCC	V
VOL	Low-level voltage output	0	0.4	V

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2.3. Operating Current

Table 9: Operating Current

parameter	Work Conditions	representative value	unit
RX	Enable reception, disable TX	54	mA
TX/RX	Enable reception; Set TX to 25 dBm	360	mA
IDLE	Idle Mode	27	mA

4.4. RF Performance

Table 10: RF Module Transmitter Power

Operating frequency band	Maximum power value	unit
505.5MHz	26	dBm
915.5MHz	TBD	dBm

Table 11: RF reception sensitivity

Operating frequency band	Spread Spectrum Factor (BW = 125 kHz)	Reception sensitivity (typical value: dBm)
475.5MHz	SF=5	-121
	SF=7	-127
	SF=12	-141
915.5MHz	SF=05	TBD
	SF=07	TBD
	SF=12	TBD

2.2. Power Interface

Table 4: Power Interface Definition

name	Pin number	IO attribute	functional description
GND	4,9,15,18,21,26,27,29,34,35,37,40,43,50		
3.3V	2,24,39,41,52	PI	3.3 V power input

The E106-xxxG27P2 module is powered by a 3.3 V supply; in TX mode, the instantaneous peak current can reach up to 400 mA. To prevent voltage sag, the switching power supply or LDO used must be capable of delivering sufficient current; additionally, a large-capacitance tantalum or electrolytic capacitor should be connected at the module's power input port. When using a switching power supply to power the module, the circuit traces should be routed as far as possible away from the antenna section to mitigate EMC interference.

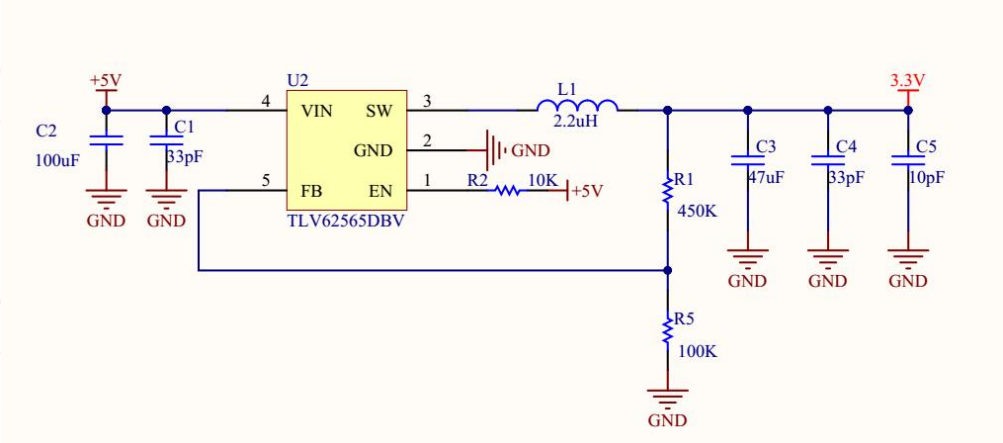


Figure 2: DC-DC Reference Circuit

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2.3. SPI Interface

The SPI interface signal definitions for the E106-xxxG27P2 module are shown in the table below.

Table 5: SPI Interface Signal Definitions

name	Pin number	I/O attribute	functional description	Voltage domain
SX_SCK	45	DI	SPI clock signal input	3.3V
SX_MISO	47	DO	SPIpresentation of information	3.3V
SX_MOSI	49	DI	SPIdata-in	3.3V
SX_CSN	51	DI	SPI Chip Select Signal Input	3.3V

Note: The main SPI interface must support full-duplex operation; for specific timing requirements, please refer to the SX1303 datasheet.

2.4. Control Signal

Table 6: Control Signal Interface Definition

name	Pin number	I/O attribute	functional description	Voltage domain
PPS	11	DI	GPS timing input	3.3V
NRESET	22	DI	Reset Control Pin	3.3V
RX_ON	42	DO	RX Signal Indicator	3.3V
TX_ON	44	DO	TX Signal Indicator	3.3V
CFG_ON	46	DO	CFG Signal Indicator	3.3V

2.4.1. PPS Signal

Supports GPS-PPS input for receiving data packets with timestamps.

2.4.2. NRESET Signal

An external control circuit can be used to reset the module. To reset the module, pull the NRESET interface signal high for 0.05–0.2s and then release it. The NRESET signal is relatively sensitive to interference; therefore, the traces on the module interface board should be as short as possible and should be properly grounded.

2.4.3. RX_ON Signal

GPIO3 connected to the SX1303.

2.4.4. TX_ON Signal

GPIO5 connected to the SX1303.

2.4.5. CFG_ON Signal

Once the module's configuration parameters are successfully set, this pin outputs a high-level signal, and the onboard LED lights up; this pin is connected to the GPIO interface of the SX1303.

2.4.6. TX_LED Indicator Light

When the module is in transmit mode, the LED lights up.

2.4.7. RX_LED Indicator Light

When the module is in the receiving state, the LED lights up.

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3. Interface Description

3.1. Interface Definition

The E106-xxxG27P2 features a standard Mini PCI Express interface; the table below provides the functional definitions and descriptions for the corresponding 52-pin gold finger pins of this module.

Table 1: IO Parameter Definition

attribute	description
DI	digital input
DO	numeric output
IO	Bidirectional input/output
PI	power input

Table 2: Primary Function Pin Definitions

name	Pin number
GND	4,9,15,18,21,26,27,29,34,35,37,40,43,50
3.3V	2,24,39,41,52
PPS	19
NRESET	22
RX_ON	42
TX_ON	44
CFG_ON	46
SX_SCK	45
SX_MISO	47
SX_MOSI	49
SX_CSN	51

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Table 3: Detailed Pin Definitions

number	MiniPCIe Pin Definition	E106-xxxG27P2 Pin Definitions	I/O attribute	functional description	remarks
1	WAKE#	RESERVED	DO	Use the transparent version; suspended.	
2	3.3Vaux	VCC_3V3	PI	3.3 V DC Main Power Input	
3	COEX1	NC	—	For internal use; keep suspended.	
4	GND	GND	—	the ground	
5	COEX2	NC	—	For internal use; keep suspended.	
6	1.5V	NC	—	unused	
7	CLKREQ#	NC	—	For internal use; keep suspended.	
8	UIM_PWR	NC	—	unused	
9	GND	GND	—	the ground	
10	UIM_DATA	RESERVED	IO	Use the transparent version; suspended.	
11	REFCLK-	RESERVED	DI	Use the transparent transmission version; keep the object suspended.	
12	UIM_CLK	RESERVED	IO	Use the transparent transmission version; keep the object suspended.	
13	REFCLK+	RESERVED	DO	Use the transparent transmission version; keep the object suspended.	
14	UIM_RESET	NC	—	unused	
15	GND	GND	—	the ground	
16	UIM_VPP	NC	—	For internal use; keep suspended.	
17	RESERVED	NC	—	For internal use; keep suspended.	
18	GND	GND	—	the ground	
19	RESERVED	PPS	DI	GPS timing input	Can be suspended
20	W_DISABLE#	NC	—	For internal use; keep suspended.	
21	GND	GND	—	the ground	
22	PERST#	NRESET	DI	Reset Control Pin	High-level reset
23	PERn0	RESERVED	DI	Reserved; externally suspended	
24	3.3Vaux	VCC_3V3	PI	3.3 V DC Main Power Input	
25	PERp0	NC	—	unused	
26	GND	GND	—	the ground	
27	GND	GND	—	the ground	
28	1.5V	NC	—	unused	
29	GND	GND	—	the ground	
30	SMB_CLK	NC	—	For internal use; keep suspended.	
31	PETn0	RESERVED	DO	Reserved; externally suspended	

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number	MiniPCIe Pin Definition	E106-xxxG27P2 Pin Definitions	I/O attribute	functional description	remarks
32	SMB_DATA	NC	—	For internal use; keep suspended.	
33	PETp0	NC	—	unused	
34	GND	GND	—	the ground	
35	GND	GND	—	the ground	
36	USB_D-	RESERVED	IO	Use the transparent transmission version; keep the object suspended.	
37	GND	GND	—	the ground	
38	USB_D+	RESERVED	IO	Use the transparent transmission version; keep the object suspended.	
39	3.3Vaux	VCC_3V3	PI	3.3 V DC Main Power Input	
40	GND	GND	—	the ground	
41	3.3Vaux	VCC_3V3	PI	3.3 V DC Main Power Input	
42	LED_WWAN#	RX_ON	DO	GPIO3 connected to SX1303	
43	GND	GND	—	the ground	
44	LED_WLAN#	TX_ON	DO	GPIO5 connected to SX1303	
45	RESERVED	SX_SCK	DI	SPI clock signal input	
46	LED_WPAN#	CFG_ON	DO	CFG indicator – connect to onboard LED.	
47	RESERVED	SX_MISO	DO	SPIpresentation of information	
48	1.5V	NC	—	unused	
49	RESERVED	SX_MOSI	DI	SPIdata-in	
50	GND	GND	—	the ground	
51	RESERVED	SX_CSN	DI	SPI Chip Select Signal Input	
52	3.3Vaux	VCC_3V3	PI	3.3 V DC Main Power Input	

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4.Mechanical Dimensions and Interface Specifications

4.1. Module Mechanical Dimensions

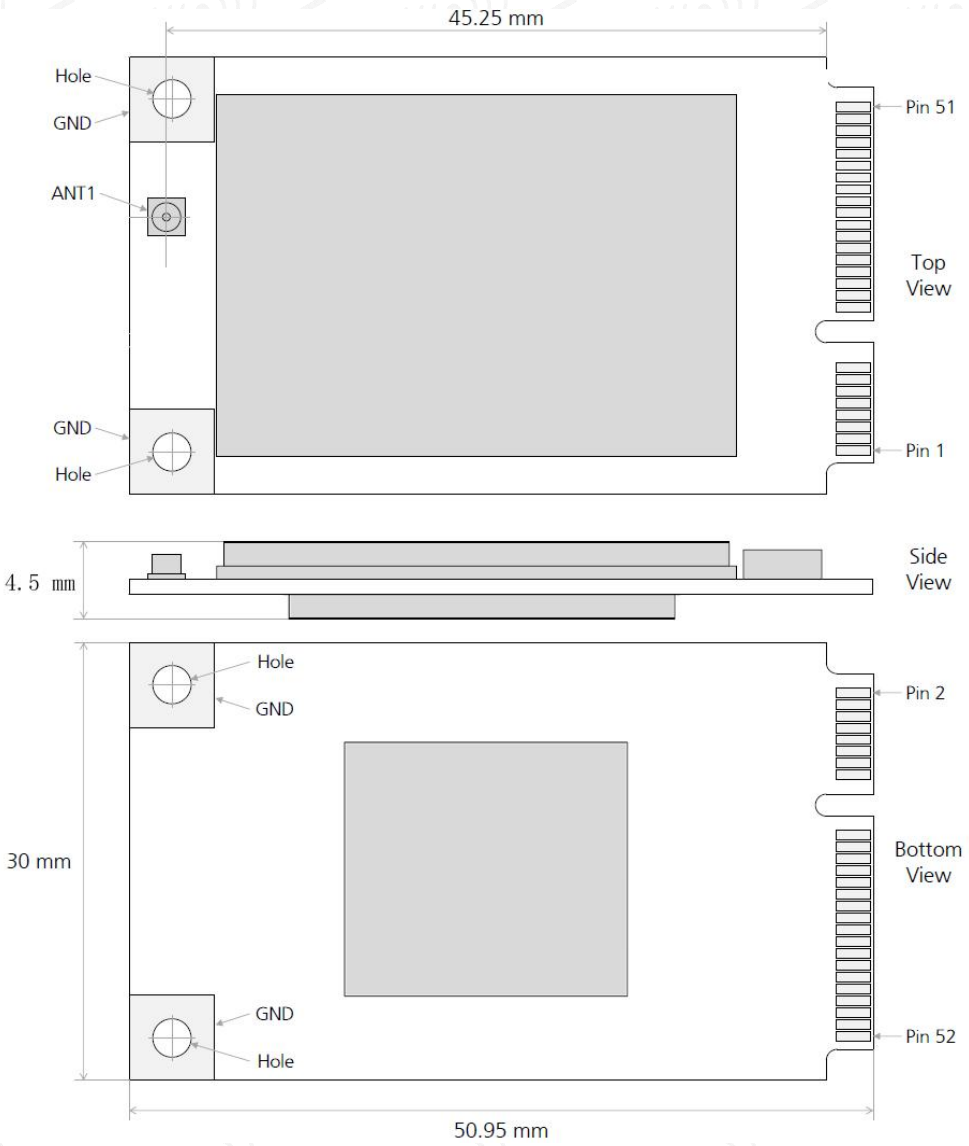


Figure 3: E106-xxxG27P2 module external dimensions

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4.2. PCIe Connector Interface

All compliant PCI Express Mini Card connectors can be used with this module; an example is the Molex 679100002 connector shown in the figure below.

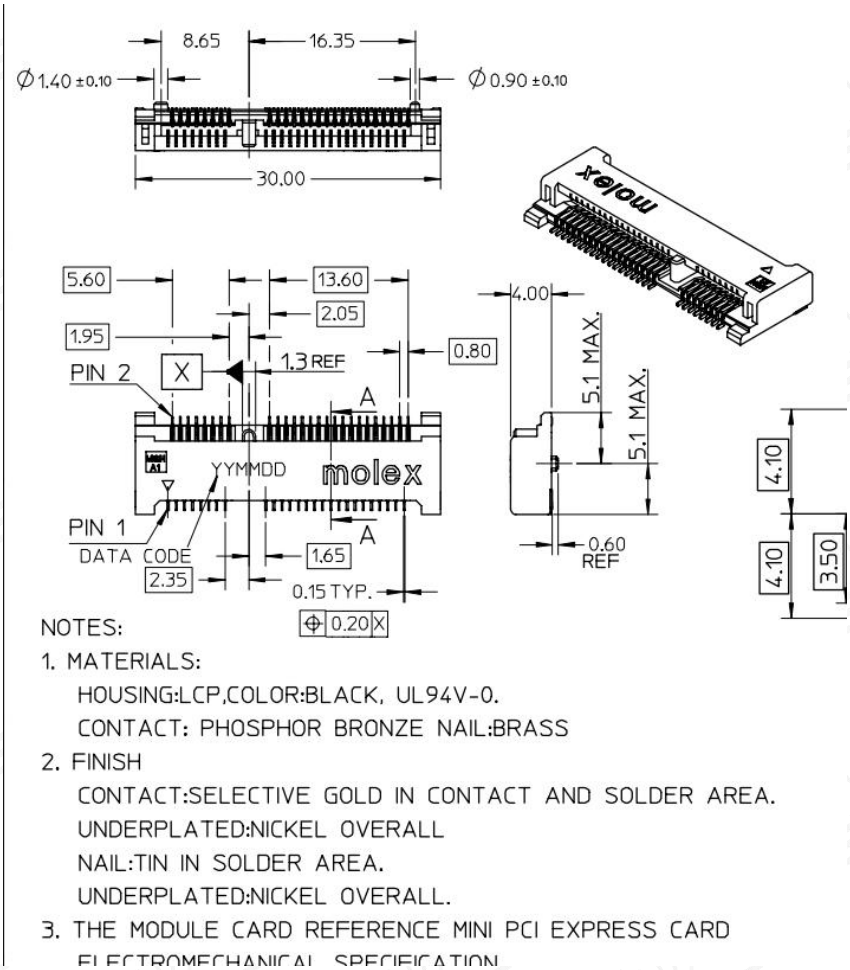


Figure 4: Mini PCI Express connector

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4.3. Antenna Interface

The module's antenna connection socket uses an I-PEX Gen 1 interface. Figure 3 shows the dimensional specifications of the RF connection socket, with measurements in mm.

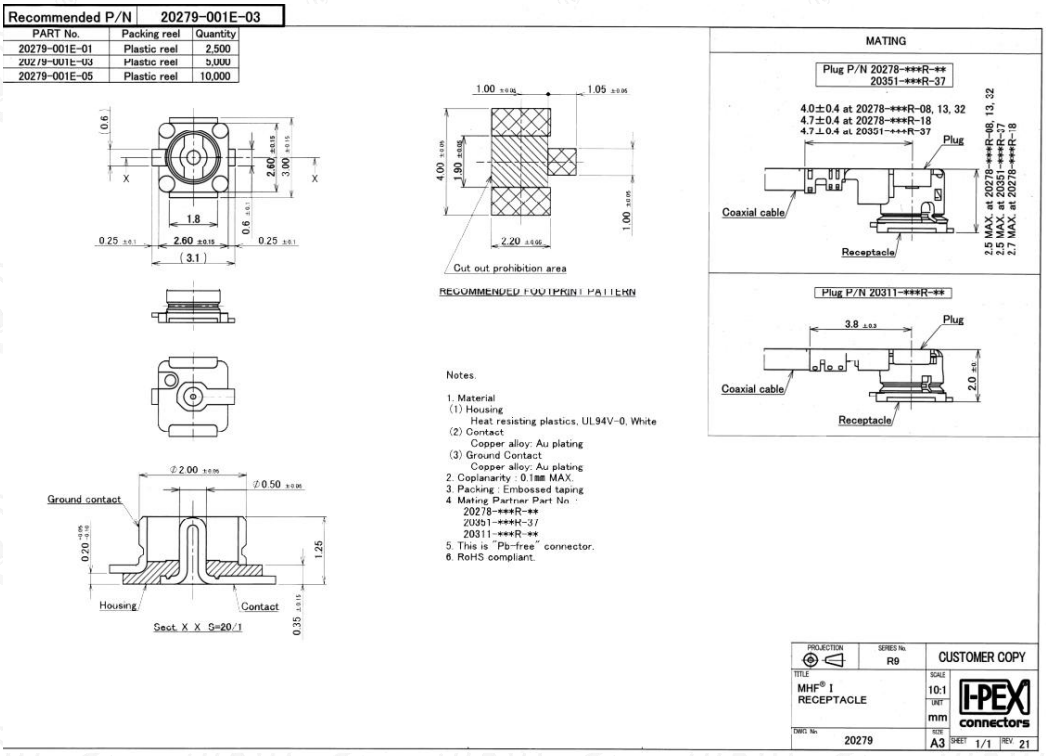


Figure 5: RF connector dimensions

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5. Internal Connections

The figure below shows the internal connection diagram for the E106-xxxG27P2 (SX1303); it is provided for reference.

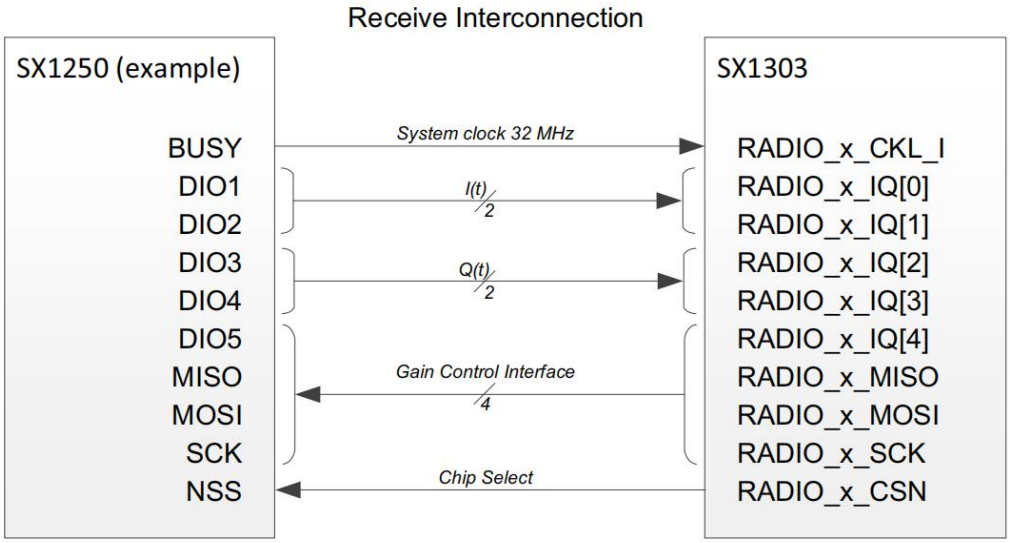


Figure 6: Received Connection Schematic Diagram

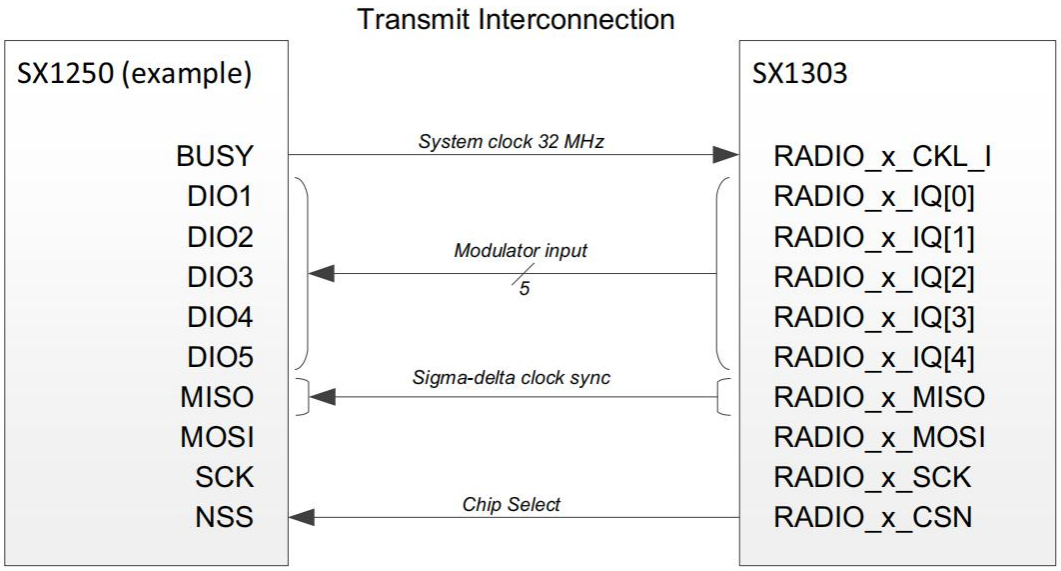


Figure 7: Data Transmission Schematic Diagram

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6. Reference Design

The E106-xxxG27P2 (SX1303) connects to the main controller via an SPI interface and powers the module using a DC-DC converter; users may modify this configuration as needed.

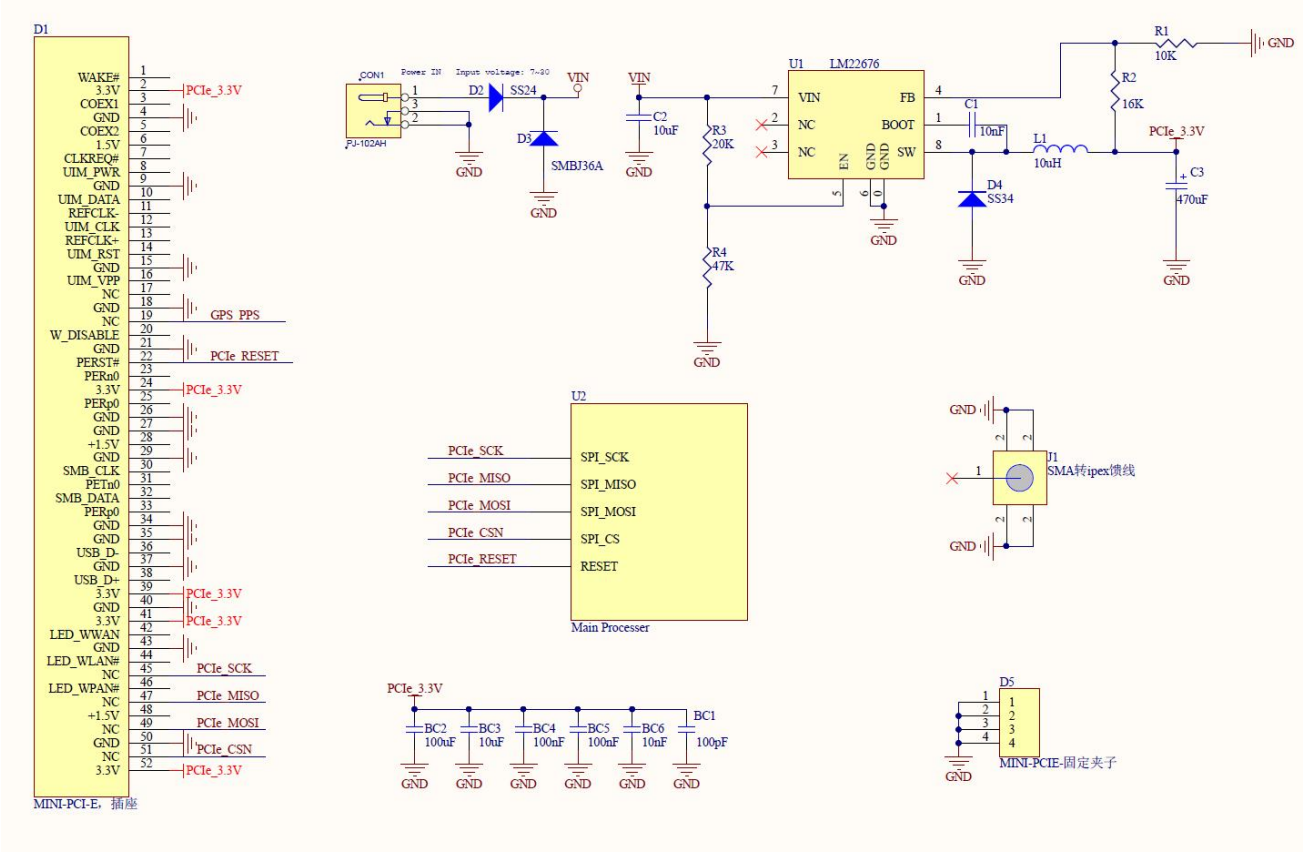


Figure 8: E106-xxxG27P2 (SX1303) Module Reference Design

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7. Hardware Design

- It is recommended to power this module using a DC regulated power supply with as low a ripple factor as possible; the module must be reliably grounded.
- Please ensure that the positive and negative power terminals are connected correctly; incorrect wiring may cause permanent damage to the module.
- Please check the power supply to ensure it operates within the recommended voltage range; exceeding the maximum voltage may cause permanent damage to the module.
- Please check the power supply stability – the voltage should not experience significant or frequent fluctuations;
- When designing the power supply circuit for a module, it is often recommended to reserve a margin of at least 30% to ensure long-term stable operation of the entire system;
- The module should be positioned as far as possible away from components that generate significant electromagnetic interference, such as power supplies, transformers, and high-frequency traces;
- High-frequency digital traces, high-frequency analog traces, and power traces must be routed away from beneath the module; however, if routing must indeed pass beneath the module – assuming the module is soldered to the Top Layer – a ground plane (full copper fill with proper grounding) must be laid on the Top Layer at the module's contact area; this ground plane should be placed as close as possible to the module's digital section, with the actual routing performed on the Bottom Layer.
- It is incorrect to place or solder a module on the Top Layer, or to route traces arbitrarily on the Bottom Layer or any other layer; such practices can adversely affect the module's stray signals and reception sensitivity to varying degrees.
- If there are components around the module that generate significant electromagnetic interference, this can greatly affect the module's performance; depending on the intensity of the interference, it is advisable to keep the module at an appropriate distance from such components. If feasible, appropriate isolation or shielding measures should be implemented.
- If the module is surrounded by traces that generate significant electromagnetic interference (e.g., high-frequency digital, high-frequency analog, or power supply traces), this can greatly impact the module's performance; depending on the severity of the interference, it is advisable to position the module at an appropriate distance from such traces. If feasible, appropriate isolation or shielding measures may be implemented.
- The antenna installation configuration has a significant impact on module performance; it is essential to ensure that the antenna is exposed and, ideally, oriented vertically upward;
- When the module is installed inside the housing, a high-quality antenna extension cable can be used to extend the antenna outside the housing;
- The antenna must never be installed inside a metal enclosure, as this will significantly reduce the transmission range.

8. Frequently Asked Questions

8.1 Inadequate transmission range

- When there is a linear communication obstruction, the communication range will correspondingly decrease;
- Temperature, humidity, and co-channel interference can increase the packet loss rate in communications;

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- Ground absorption and reflection of radio waves result in poorer testing performance when measurements are taken near the ground;
- Seawater has an exceptionally strong ability to absorb radio waves; therefore, coastal testing conditions are unfavorable.
- When a metallic object is located near the antenna or when the antenna is placed inside a metal enclosure, signal attenuation can be severe;
- Incorrect power register settings or an excessively high airspeed setting (the higher the airspeed, the shorter the range);
- At room temperature, when the power supply voltage is lower than the recommended value, the output power decreases as the voltage decreases;
- Poor antenna-module matching or inherent antenna quality issues.

8.2 Module is prone to damage

8.3 Excessively high bit error rate

- If there is nearby co-channel signal interference, move away from the interference source or change the frequency or channel to avoid the interference;
- An inadequate power supply can also cause display corruption; therefore, it is essential to ensure the reliability of the power supply.
- Poor quality or excessively long extension cables or feeder cables can also lead to a high bit error rate.

Revision History

edition	Revision Date	revision note	Maintainer
1.0	2026-9-10	Initial Version	Hao

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