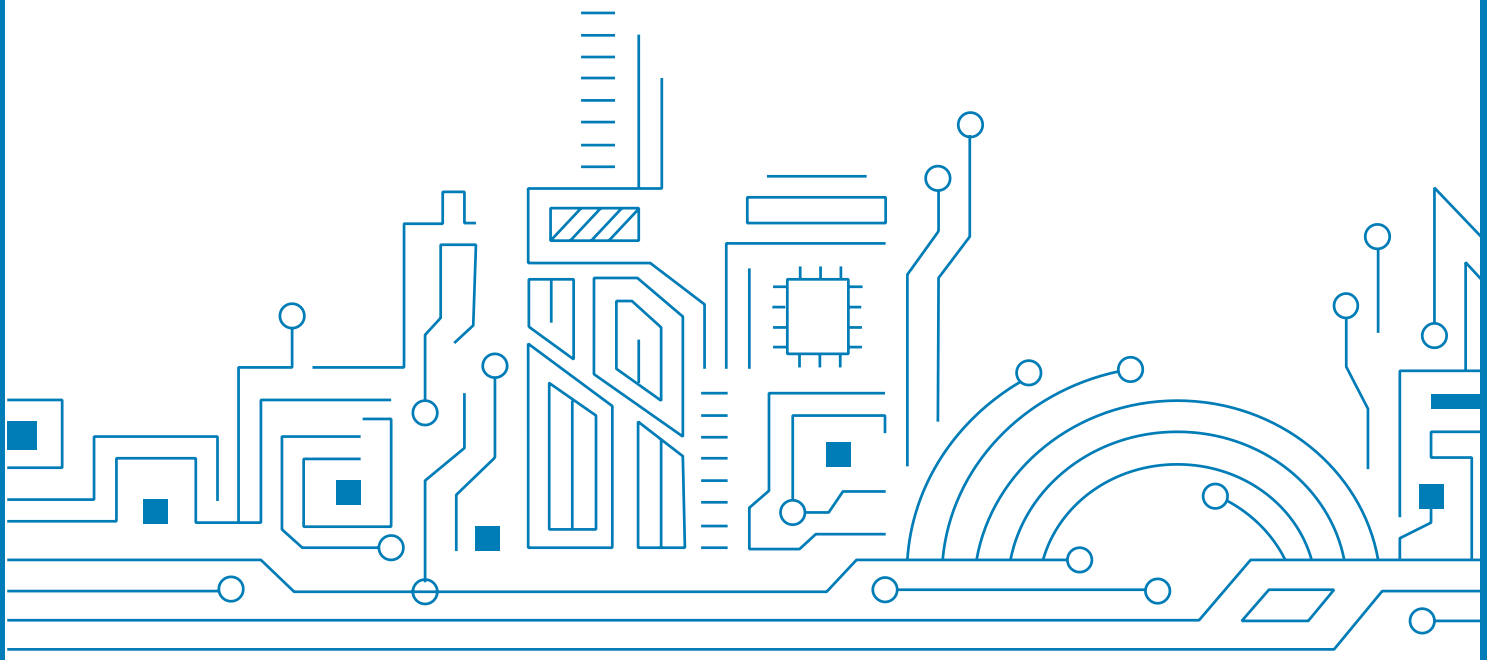
# CYNOSURE III GNSS Chip

# HD8040 Series

Datasheet V1.9



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# 1 SYSTEM OVERVIEW

## 1.1 General Description

ALLYSTAR HD8040 series is highly integrated GNSS receiver chip. It is the World's 1st multi-band multi-system SoC chip which supports BDS-3 (BeiDou Navigation Satellite System 3). Besides, it is capable of tracking all global civil navigation systems (BDS, GPS, GLONASS, Galileo, IRNSS, QZSS and SBAS) in all bands (L1, L2, L5, L6).

HD8040 series is based on the state of art CYNOSURE III architecture, integrating multi-band multi-system GNSS RF and baseband. This newly designed architecture makes this single chip achieve sub-meter level position accuracy without correction data from ground-based augmentation station and higher sensitivity, greater for improved jam resistance and multipath, provide a highly robust service in complicated environment.

An intelligent power management unit is built in the SoC chip. With the help of high efficient DCDC converter and high PSRR (Power Supply Rejection Ratio) linear regulators, HD8040 series achieves not only excellent power consumption performance but also good power supply noise immunity. A 12bit ADC, Low Voltage Detection (LVD) and Power-on Reset (POR) are implemented to monitor the main domain, the backup domain I/O and core supply voltage. There are five low power modes provided according to different application requirements.

Meanwhile, HD8040 series is equipped with a hardware cryptographic engine (CRYPTO) supporting various encryption/decryption standard (AES/DES/SM4) to protect sensitive data such as position information during data exchange. It ensures the security of positioning and navigation information.

It can be widely used in mobile phones, wearable devices, unmanned aerial vehicle, vehicle management, unmanned driving, car navigation, marine navigation, GIS data acquisition, engineering survey, and other fields.

## 1.2 Features

- Concurrent reception of multi-band multi-system satellite signals
- Supports all civil GNSS signals
- Supports BDS-3 signal: B1C, B2a and B3I
- Low power consumption
- Built-in AES/DES/SM4 data encode/decode cryptographic engine
- ARM Cortex-M4F processor with cache controller
- Smart jammer detection and suppression


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## 1.3 Block Diagram

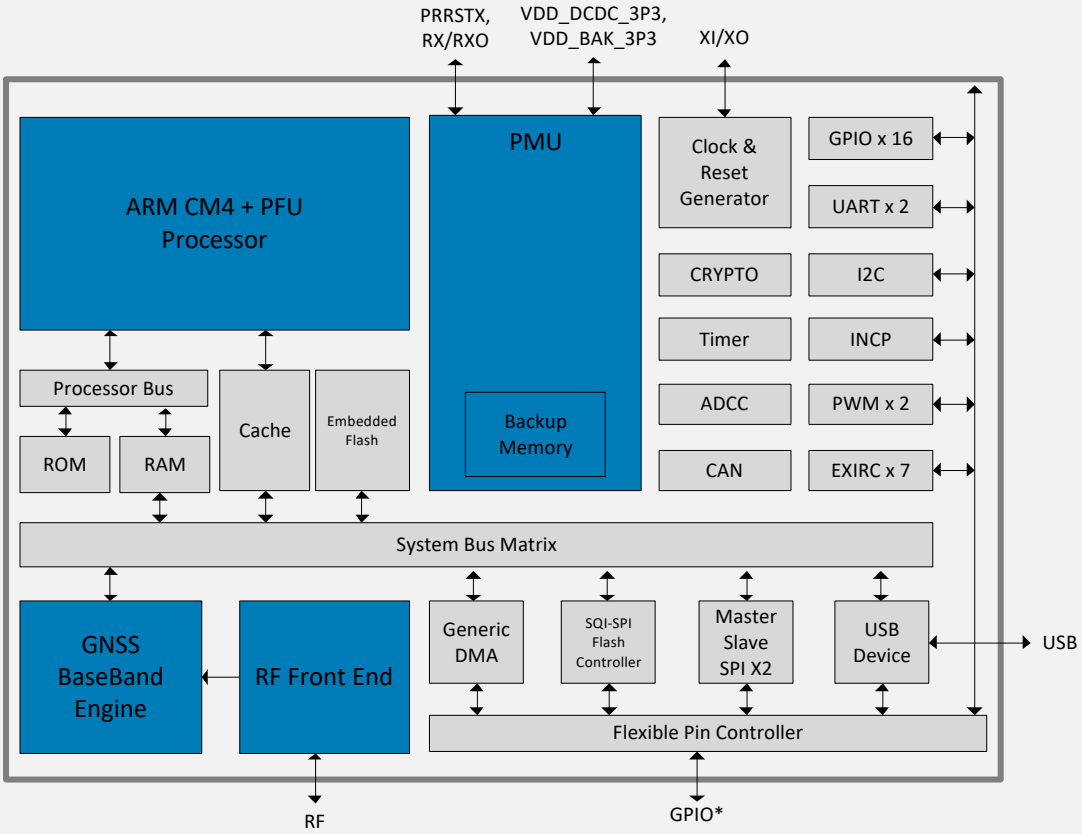



Figure 1 Block diagram


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## 1.4 Specifications

**Table 1 Specifications**

| Parameter | Specification | |
|---|---|---|
| GNSS engine | Cynosure III GNSS engine<br>Total 136 channels & DSP accelerator | |
| GNSS reception | GPS/QZSS: L1 C/A, L1C, L2C, L5, L6 | |
| | BDS: B1C, B1I, B2a, B2I, B3I | |
| | GLONASS: L1, L2 | |
| | Galileo: E1, E5, E6 | |
| | IRNSS: L5 | |
| | SBAS: WAAS, EGNOS, MSAS, GAGAN, SDCM | |
| Update rate | GNSS | 20Hz Maximum |
| Position accuracy [1] | GNSS | 2.5m CEP |
| | SBAS | 2.0m CEP |
| | D-GNSS | <1.0m CEP |
| Velocity & Time accuracy | GNSS | 0.1m/s CEP |
| | SBAS | 0.05 m/s |
| | D-GNSS | 0.05 m/s |
| | 1PPS | 25 ns |
| Time to First Fix(TTFF) [1] | Hot start | 1 sec |
| | Cold start | 28 secs |
| Sensitivity [1] | Cold start | -148dBm |
| | Hot start | -155dBm |
| | Reacquisition | -158dBm |
| | Tracking & navigation | -162dBm |
| GNSS Operating limit | Velocity | 515m/s |
| | Altitude | 18,000m |
| **Others** | | |
| Safety supervision | Antenna short circuit protection | |
| | System clock stop detection | |
| | Low voltage detection | |
| Clock | Main clock oscillator | TCXO or Crystal (16~40MHz) |
| | Sub clock oscillator | 32.768kHz Crystal (optional) |
| Serial communication interface | USB (FS, 12Mbps) | 1 |
| | UART | 2 |
| | SPI (Master/Salve Mode) | 2 |
| | SQI (1-bit/4-bit Master Mode) | 1 |
| | $I^2C$ | 1 |
| Peripheral | PWM | 4 |
| | INCP | 2 |
| | External interrupt | 7 |
| | Digital I/O | 16 |


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| Parameter | Specification | |
|---|---|---|
| Synchronization | Time synchronization | 1 |
| | Frequency synchronization | 1 |
| ADC | Analog Input Channel | 2 |
| | ENOB | 12 bit |
| Cryptographic Engine | AES / DES / TDES / SM4 | |
| Protocol | NMEA 0183 Protocol Ver. 4.00/4.10,<br>Cynosure GNSS Receiver Protocol | |
| Operating condition | Main voltage | 1.8 ~ 3.6V |
| | Digital I/O voltage | 1.8~ 3.6V |
| | Backup voltage | 1.62~3.63V |
| Power consumption | GPS+QZSS, L1 band | 34mA [2] |
| | GNSS, L1+L5 band | 40mA [3] |
| | Data backup mode | 9uA [4] |
| Operating temperature | -40°C to +85°C | |
| Storage temperature | -40°C to +125°C | |
| Package | QFN40 5.0mm X 5.0mm | |
| | WLCSP 3.0mm X 3.0mm | |
| Certification | RoHS & REACH | |

* *[1] Demonstrated with a good external LNA*
* *[2] Open sky conditions, GPS+QZSS, L1 band, 16 tracked Satellites*
* *[3] Open sky conditions, GPS+BDS+GLONASS+Galileo, L1+L5 band, 32 tracked Satellites*
* *[4] Condition: AVD33BAK=3.3V@Room Temperature; All Pins Open.*


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## 1.5 HD8040 series product

HD8040 series P/N, GNSS reception and features:

**Table 2 GNSS reception table**

| P/N | Mode | GPS/QZSS | | | | | BDS | | | | | GLONASS | | Galileo | | | IRNSS | SBAS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | L1CA | L1C | L2C | L5 | L6 | B1I | B1C | B2I | B2a | B3I | L1 | L2 | E1 | E5 | E6 | L5 | L1 |
| HD8040 | - | ● | - | - | - | - | ● | - | - | - | - | - | - | - | - | - | - | ● |
| HD8040D | A(default) | ● | ● | - | ● | - | ● | ● | - | ● | - | ● | - | ● | ● | - | - | ● |
| | B[1] | ● | ● | ● | - | - | ● | ● | ● | - | - | ● | ● | ● | - | - | - | ● |
| | C[2] | ● | ● | - | - | ● | ● | ● | - | - | ● | ● | - | ● | - | ● | - | ● |
| HD8041 | - | ● | ● | - | - | - | ● | ● | - | - | - | ● | - | ● | - | - | - | ● |
| HD8041D | - | ● | ● | - | ● | - | ● | ● | - | ● | - | ● | - | ● | ● | - | ● | ● |
| HD8040DW | - | ● | ● | - | ● | - | ● | - | - | ● | - | - | - | ● | ● | - | - | ● |

**Table 3 Key features**

| P/N | MODE | Key features |
|---|---|---|
| HD8040 | - | GPS+QZS+BDS, L1, super low power consumption |
| HD8040D | A(default) | GPS+QZS+BDS+GAL+GLO, L1+L5, D-GNSS (GNSS) for sub-meter accuracy |
| | B[1] | GPS+QZS+BDS+GAL+GLO, L1+L2, D-GNSS (GNSS) for sub-meter accuracy |
| | C[2] | GPS+QZS+BDS+GAL+GLO, L1+L6, D-GNSS (GNSS) for sub-meter accuracy |
| HD8041 | - | GPS+QZS+BDS+GAL+GLO, L1 |
| HD8041D | - | GPS+QZS+BDS+GAL+GLO+IRNSS, L1+L5, D-GNSS (GNSS) for sub-meter accuracy |
| HD8040DW | - | GPS+QZS+BDS+GAL, L1+L5, D-GNSS (GNSS) for sub-meter accuracy, GNSS raw data output. |

* *[1] For standalone application, it supports to use MODE A instead of MODE B.*
* *[2] Adopting corrections broadcasted from satellites to improve accuracy (supported by specific firmware)*
* *HD8040 series P/N within the letter "S" means to support embedded AES/DES/SM4 data encryption. (e.g. HD8040S, HD8041S)*


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# 2 NAVIGATION SUBSYSTEM

## 2.1 Block Diagram

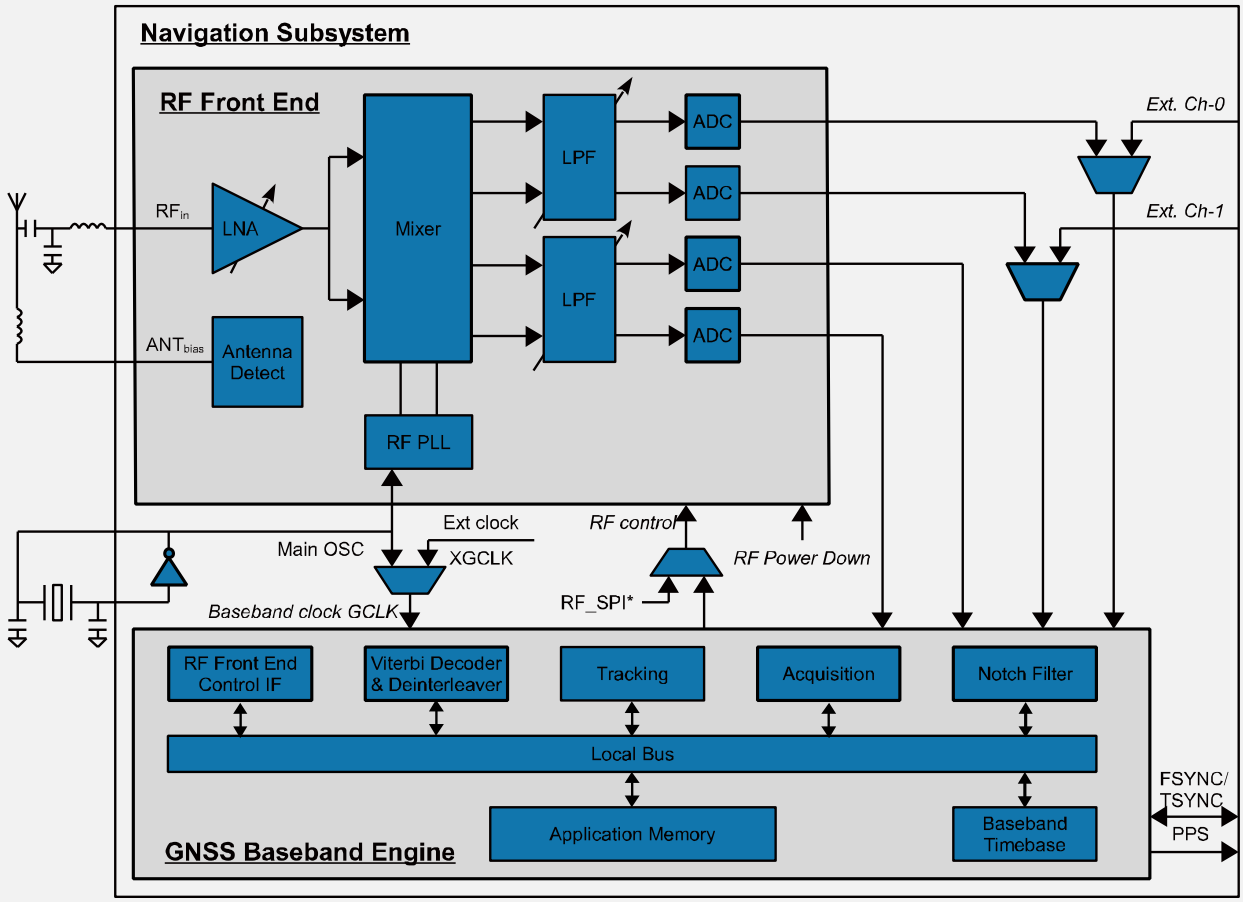



Figure 2 Navigation block diagram

## 2.2 RF Frontend

The wideband RF Frontend (RFFE) can concurrently receive L1 and L5 bands (or L1 and L2 bands) RF signals from external active or passive antenna and down-converts it to the digital IF signals. The IF signals are then processed by the GNSS baseband engine.

### 2.2.1 RF Features

- L1 band single-frequency mode
  - » Low positioning accuracy/speed
  - » For extremely low-power applications
  - » Supports:
    - GPS L1 C/A + Galileo E1 + QZSS L1
    - BDS B1I
    - GLONASS L1
- L1 band multi-frequency mode


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  - » Medium positioning accuracy/speed
  - » For most consumer/automotive applications
- L1+L2 band mode
  - » High positioning accuracy/speed
  - » For high precision and professional applications
- L1+L5 band mode
  - » High positioning accuracy/speed and best anti-multipath performance
  - » For high precision and professional applications
- L1+L6 band mode
  - » High positioning accuracy/speed and best anti-multipath performance
  - » For high precision and professional applications
  - » Improving position accuracy via correction terms (SSR-Type) broadcasted from satellites in L6 band
- Fractional-N local oscillator synthesizer of low phase noise
- L1/L2/L5 wideband Low Noise Amplifier (LNA) with single RF input
- Automatic Gain Control (AGC)
- 8-bit high-speed ADC
- Active Antenna Detection
- Can be shut down independently for power saving
- Allow bypass of each IF channel and replacement by external RF front end
- Support direct output of each IF channel for analysis or usage by external baseband device
- Receiver noise figure:
  - » 2.5dB (L1 band mode)
  - » L1: 2.8dB and L2/L5: 3.3dB (L1+L2 or L1+L5 band mode)


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## 2.3 GNSS Baseband Engine

The baseband engine acquires up to 96 and tracks up to 40 satellite signals simultaneously. It has dedicated circuit to accelerate the decoding of the tracked signal. A full featured firmware is available by request.

### 2.3.1 Baseband Engine Features

- Supports various modulation scheme and PRN (pseudorandom noise) code generator to handle all existed GNSS systems
- Supports various combinations of GNSS system and multi-band to achieve optimized solution for global or local area
- Adjustable clock frequency with clock-gating to baseband engine to achieve lower power consumption
- GNSS Decode engines: Stream/block Viterbi, CRC (cyclic redundancy codes), LDPC (low density parity check)
- Supports Multi-PPS with adjustable pulse width for various applications
- Smart adaptive anti-jamming filter
- Supports external Time and Frequency aiding signal
- Rich set of GNSS Firmware, examples:
  - Dual frequency + multi-system
  - Full L1-band for GPS + BDS + GLONASS + Galileo
  - Dual-band RTK (Real-time Kinematic) solution


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# 3 MCU SUBSYSTEM

## 3.1 ARM Processor System

HD8040 series is powered by ARM Cortex-M4F processor that runs up to 172MHz (without co-exist of USB). Together with the 4-way associative data/instruction cache, HD8040 series can deliver high processing power to many application programs. The processor system includes:

- ARM Cortex-M4F
- Integrated nested vectored interrupt controller (NVIC)
- Floating Point Unit (FPU)
- ROM
- RAM
- Embedded Flash

## 3.2 Clock Generator and Supervisor

The clock generator generates a wide range of different operating clock frequencies according to the requirement of different subsystems. It supports the critical operation of HD8040 series even in absence of the external oscillator clock. It achieves this by switching to the built-in oscillator clock automatically when the clock supervisor detects the loss of the external clock source for a certain period.

## 3.3 Timer

In addition to the ARM processor's timer, the chip has two more programmable 32/16-bit Timers for general purpose. These Timers support three modes: free-running, periodic and one-shot.

## 3.4 DMA Controller

Direct Memory Access Controller (DMAC) allows data movement among memory and most communication interfaces without CPU intervention. Furthermore, cyclic redundancy codes (CRC) can be generated simultaneously during the data movement.

## 3.5 Watchdog

The Watchdog timer can prevent deadlock. In normal operation, firmware resets the Watchdog timer at regular interval before timer overflow occurs. Otherwise, a watchdog reset will be generated.


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## 3.6 Serial Communication Interfaces

### 3.6.1 UART

HD8040 series has 2 Universal Asynchronous Receiver / Transmitter (UART) interfaces. The features of each UART include:

- Two channels with full duplex operation
- Range: 1200 bps ~ 460800 bps, the default baud rate is 115200 bps
- Programmable serial interface
- Supports ISO/IEC7816
- Hardware flow control signals shared for UART0/1

### 3.6.2 $I^2C$

$I^2C$ interface is a serial input & output port, and it can be operated in master or slave mode.

- 7-bit and 10-bit addressing modes
- Speed: 100Kps standard mode and 400Kps fast mode
- Supports DMA data transmission in master mode

### 3.6.3 SPI

The Serial Peripheral Interface (SPI) interface allows for the connection of external devices with a serial interface. The SPI supports both the common SPI protocol and the $I^2S$ audio protocol (output only). It can be operated in master or slave mode.

- SPI-features
  - » Full-duplex synchronous communication
  - » Configurable slave/master mode
  - » The frequency of SPICK clock is programmable
- $I^2S$-features
  - » The $I^2S$ clock direction is programmable
  - » The $I^2S$ (SPICK) clock can be driven by the external audio DAC

### 3.6.4 SQI

SQI supports both 1-bit and 4-bit mode interface (master mode only). It can be functioned as generic SQI/SPI interface or Serial Flash Controller. When it acts as a SQI/SPI flash controller, HD8040 series can access the serial flash area as if it was a regular memory area. It supports direct execution of program code stored in serial flash area.

In addition, the module can be set to communicate with general SQI/SPI slave device.

- Set to 1/4 wires mode
- The frequency of SQICK clock is programmable
- The MSB/LSB data transfer is programmable
- Up to 3 programmable interrupt events
- Dedicated 8 words data buffer for data transfer
- Two dedicated areas for non-prefetch and prefetch operation


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### 3.6.5 USB

USB version 2.0 FS compatible interface (device only) can be used for communication as an alternative to the UART or other communication interfaces.

- Supports USB 2.0 full speed
- USB plug-in detection via External Interrupt 7
- Full Speed: 12Mbps
- Supports Windows XP/7/8/10 OS®, Android, Linux

## 3.7 Time Synchronization Interfaces

### 3.7.1 PPS

An extremely accurate time pulse signal “Pulse Per Second” (PPS) generated by GNSS can be output to designated pin. It is useful in many timing applications. The pulse interval can be adjusted by changing internal parameters.

### 3.7.2 FSYNC / TSYNC

HD8040 series supports the use of external aiding signals (precise clock signal FSYNC or timestamp signal TSYNC) to correct its local real-time drift with proper firmware. It reduces the search time in weak satellite condition, shortens the positioning time and improves the Time to First Fix (TTFF).

## 3.8 Other Peripherals

### 3.8.1 INCP

Input Capture (INCP) records a free-running timer value whenever specified edge of input signal is detected. As a result, duration between two specified events can be calculated. It can also be acted as event counter.

- Two independent channels with dedicated edge detection circuit
- Edge detection: rise, fall or both edges
- Interrupt is generated when timer wraps around or match desired value

### 3.8.2 PWM

Pulse Width Modulator (PWM) is a programmable waveform generator

- Two group of PWMs with two channels in each PWM group
- Two waveform outputs synchronized or not synchronized for each group
- Programmable width, phase, duty and polarity
- One-shot or continuous pulse format
- Waveform data can be updated by DMA so that complex waveform can be generated


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### 3.8.3 External Interrupts

External Interrupts (EXIRC) allows HD8040 series to interact with external device (e.g. host or user) by generating interrupt request to CPU upon detection of defined event.

- 7 independent interrupt requests, the eighth interrupt request is dedicated for USB plug-in detection
- 4 kinds of interrupt event: high level, low level, rise edge & fall edge
- Wake up the system from stop mode (high or low level only)

### 3.8.4 ADC

ADC controller measures external analog signals or internal power signal (main power and backup power). The measured value can be stored in backup memory automatically, or generating interrupt request to CPU when defined level is detected.

- Configurable input voltage range
- Single-end or Differential-end inputs
- Integrated internal temperature sensor
- Interrupt generation
- Data logging
- 1sec pulse period scan mode for power saving
- One shot scan mode

### 3.8.5 External I/O Port Configuration

HD8040 series supports up to 16 I/O pins. The resources include two types: dedicated and non-dedicated. The dedicated resources are defined to the I/O pins described in the following table, and the non-dedicated resources are assigned freely to any undefined I/O pin. Dedicated resources assignment has higher priority than non-dedicated resources.

- Dedicated resources: SQI, ADC analog input
- Non-dedicated resources: SPI, UART, $I^2C$, EXIRC, PWM, INCP, PPS, FSYNC, TSYNC.

**Table 4 Pins for dedicated resources**

| Dedicated resource | Pins |
|---|---|
| SQI | GPIO0~GPIO5 |
| Analog input | GPIO11, GPIO12 |


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### 3.8.6 Cryptographic Engine (CRYPTO)

HD8040 series is equipped with a hardware cryptographic engine (CRYPTO) supporting various encryption/decryption standard to protect sensitive data such as position information during data exchange. A secret 256-bit key can be programmed in HD8040 with protection features. Except the on-chip cryptographic engine, no software means can access the key.

It uses the AES, DES, TDES or SM4 algorithms complied with the following standards:

- Advanced Encryption Standard (AES) as defined by Federal Information Processing Standards Publication (FIPS PUB 197)
- Data Encryption Standard (DES) & Triple-DES (TDES) as defined by Federal Information Processing Standards Publication (FIPS PUB 46-3)
- Chinese block cipher standard SM4 encryption algorithm, formerly known as SMS4

In addition, the engine incorporates cryptographically secure True Random Number Generator (TRNG) & Pseudo Random Number Generator (PRNG) for random number generation.

- » Performs data encryption or decryption
- » Supports Electronic Codebook (ECB) or Cipher Block Chaining (CBC) mode
- » Supports DMA transfer with 8 x 32-bit depth for each input & output FIFO
- » Swaps input & output data on bit, byte or half-word level
- » AES, DES, TDES and SM4 algorithm
- » Random number generation


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# 4 POWER MANAGEMENT UNIT (PMU)

The Power Management Unit (PMU) has two independent power domains, the main and backup power domain. The backup power source is enabled to keep important data while the main power supply is off. Furthermore, PMU can control the power supply for the external TCXO oscillator and on-chip flash. The standalone backup supply provides a convenient way to keep valuable information even though the main supply is removed. Because PMU is working on backup domain, the chip cannot work without the backup supply.

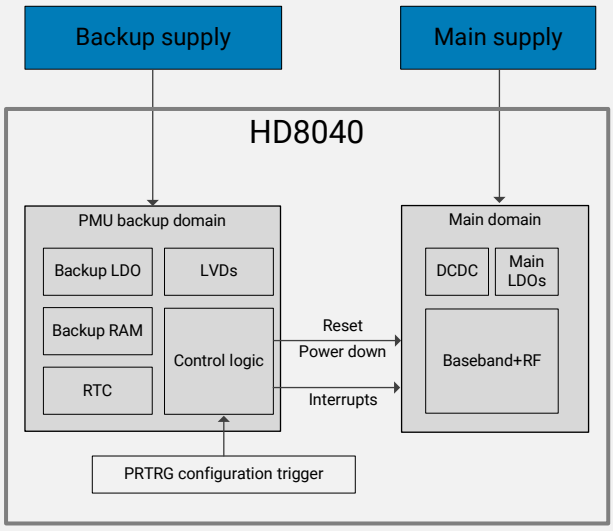



**Figure 3 Power Management Unit**

In order to achieve the best possible power performance, the device provides the following modes to lower the power consumption.

**Table 5 Application power mode**

| Power mode / Unit | Run | Sleep | Deep sleep | Data Retention | Data Backup | RTC |
|---|---|---|---|---|---|---|
| CPU | Enabled | Halted | Halted | Halted | Powered off | Powered off |
| Peripherals | Enabled | Enabled | Halted | Halted | Powered off | Powered off |
| RF | Enabled | Enabled | Powered off | Powered off | Powered off | Powered off |
| Oscillator | Enabled | Enabled | Powered off | Powered off | Powered off | Powered off |
| Main core voltage | Enabled | Enabled | Enabled | Retention voltage | Powered off | Powered off |
| RTC | Enabled | Enabled | Enabled | Enabled | Enabled | Enabled |
| System RAM data | Enabled | Enabled | Enabled | Retained | Powered off | Powered off |
| Backup RAM data | Enabled | Enabled | Enabled | Retained | Retained | Powered off |


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## 4.1 Control Logic Block

Control logic block generates an interrupt signal to reset or power down the Main domain by a custom signal from external input.

## 4.2 Low Voltage Detection

PMU has four Low Voltage Detectors (LVDs) to monitor internal operating voltage and supply voltage level to ensure device is operating in normal voltage.
When internal voltage (Main domain and Backup domain) level is lower than defined threshold voltage, the system will enter into reset state and stay in reset state until all internal voltage higher than threshold voltage level.
Supply voltages (Main supply and Backup supply) are also monitored. If the supply voltage is lower than the defined threshold, device will enter the reset state or jump into non-maskable interrupt service routine (NMI) in which some necessary operation such as power-down the device can be carried out.

## 4.3 Backup RAM

There is a 32K-byte RAM located in the Backup domain mainly used to keep the valuable data when main power is off.

## 4.4 RTC

The RTC is driven by its own 32.768 kHz oscillator and is, together with the 32KB backup RAM, powered by the backup supply voltage. When the engine is in a power-saving mode or the battery is low, part of the baseband switches off. The RTC provides a time reference as system powers up to secure a Hot-Start as long as backup power presents during main power off.

## 4.5 DCDC

HD8040 series integrates a DCDC converter in the Main power domain to convert AVD33DC1 to 1.35V for the main LDOs supply. The DCDC can be also configured to be linear regulation mode to reduce output voltage ripple. However, the power conversion efficiency is low in this linear regulation mode.

## 4.6 LDO

The HD8040 series PMU includes two types of LDOs regulator to provide power supply to the digital core.

- The Main LDO: converts DCDC output (1.35V) to a 1.1V core voltage for the main domain logic.
- The Backup LDO: converts AVDD33BAK to a 0.9V core voltage for the backup domain logic.


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## 4.7 Dynamic Voltage Frequency Scaling (DVFS)

To balance the maximum performance and power consumption of the chip, HD8040 series is equipped with DVFS function. When DVFS is enabled, core voltage will vary with the corresponding clock frequency.

## 4.8 Power on/off Sequence

HD8040 has two independent power domains (backup and main domain). In data backup mode (refer to Table 5 Application power mode), main power supply can be completely shut down for further power reduction for ultra-low power application.

### 4.8.1 Initial system power on

When both backup and main supply power on from their off state, external reset (PRRSTX) must be active and hold more than 5ms after both backup supply and main supply reach the minimum operating voltage. Initial system power on sequence is illustrated in Figure 4.

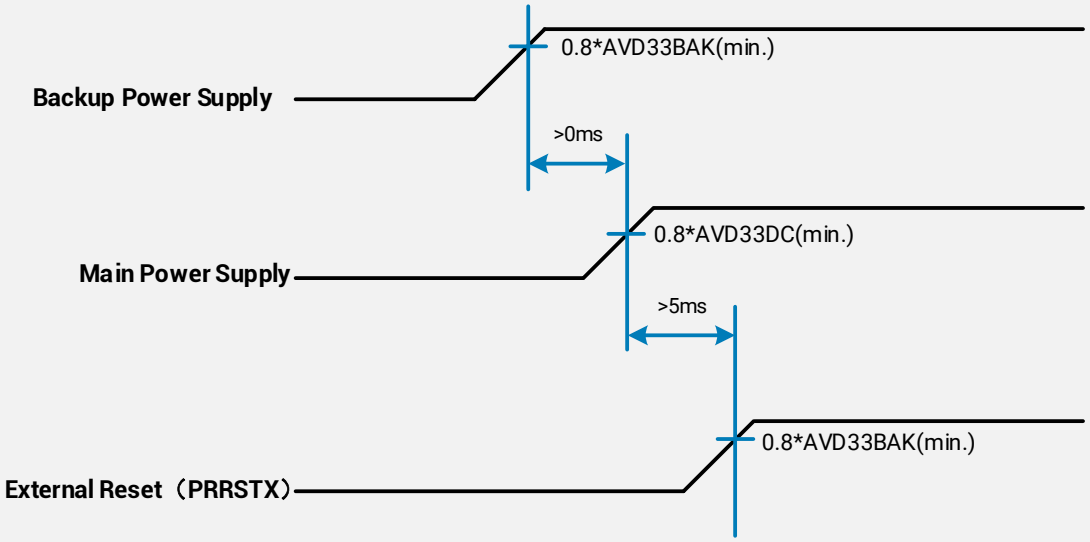



Figure 4 Initial system power on sequence

### 4.8.2 Main power supply off/on in application

If application intends to shut down main power supply (AVD33DC) while keep backup power supply (AVD33BAK) alive to save backup data, the following rules should be applied:
External reset (PRRSTX) must be active when main power supply is under power off. In this case, external reset must be hold active more than 5ms after main power supply resumes to minimum operating voltage. Main power on sequence in application is illustrated in Figure 5.


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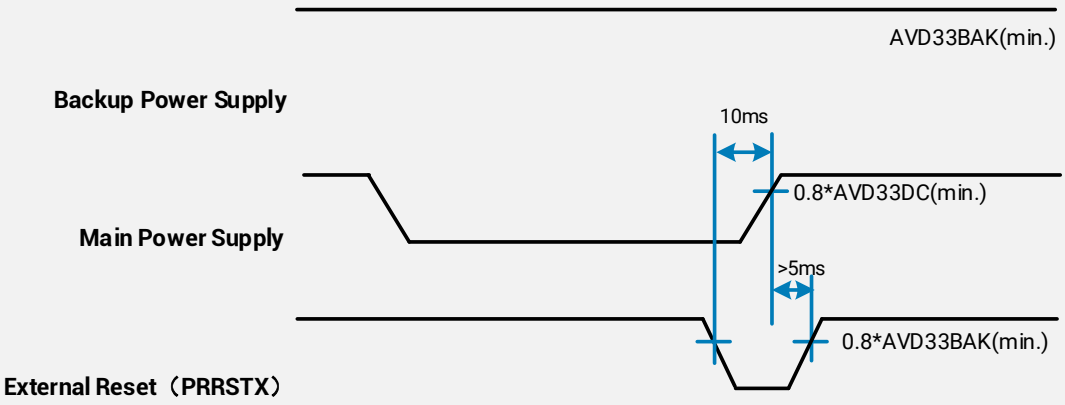



Figure 5 Main power on sequence


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# 5 FIRMWARE UPDATE

HD8040 series allows users to update the firmware in either User normal mode or BootROM command mode. Each mode supports two types of interfaces - UART and USB[1].

* *[1]: It is advised to install the HD-GNSS USB driver before first use.*

## 5.1 Mode Entry

The state of PRTRG pin during system power-up or external reset active (PRRSTX from “low” to “high”) determines HD8040 series operating mode.

### 5.1.1 User Normal Mode

Keeping PRTRG pin floating (Hi-z) during system power-up or the external reset (PRRSTX from “low” to “high”), system will enter User Normal Mode after internal system reset releases.

- If PRTRG is controlled by any host GPIO, that host GPIO MUST be set as an input pin without pull-up or pull-down resistance during PRRSTX = “low” or power up and keep the status for at least 50ms till PRRSTX releases or power up.

**Note:** If external pull-down resistor is needed at PRTRG pin, the pull-down value larger than 500Kohm is required. Otherwise, system maybe fail to enter User Normal Mode.

### 5.1.2 BootROM Command Mode

Drive PRTRG pin to "low" or connect PRTRG to GND directly (not by pull-down resistance) during system power-up or the external reset (PRRSTX from “low” to “high”), system will enter BootROM Command Mode after internal system reset release.

- If PRTRG is controlled by any host GPIO, that host GPIO MUST be set to output "0" during PRRSTX = “low” or power up and keep the status for at least 50ms till PRRSTX releases or power up.

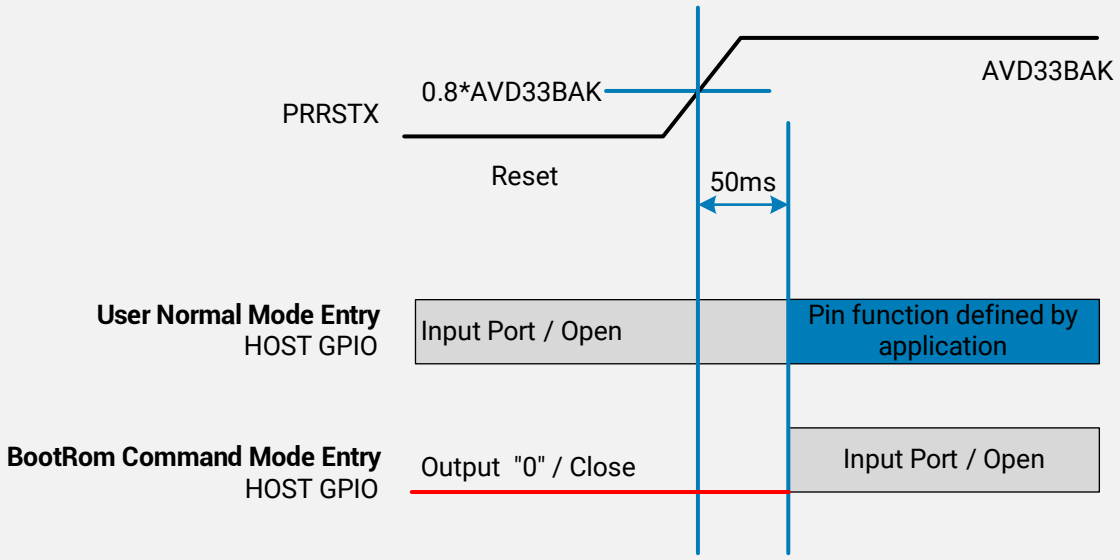



**Figure 6 Timing of mode entry with host controller**


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## 5.2 Update Firmware in User Normal Mode

When the GNSS firmware of HD8004 is running in User normal mode, the firmware can be updated by GNSS monitoring software "Satrack". For more information, please refer to *Satrack user manual*.

## 5.3 Update Firmware in BootROM Command Mode

If the flash memory of the chip has not been programmed, the chip will automatically enter BootROM Command Mode after power-up and reset, and then users can download firmware to the Flash memory. Users can also enter BootROM Command Mode manually to update firmware if necessary.

- The BootROM command mode provides a secure way to update firmware


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# 6 PIN DESCRIPTION

## 6.1 Package Pin Assignment

### 6.1.1 QFN40

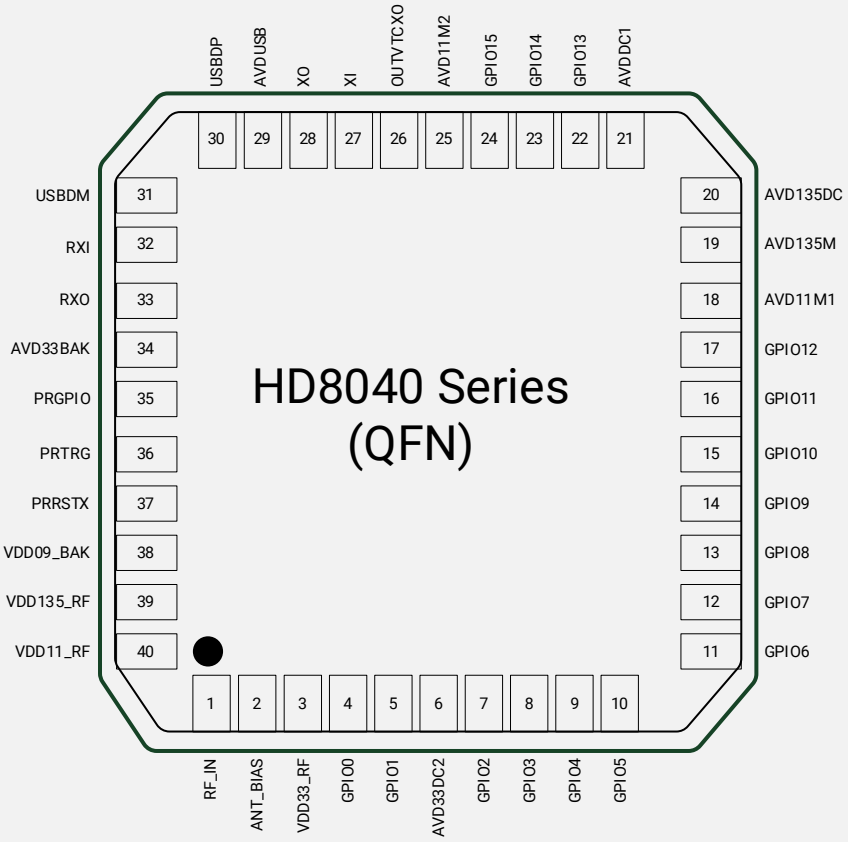



Figure 7 QFN40 (top view)


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### 6.1.2 WLCSP

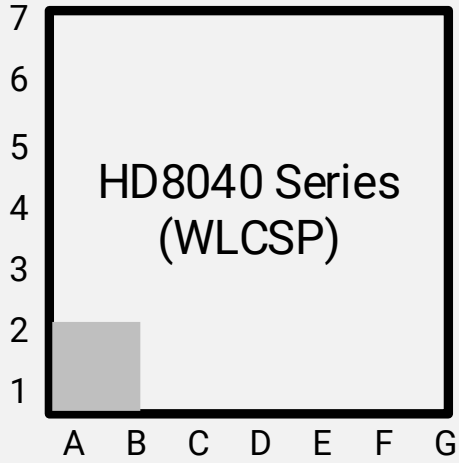



Figure 8 WLCSP (top side view)

**Table 6 WLCSP Ball map**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | GPIO5 | GPIO12 | GPIO11 | AVD11M1 | AVD135M | AVSDC1 | AVD135DC |
| **6** | GPIO14 | GPIO3 | GPIO4 | GPIO10 | AVSSM | AVSBAK | AVD33DC1 |
| **5** | VDD33_RF | GPIO2 | AVD33DC2 | GPIO8 | GPIO13 | AVD33BAK | AVSDC2 |
| **4** | VDD135_RF | VSS1 | GPIO1 | GPIO0 | GPIO9 | GPIO15 | OUTVTCXO |
| **3** | VDD11_RF | VSS_RF | VSS_A | PRRSTX | PRTRG | GPIO7 | XI |
| **2** | VSS_LNA | VSS_VCO | ANT_BIAS | PRGPIO | AVDUSB | GPIO6 | XO |
| **1** | RF_IN | NC | VDD09_BAK | USBDP | USBDM | RXI | RXO |
| | **A** | **B** | **C** | **D** | **E** | **F** | **G** |


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## 6.2 Pin Description

### 6.2.1 Power and Ground Pins

**Table 7 Power and ground pins**

| Symbol | No. | | Direction | Function |
|---|---|---|---|---|
| | QFN40 | WLCSP | | |
| VDD33_RF | 3 | A5 | Power In | 3.3V RF power supply<br>ANTDET input |
| AVD33DC2 | 6 | C5 | Power In | 3.3V Main Domain I/O power supply<br>GPIO0~GPIO12 I/O power supply |
| AVD11M1 | 18 | D7 | Power Out | 1.1V Main Domain core power supply<br>Main LDO output |
| AVD135M | 19 | E7 | Power In | DCDC Feedback<br>Main LDO input |
| AVD135DC | 20 | G7 | Power Out | DCDC output |
| AVD33DC1 | 21 | G6 | Power In | 3.3V DCDC input power supply<br>3.3V Main Domain I/O power supply<br>GPIO13~GPIO15 I/O power supply<br>LDO for TCXO input |
| AVD11M2 | 25 | -- | Power In | 1.1V Main Domain core power supply |
| OUTVTCXO | 26 | G4 | Power Out | 2.8V/1.8V LDO for TCXO output |
| AVDUSB | 29 | E2 | Power In | 3.3V USB power supply |
| AVD33BAK | 34 | F5 | Power In | 3.3V Backup Domain I/O power supply<br>Backup LDO input |
| VDD09_BAK | 38 | C1 | Power Out | 0.9V Backup Domain core power supply<br>Backup LDO output |
| VDD135_RF | 39 | A4 | Power In | 1.35V RF power supply<br>RF LDO input |
| VDD11_RF | 40 | A3 | Power Out | 1.1V RF power supply<br>RF LDO output |
| VSS_LNA | -- | A2 | GND | VSS for RF LNA |
| NC | -- | B1 | GND | Reserved |
| VSS_VCO | -- | B2 | GND | VSS for RF VCO |
| VSS_RF | -- | B3 | GND | VSS for RF 3.3V power |
| VSS_A | -- | C3 | GND | VSS for RF Analog Circuit |
| VSS1 | -- | B4 | GND | VSS for AVD11M1 |
| AVSSM | -- | E6 | GND | VSS for AVD135M |
| AVSBAK | -- | F6 | GND | VSS for AVD33BAK |
| AVSDC1 | -- | F7 | GND | VSS for AVD33DC* |
| AVSDC2 | -- | G5 | GND | VSS for AVD33DC* |


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### 6.2.2 Oscillator Pins

**Table 8 Oscillator pins**

| Symbol | No. | | Direction | Function | Description |
|---|---|---|---|---|---|
| | QFN40 | WLCSP | | | |
| XI | 27 | G3 | I | Main-Clock Oscillator, 16MHz ~ 40MHz crystal oscillation or TCXO input for RF and system operation. | XO input / TCXO input |
| XO | 28 | G2 | O | | XO output / 1.2V power supply output for 1.2V TCXO |
| RXI | 32 | F1 | -- | Sub-Clock Oscillator, 32.768kHz crystal oscillation clock for Real Time Clock and wakeup logic. | RXO input |
| RXO | 33 | G1 | -- | | RXO output |

### 6.2.3 RF Pins

**Table 9 RF pins**

| Symbol | No. | | Direction | Function | Description |
|---|---|---|---|---|---|
| | QFN40 | WLCSP | | | |
| RF_IN | 1 | A1 | I | RF input | -- |
| ANT_BIAS | 2 | C2 | Power Out | ANTDET output | Output power supply for external LNA or active antenna |

### 6.2.4 USB Interface Pins

**Table 10 USB interface pins**

| Symbol | No. | | Direction | Function | Description |
|---|---|---|---|---|---|
| | QFN40 | WLCSP | | | |
| USBDP | 30 | D1 | -- | USB differential data plus | USB 2.0 FS/LS I/O pins with internal Pull-up/down control |
| USBDM | 31 | E1 | -- | USB differential data minus | |

### 6.2.5 Reset and Mode Pins

**Table 11 Reset and mode pins**

| Symbol | No. | | Direction | Function | Description |
|---|---|---|---|---|---|
| | QFN40 | WLCSP | | | |
| PRGPIO | 35 | D2 | I/O | System GPIO | Multi-Function Port: System Power Enable, Pin unassociated Peripherals or GPIO |


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| | | | | | |
|---|---|---|---|---|---|
| PRTRG | 36 | E3 | I/O | System trigger | Multi-Function Port: System Wakeup Input, Pin unassociated Peripherals or GPIO |
| PRRSTX | 37 | D3 | Input | System reset | Active "L" with internal Pull-up resistor |


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### 6.2.6 General Purpose Pins

**Table 12 General purpose pins**

| Symbol | No. | | Direction | Description |
|---|---|---|---|---|
| | QFN40 | WLCSP | | |
| GPIO0 | 4 | D4 | I/O | MUX IO: General Purpose Input / Output (GPIO), SQI / SPI-1 signal selection (SQICX) |
| GPIO1 | 5 | C4 | I/O | MUX IO: GPIO, SQI / SPI-1 clock (SQICK) |
| GPIO2 | 7 | B5 | I/O | MUX IO: GPIO, SQI data 0 / SPI-1 Data In (SQI0) |
| GPIO3 | 8 | B6 | I/O | MUX IO: GPIO, SQI data 1 / SPI-1 Data Out (SQI1) |
| GPIO4 | 9 | C6 | I/O | MUX IO: GPIO, SQI data 2 (SQI2) |
| GPIO5[1] | 10 | A7 | I/O | MUX IO: GPIO, SQI data 3 (SQI3), UART 1 Serial Data Receive (UIN1) |
| GPIO6 | 11 | F2 | I/O | MUX IO: GPIO |
| GPIO7 | 12 | F3 | I/O | MUX IO: GPIO |
| GPIO8 | 13 | D5 | I/O | MUX IO: GPIO |
| GPIO9 | 14 | E4 | I/O | MUX IO: GPIO |
| GPIO10 | 15 | D6 | I/O | MUX IO: GPIO, Serial Wire Debug I/O (SWIO) |
| GPIO11[2] | 16 | C7 | I/O | MUX IO: GPIO, UART 0 Serial Data Receive (UIN0) |
| GPIO12[2] | 17 | B7 | I/O | MUX IO: GPIO, UART 0 Serial Data Transmit (UOUT0) |
| GPIO13 | 22 | E5 | I/O | MUX IO: GPIO, Serial Wire Debug Clock (SWCK), 1PPS(DEFAULT) |
| GPIO14[1] | 23 | A6 | I/O | MUX IO: GPIO, UART 1 Serial Data Transmit (UOUT1) |
| GPIO15 | 24 | F4 | I/O | MUX IO: GPIO |

* *[1] In BootROM command mode, GPIO5 and GPIO14 act as UART 1.*
* *[2] In BootROM command mode, GPIO11 and GPIO12 act as UART 0. When using GPIO11 and GPIO12 as input pins, please make sure the voltage level on GPIO11 and GPIO12 should not exceed the power supply voltage of AVDD33BAK.*


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# 7 ELECTRICAL CHARACTERISTICS

## 7.1 Absolute Maximum Rating

This product is equipped with the device to protect the inputs from high static voltage damages; however, it is advisable to take appropriate precautions to avoid application of any voltage higher than the specified maximum rated voltages. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device.

**Table 13 Absolute rating**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| AVD33DC1/AVD33DC2 | Power input for the main power domain | -0.5 | 3.63 | V |
| AVDUSB | USB power input | -0.5 | 3.63 | V |
| AVD33BAK | Power input for the backup power domain | -0.5 | 3.63 | V |
| AVD135M | Main LDO power input | -0.5 | 1.98 | V |
| VDD33_RF | 3.3V RF power input | -0.5 | 3.63 | V |
| VDD135_RF | 1.35V RF power input | -0.5 | 1.98 | V |
| $VI_{max}$ | Input voltage on the I/O pin | -0.5 | 3.63 | V |
| $T_j$ | Junction temperature | -40 | 125 | °C |
| $T_{storage}$ | Storage temperature | -65 | 150 | °C |
| $T_{solder}$ | Solder reflow temperature | -- | 260 | °C |
| $T_a$ | Ambient temperature | -40 | 85 | °C |

## 7.2 IO Type of Pin

**Table 14 IO type of pin**

| IO type | Pin name | Power domain | Description |
|---|---|---|---|
| IO-1 | PRRSTX | AVD33BAK | Chip Reset with internal Pull-up resistor, default “on” |
| IO-2 | PRTRG, PRGPIO | AVD33BAK | General I/O |
| IO-3 | GPIO0 ~ 12 | AVD33DC2 | General I/O |
| IO-4 | GPIO13 ~ 15 | AVD33DC1 | General I/O |
| OSC | RXI | AVD33BAK | 32.768kHz XO input |
| | RXO | AVD33BAK | 32.768kHz XO output |
| | XI | OUTVTCXO | 16~40MHz TCXO/XO input |
| | XO | OUTVTCXO | 16~40MHz XO output |
| RF_Signal | RF_IN | VDD11_RF | RF signal input |
| | ANT_BIAS | VDD33_RF | Power supply for the external active antenna |
| USB_Signal | USBDM | AVDUSB | USB 2.0 FS/LS I/O pins with an internal pull-up/pull-down controller |
| | USBDP | AVDUSB | |


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## 7.3 IO Characteristics

### 7.3.1 Type IO-1

**Table 15 Type IO-1**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{IZ}$ | Input leakage current | -- | -- | -- | +/-1 | uA |
| $V_{IH}$ | Input high voltage | -- | AVD33BAK*0. 7 | -- | AVD33BAK | V |
| $V_{IL}$ | Input low voltage | -- | 0 | -- | AVD33BAK*0.3 | V |
| $C_i$ | Input capacitance | -- | -- | -- | 10 | pF |
| $R_{PU}$ | Pull-up resistance | -- | 18 | -- | 84 | kOhm |

### 7.3.2 Type IO-2

**Table 16 Type IO-2**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{IZ}$ | Input leakage current | -- | -- | -- | +/-1 | uA |
| $V_{IH}$ | Input high voltage | -- | AVD33BAK*0.7 | -- | AVD33BAK | V |
| $V_{IL}$ | Input low voltage | -- | 0 | -- | AVD33BAK *0.3 | V |
| $V_{OH}$ | Output high voltage | $I_{OH}$=-5.3 mA, AVD33BAK=3.3V | 2.4 | -- | -- | V |
| | | $I_{OH}$=-1.2 mA, AVD33BAK=1.8V | 1.3 | -- | -- | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$=3.9 mA, AVD33BAK=3.3V | -- | -- | 0.4 | V |
| | | $I_{OL}$=1.9 mA, AVD33BAK=1.8V | -- | -- | 0.32 | V |
| $C_i$ | Input capacitance | -- | -- | -- | 10 | pF |
| $R_{PU}$ | Pull-up resistance | -- | 18 | -- | 84 | kOhm |


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### 7.3.3 Type IO-3

**Table 17 Type IO-3**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{IZ}$ | Input leakage current | -- | -- | -- | +/-1 | uA |
| $V_{IH}$ | Input high voltage | -- | AVD33DC2*0.7 | -- | AVD33DC2 | V |
| $V_{IL}$ | Input low voltage | -- | 0 | -- | AVD33DC2 *0.3 | V |
| $V_{OH}$ | Output high voltage | $I_{OH}$=11.9 mA, AVD33DC2=3.3V | 2.64 | -- | -- | V |
| | | $I_{OH}$=2.8 mA, AVD33DC2=1.8V | 1.53 | -- | -- | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$=7.9 mA, AVD33DC2=3.3V | -- | -- | 0.4 | V |
| | | $I_{OL}$=3.9 mA, AVD33DC2=1.8V | -- | -- | 0.45 | V |
| $C_i$ | Input Capacitance | -- | -- | -- | 11 | pF |
| $R_{PU}$ | Pull-up resistance | - | 35 | -- | 84 | kOhm |

### 7.3.4 Type IO-4

**Table 18 Type IO-4**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{IZ}$ | Input leakage current | -- | -- | -- | +/-1 | uA |
| $V_{IH}$ | Input high voltage | -- | AVD33DC1*0.7 | -- | AVD33DC1 | V |
| $V_{IL}$ | Input low voltage | -- | 0 | -- | AVD33DC1 *0.3 | V |
| $V_{OH}$ | Output high voltage | $I_{OH}$=11.9 mA, AVD33DC1=3.3V | 2.64 | -- | -- | V |
| | | $I_{OH}$=2.8 mA, AVD33DC1=1.8V | 1.53 | -- | -- | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$=7.9 mA, AVD33DC1=3.3V | -- | -- | 0.4 | V |
| | | $I_{OL}$=3.9 mA, AVD33DC1=1.8V | -- | -- | 0.45 | V |
| $C_i$ | Input capacitance | -- | -- | -- | 11 | pF |
| $R_{PU}$ | Pull-up resistance | - | 35 | -- | 84 | kOhm |


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### 7.3.5 USB I/O

**Table 19 USB signal**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{IZ}$ | Input leakage current | -- | -- | -- | +/-10 | uA |
| $V_{IH}$ | Input high voltage | -- | AVDUSB*0.9 | -- | AVDUSB | V |
| $V_{IL}$ | Input low voltage | -- | 0 | -- | AVDUSB*0.1 | V |
| $V_{OH}$ | Output high voltage | $I_{OH}$=10 mA, AVDUSB =3.3V | 2.35 | -- | -- | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$=10 mA, AVDUSB =3.3V | -- | -- | 0.5 | V |
| $R_{PUIDEL}$ | Pull-up resistance, idle state | -- | 0.9 | -- | 1.575 | kOhm |
| $R_{PUACTIVE}$ | Pull-up resistance, active state | -- | 1.425 | -- | 3.09 | kOhm |

## 7.4 DC Characteristics

### 7.4.1 Operating Conditions

**Table 20 Operating conditions**

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| AVD33DC1 | Power input for the main power domain | 1.8 | 3.3 | 3.6 | V |
| AVDUSB | USB power input | 3.0 | 3.3 | 3.6 | V |
| AVD33BAK | Power input for the backup power domain | 1.62 | 3.3 | 3.63 | V |
| AVD135M | Main LDO power input | 1.28 | 1.35 | 1.98 | V |
| VDD33_RF | 3.3V RF power input | 1.62 | 3.3 | 3.63 | V |
| VDD135_RF | 1.35V RF power input | 1.28 | 1.35 | 1.98 | V |
| OUTVTCXO | Output power of the external TCXO | -- | 2.8/1.8 | -- | V |
| $ICC_{max}$ | Maximum operating current @ AVD33DC1 | -- | -- | 200 | mA |
| $ICC_{tcxo}$ | Maximum load current @ OUTVTCXO | -- | -- | 4 | mA |
| $ICC_{tcxoL}$ | Maximum load current @ OUTVTCXOL | -- | -- | 4 | mA |


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### 7.4.2 Power Consumption

**Table 21 HD8040 series power consumption**

| Symbol | Parameter | Measure Pin | Typ. | Unit |
|---|---|---|---|---|
| $I_{CCRX1}$[1] | Run Mode (GPS+QZSS, L1 only) | AVD33DC1[4] | 34 | mA |
| $I_{CCRX2}$[2] | Run Mode (All GNSS, L1+L5) | AVD33DC1[4] | 40 | mA |
| $I_{CCDSM}$ | Deep sleep Mode | AVD33DC1[5] | 0.98 | mA |
| $I_{CCRETM}$[3] | Data retention Mode | AVD33DC1[4] | 0.55 | mA |
| $I_{CCDBM}$ | Data backup Mode | AVD33BAK[6] | 9.0 | uA |

* *[1] GPS+QZSS, L1 band only, 16 tracking channels, position fixed*
* *[2] All GNSS, L1 + L5 band, 32 tracking channels, position fixed*
* *[3] Retention voltage = 0.7V*
* *[4] Condition: AVD33DC1=3.3V@Room Temperature; All Pins Open.*
* *[5] When DVFS is used to lower core voltage to 0.9V*
* *[6] Condition: AVD33BAK=3.3V@Room Temperature; All Pins Open.*


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# 8 AC CHARACTERISTICS

All AC timings listed below are under the following conditions

- Core operation voltage = 1.1V
- AVD33DC1 = 3.3V
- Temperature = 25°C

## 8.1 Reset Minimum Timing

**Table 22 Reset minimum timing**

| Parameter | Symbol | Pin | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Reset input time | $t_{RSTL}$ | PRRSTX | There is power supply and the oscillator is stable. | 100 | -- | -- | mS |

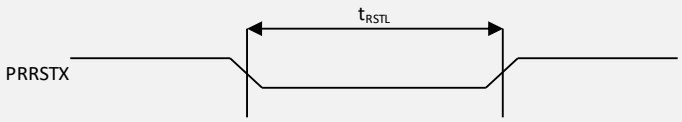



Figure 9 Reset minimum timing

## 8.2 Crystal Oscillation

**Table 23 Crystal oscillation**

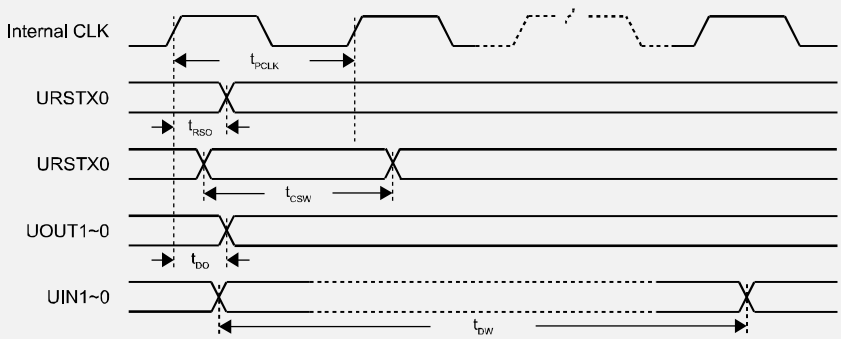
| Parameters | Symbol | Pin | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Main clock oscillation frequency | $f_{OSC}$ | XI, XO | 16 | -- | 40 | MHz |
| Real time clock oscillation frequency | $f_{RTC}$ | RXI, RXO | -- | 32.768 | -- | kHz |

## 8.3 UART Interface Timing

**Table 24 UART interface timing**

| Parameters | Symbol | Pin | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Output delay time | $t_{DO}$ | UOUT1~0 | -- | -- | 10 | nS |
| Input data minimum pulse width | $t_{DW}$ | UIN1~0 | 16 | -- | -- | $t_{PCLK}$[1] |
| UART0 request output delay time | $t_{RSO}$ | URTSX0 | -- | -- | 10 | nS |
| UART0 clear input minimum pulse width | $t_{CSW}$ | UCTSX0 | 1 | -- | -- | $t_{PCLK}$ |

* *[1] $t_{PCLK}$ is APB bus clock cycle time.*





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Figure 10 UART interface timing

## 8.4 I²C Interface Timing

**Table 25 I²C interface timing**

| Parameter | Symbol | Standard Mode | | Fast Mode | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| I2C clock frequency | $f_{SCL}$ | 0 | 100 | 0 | 400 | kHz |
| LOW period of the I2C clock | $t_{LOW}$ | 4.7 | -- | 1.3 | -- | mS |
| HIGH period of the I2C clock | $t_{HIGH}$ | 4.0 | -- | 0.6 | -- | mS |
| Data setup time | $t_{SUDAT}$ | 250 | -- | 100 | -- | nS |
| Data hold time | $t_{HDDAT}$ | 0[2] | 3.45[3] | 0[2] | 0.9[3] | mS |
| Bus free time between a STOP and START condition | $t_{BUF}$ | 4.7 | -- | 1.3 | -- | mS |
| Set-up time for STOP condition | $t_{SUSTO}$ | 4.0 | -- | 0.6 | -- | mS |
| Set-up time for a repeated START condition | $t_{SUSTA}$ | 4.7 | -- | 0.6 | -- | mS |
| Hold time (repeated) START condition | $t_{HDSTA}$ | 4.0 | -- | 0.6 | -- | mS |

* *[2] A device must internally provide a hold time of at least 300ns for the ISA signal to bridge the undefined region of the falling edge of ISL.*

* *[3] The maximum $t_{HDDAT}$ has only to be met if the device does not stretch the LOW period ($t_{LOW}$) of the ISL signal.*

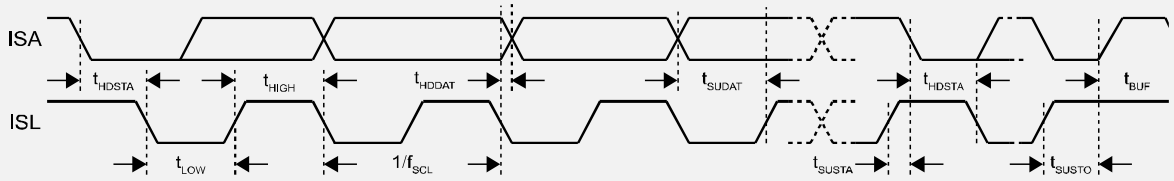



Figure 11 I²C interface timing

## 8.5 Master/Slave SPI Timing

**Table 26 Master/Slave SPI timing**

| Parameters | Symbol | Pin | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| SPI clock frequency | $f_{SCK}$ | SPICK1~0 | -- | -- | 50 | MHz |
| SPI clock frequency pulse width | $f_{SCKPW}$ | | 9 | -- | -- | nS |
| Data input setup time | $t_{SDI}$ | SPIDI | 4 | -- | -- | nS |
| Data input hold time | $t_{HDI}$ | | 6 | -- | -- | nS |
| Data output delay time | $t_{DO}$ | SPIDO | 0.1 | -- | 13.5 | nS |
| Select signal input setup before clock active[4] | $t_{SSSI}$ | SPICX2~0 | 1.7 | -- | -- | $t_{ckop}$ |
| Select signal input hold after clock inactive | $t_{HSSI}$ | | 6 | -- | -- | nS |
| Select signal output active to SPI clock active | $t_{SSO_A}$ | | 6 | -- | -- | nS |
| Select signal output inactive from SPI clock inactive | $t_{SSO_IA}$ | | 6 | -- | -- | nS |
| Word select/Bit clock output delay time[5] | $t_{WSO}$ | | 0.1 | -- | 24 | nS |

* *[4] $t_{ckop}$ is SPI operating clock period*


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* *[5] Applicable only when configured as I2S.*

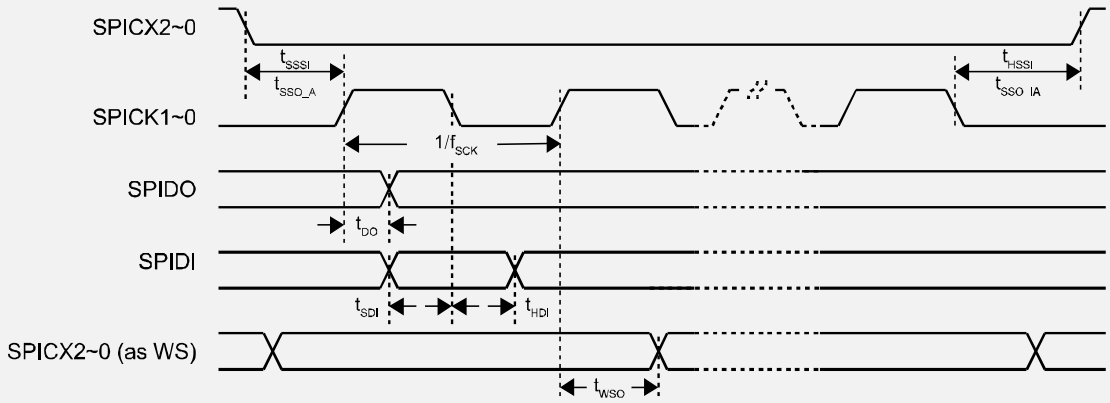



Figure 12 Master/Slave SPI timing

## 8.6 Master SQI/SPI Timing

**Table 27 Master SQI/SPI timing**

| Parameters | Symbol | Pin | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| SQI clock frequency (SPI mode) | $f_{QCK(spi)}$ | SQICK | -- | -- | 76 | MHz |
| SQI clock frequency (SQI mode) | $f_{QCK(sqi)}$ | | -- | -- | 43 | MHz |
| SQI clock output pulse width | $t_{QCKPW}$ | | 5 | -- | -- | nS |
| Data input setup time | $t_{SDI}$ | SQI3~0 | 0.13 | -- | -- | nS |
| Data input hold time | $t_{HDI}$ | | 0.1 | -- | -- | nS |
| Data output delay time | $t_{DO}$ | | 0.1 | -- | 9.1 | nS |
| Select signal output active to SQI clock active | $t_{SSO_A}$ | SQICX | 5 | -- | -- | nS |
| Select signal output inactive from SQI clock inactive | $t_{SSO_IA}$ | | 5 | -- | -- | nS |

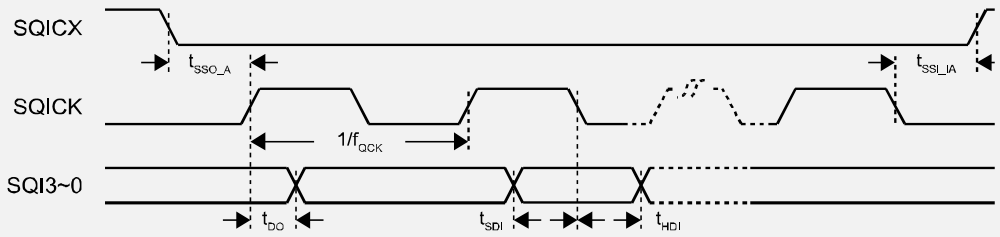



Figure 13 Master SQI/SPI timing

## 8.7 GNSS SYNC Signal Timing

**Table 28 GNSS SYNC signal timing**

| Parameters | Symbol | Pin | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Frequency sync input | $f_{SYNC}$ | FSYNC | -- | -- | 50 | MHz |
| Time sync input minimum pulse width | $t_{PW}$ | TSYNC | 1.5 | -- | -- | $1/f_{OSC}$[6] |

* *[6] $f_{OSC}$ is the main oscillator frequency.*


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## 8.8 GPIO and Other Peripherals Timing

**Table 29 GPIO and other peripherals timing**

| Parameters | Symbol | Pin | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Output delay time from APB clock | $t_{DO}$ | GPIOxx[8] | 0.1 | -- | 19.5 | ns |
| Minimum input pulse width | $t_{PW}$ | | 1.5 | -- | -- | $f_{PCLK}$[7] |

* *[7] $t_{PCLK}$ is APB clock cycle time.*
* *[8] Above parameters are also applied to peripheral functions: PWM output PWM1~0, Input Capture input IN1~0, External Interrupt input INT6~0.*
* *When External Interrupt INT6~0 is selected as level detection, its input level should be held until interrupt process is completed.*

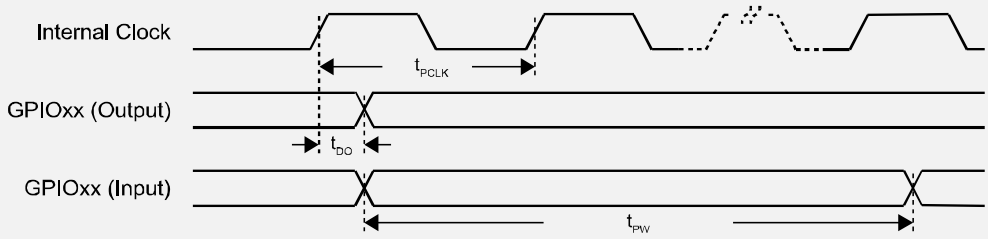



Figure 14 GPIO and other peripherals timing


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# 9 MECHANICAL SPECIFICATION

## 9.1 QFN40

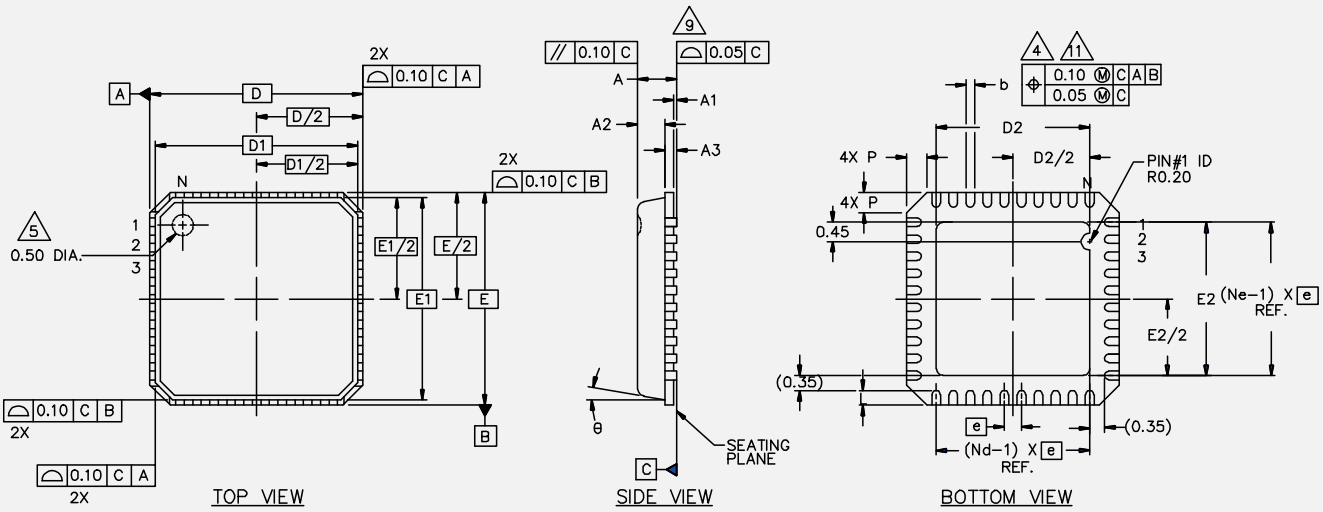



Figure 15 QFN40 Top/side/bottom view

**Table 30 Common dimensions**

| Symbol | Common dimension | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.01 | 0.05 |
| A2 | 0.60 | 0.65 | 0.70 |
| A3 | | 0.20 REF. | |
| D | | 5.00 BSC | |
| D1 | | 4.75 BSC | |
| E | | 5.00 BSC | |
| E1 | | 4.75 BSC | |
| D2 | 3.50 | 3.60 | 3.70 |
| E2 | 3.50 | 3.60 | 3.70 |
| e | | 0.40 BSC | |
| N | | 40 | |
| Nd | | 10 | |
| Ne | | 10 | |
| L | 0.25 | 0.35 | 0.45 |
| b | 0.15 | 0.20 | 0.25 |
| θ | -- | -- | 12° |
| p | 0.24 | 0.42 | 0.60 |


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## 9.2 WLCSP

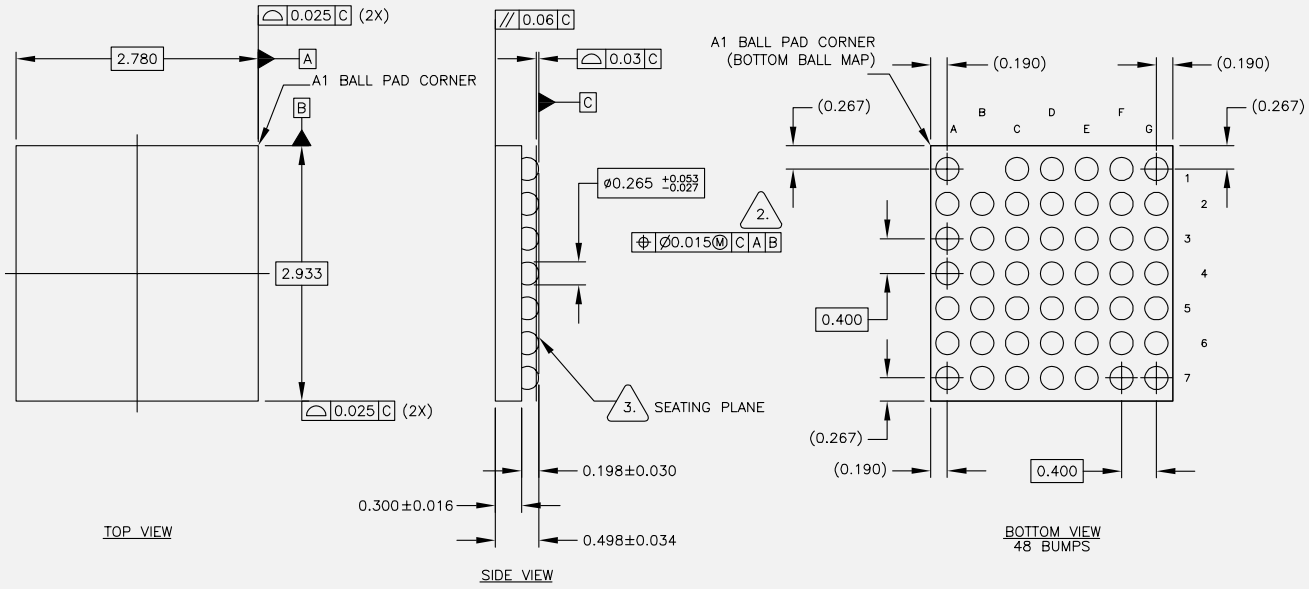



Figure 16 WLCSP Top/side/bottom view

**Table 31 Dimensions**

| Scale | Body X | Body Y | Body Z |
|---|---|---|---|
| 21:1 | 2.780 | 2.933 | 0.498 |
| **Ball count** | **Ball pitch** | **Raw ball diameter** | |
| 48 | 0.400 | 0.250 | |

* *Primary datum C and seating plane are defined by the spherical crowns of the solder balls.*
* *Dimensions is measured at the maximum solder ball diameter, parallel to primary datum C.*
* *All dimensions and tolerances conform to ASME Y14.5 – 1994.*


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# 10 PRODUCT PACKAGING

## 10.1 Packing Hierarchy

The general packing hierarchy differs depending on whether the product is delivered on reels or trays.

**Table 32 Packing hierarchy**

| Chip on tape | Reel | Sealed bag | Packing box | Shipping carton |
|---|---|---|---|---|
|  |  |  |  |  |

### 10.1.1 Reel Packaging

HD8040 series chips are delivered as hermetically sealed, reeled tapes in order to enable efficient production, production lot set-up and tear-down.

- HD8040 series' chips in QFN40 package are deliverable in quantities of 4000pcs on a reel.
- HD8040 series' chips in WLCSP package are deliverable in quantities of 5000pcs on a reel.

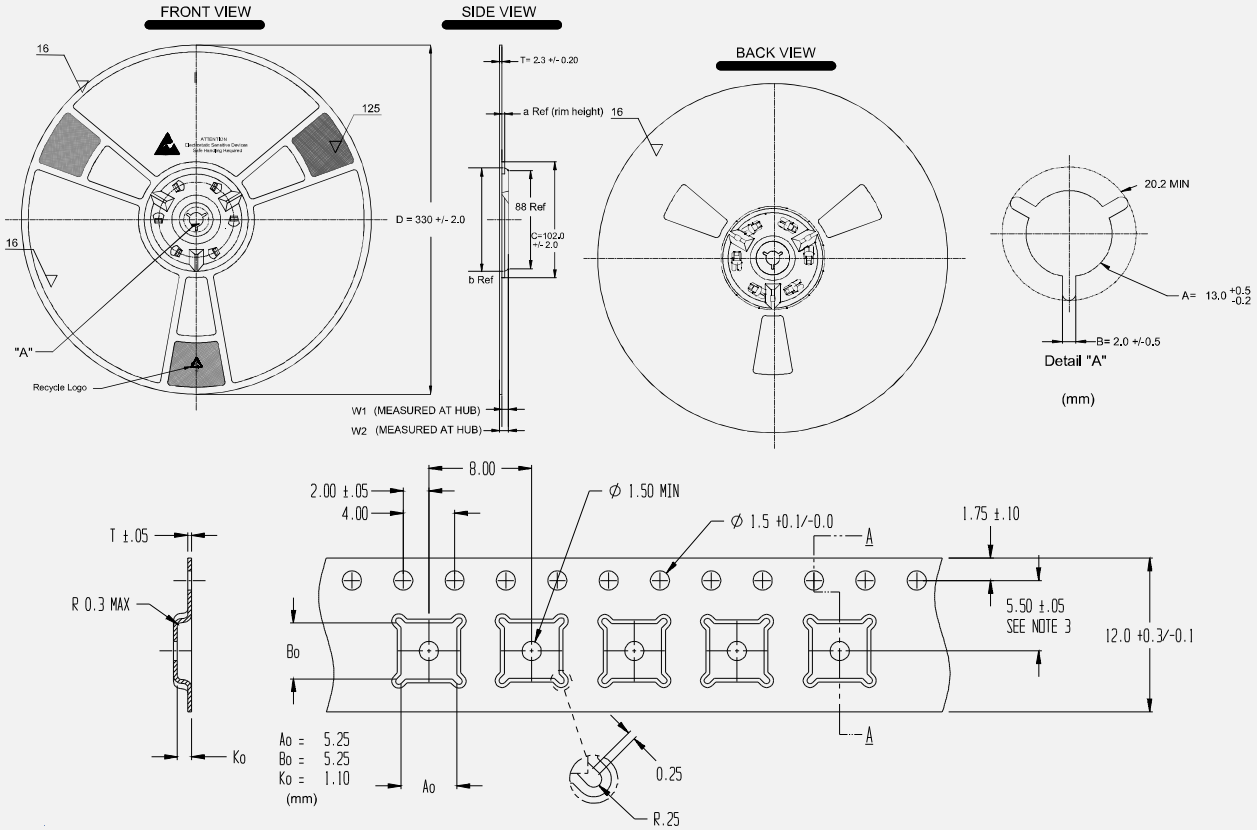



Figure 17 QFN40 Reel and tape dimensions


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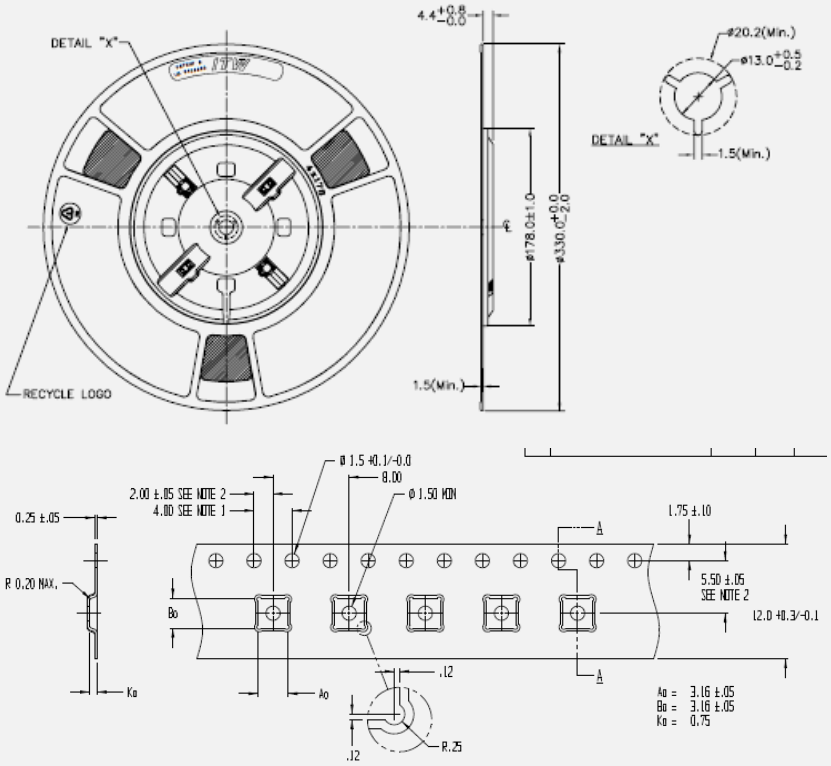



Figure 18 WLCSP Reel and tape dimensions

### 10.1.2 Package Dimensions

The reels of chips are packed in the sealed bags and shipped by the packing boxes and shipping cartons.

**Table 33 Package dimensions**

| Material | Dimension |
|---|---|
| Sealed bag | 410*460*0.15mm |
| Packing box | 353*350*48mm |
| Shipping carton | 370*260*360mm |


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# 11 ORDERING INFORMATION

## 11.1 Product Marking

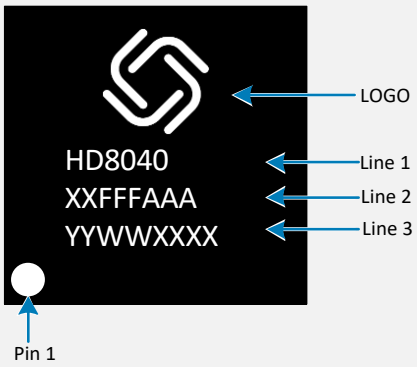



Figure 19 Product marking

**Table 34 Product codes explanation**

| Line | Content | Description |
|---|---|---|
| Logo | -- | Company Logo |
| Line1 | HD8040 | Model |
| Line2 | XXFFFAAA | Reserved |
| Line3 | YY | Year |
| | WW | Week |
| | XXXX | Reserved |


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## 11.2 Ordering Codes

**Table 35 Ordering codes**

| Ordering Number | Category | Package | GNSS | | | | | Features |
|---|---|---|---|---|---|---|---|---|
| | | | GPS/QZS | BDS | GLONASS | Galileo | IRNSS | |
| HD8040-1213NM | Standard Precision | QFN40 | ✓ | ✓ | -- | -- | -- | GPS+BDS (L1 band only) |
| HD8040D-1213NM | High Precision | QFN40 | ✓ | ✓ | ✓ | ✓ | -- | GNSS (multi-band sub-meter accuracy) |
| HD8040S-1213NM | Standard Precision | QFN40 | ✓ | ✓ | -- | -- | -- | Security GNSS chip |
| HD8041-1213NM | Standard Precision | QFN40 | ✓ | ✓ | ✓ | ✓ | -- | GNSS (L1 band only) |
| HD8041D-1213NM | High Precision | QFN40 | ✓ | ✓ | ✓ | ✓ | ✓ | GNSS (multi-band sub-meter accuracy) |
| HD8041S-1213NM | Standard Precision | QFN40 | ✓ | ✓ | ✓ | ✓ | ✓ | Security GNSS chip |
| HD8040-1213WM | Standard Precision | WLCSP | ✓ | ✓ | -- | -- | -- | GPS+BDS (L1 band only) |
| HD8040D-1213WM | High Precision | WLCSP | ✓ | ✓ | ✓ | ✓ | -- | GNSS (multi-band sub-meter accuracy) |
| HD8040S-1213WM | Standard Precision | WLCSP | ✓ | ✓ | -- | -- | -- | Security GNSS chip |
| HD8041-1213WM | Standard Precision | WLCSP | ✓ | ✓ | ✓ | ✓ | -- | GNSS (L1 band only) |
| HD8041D-1213WM | High Precision | WLCSP | ✓ | ✓ | ✓ | ✓ | ✓ | GNSS (multi-band sub-meter accuracy) |
| HD8041S-1213WM | Standard Precision | WLCSP | ✓ | ✓ | ✓ | ✓ | ✓ | Security GNSS chip |
| HD8040DW-1213NM | High Precision | QFN40 | ✓ | ✓ | -- | ✓ | -- | GNSS (multi-band sub-meter accuracy), raw data output |
| HD8040D-1313NM | High Precision | QFN40 | ✓ | ✓ | ✓ | ✓ | -- | GNSS (multi-band sub-meter accuracy) |
| HD8040DW-1313NM | High Precision | QFN40 | ✓ | ✓ | -- | ✓ | -- | GNSS (multi-band sub-meter accuracy), raw data output |


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# 12 RELATED DOCUMENTS

[1] Satrack User Manual

[2] Cynosure Receiver Protocol

# 13 REVISION HISTORY

| Revision | Date | Reviser | Status / Comments |
|---|---|---|---|
| V1.0 | 2018-08-15 | Daisy | Start version, first released |
| V1.1 | 2018-11-12 | Daisy | Updates section 1.4, 6.7. |
| V1.2 | 2018-11-30 | Daisy | Updates table 9 |
| V1.3 | 2019-04-24 | Daisy | Updates HD8040 series product table<br>Add 4.1.7; updates Table 6, 12, 13, 16, 17, 19, 41;<br>Updates Figure 2<br>Add WLCSP package contents<br>Change VDDE to AVD33DC2 |
| V1.4 | 2019-09-11 | Vita Wu | Updates 5.1.1;<br>Updates sensitivity in Section 1.4;<br>Updates main voltage to 1.8~3.6V (in Section 1.4 and 7.4.1);<br>Updates the number of UART interface in Section 3.6.1; |
| V1.5 | 2019-12-12 | Vita Wu | Updates Ordering Number in *Section 11.2 Ordering Codes*; |
| V1.6 | 2020-04 | Vita Wu | Adds external pull-down resistance description in *Section 5.1.1*. |
| V1.7 | 2020-10 | Vita Wu | Includes HD8040DW info.<br>Updates power consumption in running mode. |
| V1.8 | 2020-12 | Vita Wu | Clarify the power on/off sequence.<br>Fix AVD33BAK voltage to be 1.62V of min., and 3.63V of max. |
| V1.9 | 2021-06 | Vita Wu | Includes HD8040DW-1313NM and HD8040-1313NM code in Table 35. |
| | | | |
| | | | |


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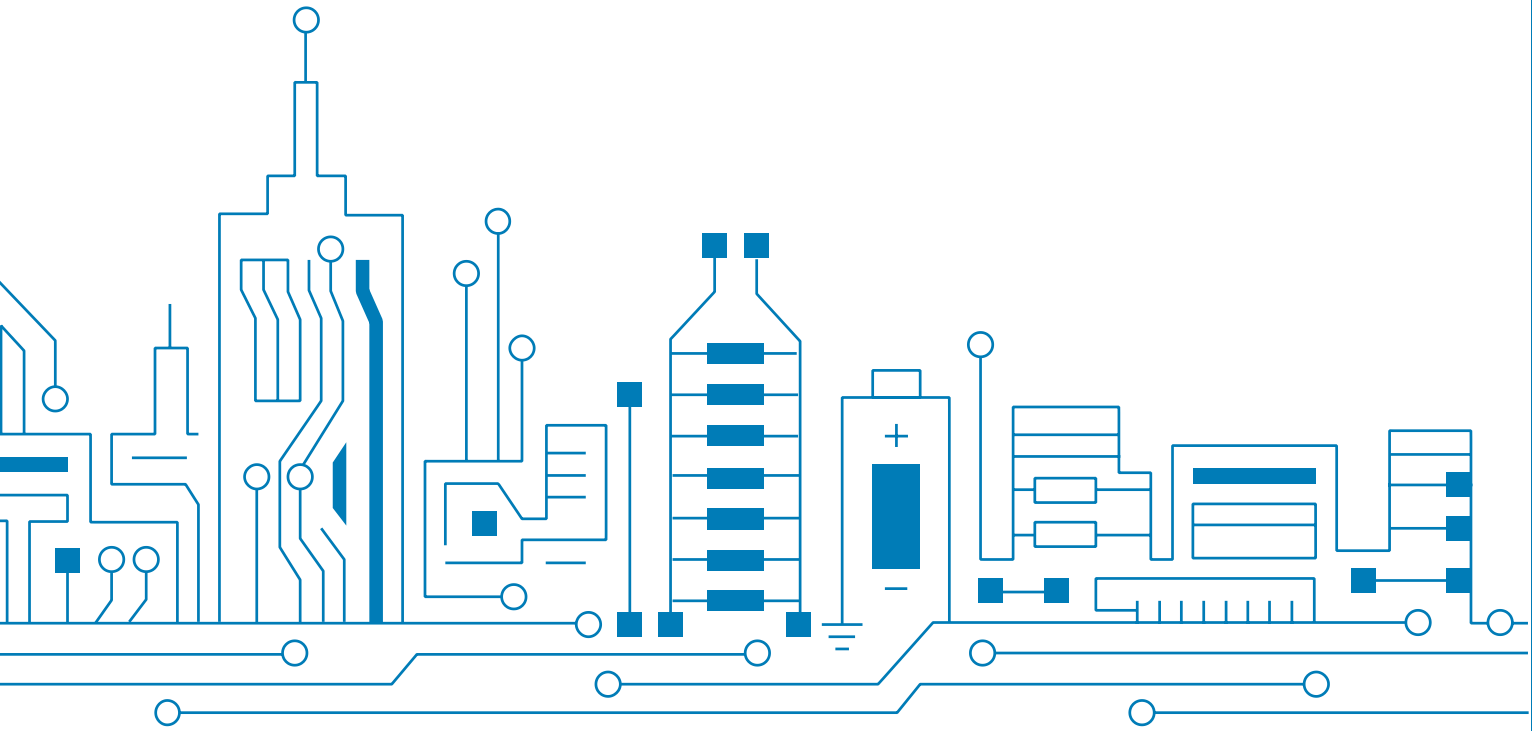
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